LatticeECP2/M Pin Assignment Recommendations

August 2009 Technical Note TN1159

Introduction

The LatticeECP2™ and LatticeECP2M™ device families are designed for high-speed FPGA system applications. As with any high-speed system design, care must be given to certain critical pins that are designed to supply the device with proper reference or supply voltage. For a given package, the general VCC and GND pins are designed to supply the device with the best power and ground reference. The packages have multiple VCC and GND pins and these are the obvious pins to take care of when the boards are designed.

In addition to the general VCC and GND pins, both the LatticeECP2 and LatticeECP2M devices have VCCPLL (PLL power supply) and XRES (External Reference Resistor) pins that supply the external references to the on-chip high-speed circuitry. Care must be given to isolate noise from these pins.

For the LatticeECP2M with high-speed SERDES operation, the SERDES transmit and receive supplies must also be isolated from noise.

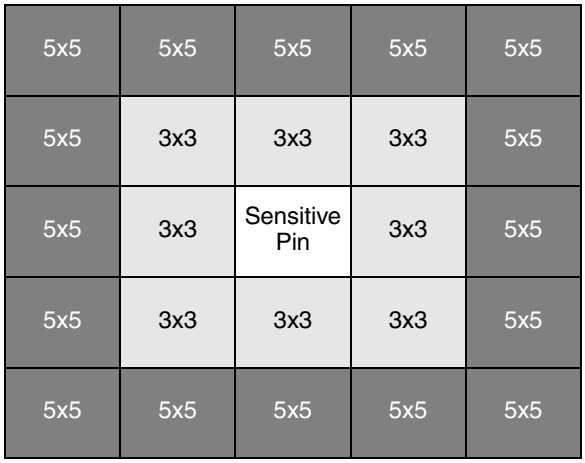
General Package Pin Considerations for Noise

LatticeECP2/M FPGAs come in two general package types, QFP and BGA.

When considering pin assignments for QFP packages, “pin adjacency” is defined as the pins on either side of a given “sensitive” pin.

For BGA packages, the 3x3 and 5x5 diagram shown in Figure 1 defines pin adjacency. Specific 3x3 and 5x5 pins for all LatticeECP2/M packages are given in Appendix A.

Figure 1. BGA Pin Adjancency



Pin Assignment Criteria

Once the sensitive pin is identified, general pin assignment surrounding the sensitive pin should be done in the following order.

1. Place I/O pins outside of the 5x5 adjacent balls for BGA.
2. Next, place I/O pins outside of the 3x3 adjacent balls for BGA packages and away from the adjacent pins for QFP packages.

3. When placing I/O pins, start by assigning inputs to the adjacent pins.
4. If outputs must be assigned to the adjacent pins, start with differential or reduced swing output standards first.
5. For LVCMOS outputs, start from 1.2V output and go up to 3.3V. Use the slow slew setting when possible.

Pin Assignment Guidelines for I/O Pins within the 3x3 and 5x5 Adjacency

When utilizing the I/O pins within the 3x3 and 5x5 array, use the following guidelines in the given order.

1. Assign static logic signals.
2. When assigning dynamic logic signals, start with the signal that has the least amount of activity (i.e., low activity factor).
3. Begin with input signals before assigning output signals.
4. When assigning outputs, start with the weakest output drive and slowest slew rate before going to stronger output drives and faster slew rates.

User System PCB Considerations

The following system or PCB layout considerations should be used when assigning user I/O pins next to the sensitive pins.

1. Minimize the capacitive load for outputs.
2. If possible, assign individual signals as opposed to bus signals that have the possibility of switching multiple outputs simultaneously.
3. PCB traces for these adjacent signal should have well matched impedance to reduce reflective signal noise.
4. Minimize PCB trace cross-talk by avoiding parallel traces.

LatticeECP2M SERDES Related Pin Assignment Recommendations

With high-speed switching of the SERDES pins special care must be given to the pin assignment surrounding the SERDES block. The following guidelines should be applied when assigning the general purpose I/O pins close to the SERDES block. The SERDES recommendations are needed if and only if SERDES channels are used on the ECP2M devices.

1. Place general purpose I/O pins outside of the 5x5 adjacent balls relative to the [LOC]_SQ_VCCRXm and [LOC]_SQ_VCCTXm.
2. Avoid assigning high-speed output pins at the top and bottom I/O banks closest to the SERDES block.
   a. I/O bank 1 is the closest bank to the upper-right SERDES block on LatticeECP2M20 and LatticeECP2M35.
   b. I/O bank 1 is the closest bank to the upper-right SERDES block and I/O bank 4 is the closest bank to the lower-right SERDES block on LatticeECP2M50.
   c. I/O banks 0 and 1 are the closest banks to the upper-left and upper-right SERDES blocks, respectively, on LatticeECP2M70 and LatticeECP2M100. I/O banks 4 and 5 are the closest banks to the lower-right and lower-left SERDES blocks, respectively, on LatticeECP2M70 and LatticeECP2M100.
3. After applying recommendations 1 and 2 above, review the LatticeECP2M pinout from the standpoint of BGA ball locations. Avoid assigning high-speed outputs to the I/O balls physically closest to the SERDES

block from the BGA package view. To determine this, draw a boundary of I/O ball locations of the SERDES balls, not including the VCC, GND and NC balls on either side of the SERDES bank. Make sure that there is at least one static ball location outside of this boundary. If a general purpose I/O pin falls on this boundary, avoid assigning high-speed outputs to these balls.

4. When using the general purpose PLLs from the FPGA fabric in conjunction with the SERDES, place the general-purpose I/O pins outside of the 3x3 adjacent balls relative to the VCCPLL and XRES pins.

For additional hardware recommendations, refer to TN1162, LatticeECP2/M Hardware Checklist for power supply and configuration hardware pin assignment recommendations.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
September 2007	01.0	Initial release.
August 2009	01.1	Added ECP2M-50 fpBGA672 missing table to the appendix.

Appendix A. 3x3 and 5x5 Pin Table

Special_Pad	3x3	5x5
Device=ecp2-06; PKG=fpbga256		
xres	pt6a;pt5b;pt2b;pt2a;pt4b;pt4a;pl9a	pt6b;pt5a;pt3b;pt13a;pl4a;pt10a;pl4b;pt10b;pl8a;pl9b;pl8b
Device=ecp2-12; PKG=fpbga256		
xres	pt24a;pt23b;pt2b;pt2a;pt22b;pt22a;pl9a	pt24b;pt23a;pt21b;pt31a;pl4a;pt28a;pl4b;pt28b;pl8a;pl9b;pl8b
Device=ecp2-12; PKG=fpbga484		
xres	pt34b;pt33b;pt25b;pt25a	pt37b;pt34a;pt33a;pt18b;pt36b;pt18a;pt36a;pt15b
Device=ecp2-20; PKG=fpbga256		
xres	pt33a;pt32b;pt2b;pt2a;pt31b;pt31a;pl15a	pt33b;pt32a;pt30b;pt40a;pl6a;pt37a;pl6b;pt37b;pl14a;pl15b;pl14b
Device=ecp2-20; PKG=fpbga484		
xres	pt43b;pt42b;pt34b;pt34a	pt46b;pt43a;pt42a;pt27b;pt45b;pt27a;pt45a;pt24b
Device=ecp2-20; PKG=fpbga672		
xres	pt54a;pt49a;pt43b;pt43a	pt53b;pt47a;pt39b;pt41b;pt53a;pt37b;pt63a
Device=ecp2-35; PKG=fpbga484		
vccpll	pr40a;pr25b;pr40b;pr46a;pr46b	pr24a;pr24b;pr23b;pr25a;pr28b;pr42a;pr45b;pr52a;pr52b;pr58a;pr58b
xres	pt43b;pt42b;pt34b;pt34a	pt46b;pt43a;pt42a;pt27b;pt45b;pt27a;pt45a;pt24b
Device=ecp2-35; PKG=fpbga672		
vccpll	pr30b;pr28b;pr34a	pr21b;pr21a;pr30a;pr40b;pr42b
xres	pt54a;pt49a;pt43b;pt43a	pt53b;pt47a;pt39b;pt41b;pt53a;pt37b;pt72a
Device=ecp2-50; PKG=fpbga484		
vccpll	pr26b;pr26a;pr39b;pr42a	pr15b;pt75b;pt75a;pr25a;pr39a;pr41b;pr42b;pr44a
xres	pt52b;pt51b;pt43b;pt43a	pt55b;pt52a;pt51a;pt36b;pt54b;pt36a;pt54a;pt33b
Device=ecp2-50; PKG=fpbga672		
vccpll	pr38b;pr17b;pr13b;pr43b;pr17a;pr38a;pr40b;pr40a	pr15b;pr13a;pt81a;pr43a;pr39b;pr39a;pr51b;pr47a;pr49a;pr49b;pr47b
xres	pt68b;pt63a;pt58a;pt52b;pt52a	pt67a;pt62b;pt56a;pt48b;pt50b;pt62a;pt46b;pt81a
Device=ecp2-50; PKG=fpbga900		
llm0_vccpll	pl61b;pl59b;pl61a;pl64b;pl66b;pl68a;pl66a	pl57a;pl55a;pl57b;pl55b;pl59a;pl64a;pl68b;pl78b;pl72a;pl70a;pl72b;pl70b
lum0_vccpll	pl25b;pl26b;pl38b;pl38a;pl42b;pl44b	pl21a;pl23a;pl21b;pl25a;pl40a;pl42a;pl37a;pl49b;pl47b;pl49a
rlm0_vccpll	pr42b;pr49b;pr53a	pr40a;pr38a;pr44b;pr47b;pr51a;pr55a;pr57a
rum0_vccpll	pr25b;pr38a;pr42b	pr23a;pr21a;pr26b;pr40a;pr44b;pr47b;pr49b
xres	pt44a;pt44b	pt56a;pt53b;pt48b;pt42a;pt36b
Device=ecp2-70; PKG=fpbga672		
vccpll	pr62b;pr60b;pr66a;pr67a	pr53b;pr53a;pr62a;pr67b;pr72b;pr74b
xres	pt77b;pt72a;pt67a;pt61b;pt61a	pt76a;pt71b;pt65a;pt57b;pt59b;pt71a;pt55b;pt99a
Device=ecp2-70; PKG=fpbga900		
vccpll	pl74b;pl72b;pl74a;pl77b;pl79b;pl81a;pl79a	pl70a;pl68a;pl70b;pl68b;pl72a;pl77a;pl81b;pl91b;pl85a;pl83a;pl85b;pl83b
xres	pt53a;pt53b	pt65a;pt62b;pt57b;pt51a;pt45b

Special_Pad	3x3	5x5
Device=ecp2m-20; PKG=fpbga256		
urc_sq_vccrx0	pr9a;pr9b;pr11b;pr11a	pr31b;pr13b
urc_sq_vccrx1	pr11a	pr9a;pr9b;pr11b;pr31b;pr13b;pr12a
urc_sq_vccrx2	pl3a	pl2a;pl2b;pl3b;pl6a;pl4b;pl4a
urc_sq_vccrx3	pl2b;pl3b;pl3a;pl6a	pl2a;pl5a;pl5b;pl6b;pl4b;pl4a;pl7a
urc_sq_vcctx0	NONE	pr13b;pr12a
urc_sq_vcctx1	NONE	pr13b;pr12a
urc_sq_vcctx2	NONE	pl4b
urc_sq_vcctx3	NONE	pl4b;pl4a
vccpll	pr12b;pr14a;pr14b	pr12a;pr13a;pr42a;pr27a;pr27b
xres	pl4b;pl4a;pl9b;pl8a;pl11a;pl11b	pl3a;pl6a;pl9a;pl8b;pl24a;pl12b;pl24b;pl27b;pl27a; pl14b;pl14a
Device=ecp2m-20; PKG=fpbga484		
urc_sq_vccrx0	pr14a	pr13a;pr14b;pr13b
urc_sq_vccrx1	pr14a;pr13a	pr12b;pr14b;pr13b;pr12a
urc_sq_vccrx2	pt28a;pt21b;pt21a	pt27b;pt18b;pt18a;pt28b;pt25b;pt22a;pt15b;pt11a
urc_sq_vccrx3	pt18b;pt21b;pt21a;pt18a	pt27b;pt27a;pt23a;pt12b;pt28a;pt12a;pt25b;pt22a; pt15b;pt11a;pt11b
urc_sq_vcctx0	pr13a;pr12b;pr9a	pr13b;pr12a;pr9b
urc_sq_vcctx1	pr12b;pr9a	pr13a;pr13b;pr12a;pr9b
urc_sq_vcctx2	NONE	pt28a;pt28b;pt25b
urc_sq_vcctx3	pt28a	pt21b;pt28b;pt25b;pt22a
vccpll	pr43b;pr51b;pr49b;pb39b	pr39b;pr41a;pr43a;pr49a;pr51a;pb37b;pr52b;pr52a; pb43b;pb39a;pb36b
xres	pr15a;pr15b;pr19b	pr9a;pr9b;pr11b;pr19a;pr22a;pr22b
Device=ecp2m-35; PKG=fpbga256		
urc_sq_vccrx0	pr9a;pr9b;pr11b;pr11a	pr41b;pr13b
urc_sq_vccrx1	pr11a	pr9a;pr9b;pr11b;pr41b;pr13b;pr12a
urc_sq_vccrx2	pl3a	pl2a;pl2b;pl3b;pl6a;pl4b;pl4a
urc_sq_vccrx3	pl2b;pl3b;pl3a;pl6a	pl2a;pl5a;pl5b;pl6b;pl4b;pl4a;pl7a
urc_sq_vcctx0	NONE	pr13b;pr12a
urc_sq_vcctx1	NONE	pr13b;pr12a
urc_sq_vcctx2	NONE	pl4b
urc_sq_vcctx3	NONE	pl4b;pl4a
vccpll	pr12b;pr14a;pr14b	pr12a;pr13a;pr57a;pr37a;pr37b
xres	pl4b;pl4a;pl9b;pl8a;pl11a;pl11b	pl3a;pl6a;pl9a;pl8b;pl34a;pl12b;pl34b;pl37b;pl37a; pl14b;pl14a
Device=ecp2m-35; PKG=fpbga484		
urc_sq_vccrx0	pr14a	pr13a;pr14b;pr13b
urc_sq_vccrx1	pr14a;pr13a	pr12b;pr14b;pr13b;pr12a
urc_sq_vccrx2	pt46a;pt39b;pt39a	pt45b;pt36b;pt36a;pt46b;pt43b;pt40a;pt33b;pt29a
urc_sq_vccrx3	pt36b;pt39b;pt39a;pt36a	pt45b;pt45a;pt41a;pt30b;pt46a;pt30a;pt43b;pt40a; pt33b;pt29a;pt29b
urc_sq_vcctx0	pr13a;pr12b;pr9a	pr13b;pr12a;pr9b
urc_sq_vcctx1	pr12b;pr9a	pr13a;pr13b;pr12a;pr9b
urc_sq_vcctx2	NONE	pt46a;pt46b;pt43b

Special_Pad	3x3	5x5
urc_sq_vcctx3	pt46a	pt39b;pt46b;pt43b;pt40a
vccpll	pr58b;pr66b;pr64b;pb57b	pr49b;pr51a;pr58a;pr64a;pr66a;pb55b;pr67b;pr67a; pb61b;pb57a;pb54b
xres	pr25a;pr25b;pr29b	pr9a;pr9b;pr11b;pr29a;pr32a;pr32b
Device=ecp2m-35; PKG=fpbga672		
urc_sq_vccrx0	NONE	pr9b;pr9a
urc_sq_vccrx1	NONE	pr9b;pr9a
urc_sq_vccrx2	pt43a;pt40b;pt40a	pt35b;pt37b;pt45a;pt34b;pt43b;pt42a;pt41a;pt38a; pt39a
urc_sq_vccrx3	pt37b;pt40b;pt40a;pt34b	pt35b;pt35a;pt36b;pt43a;pt31b;pt42a;pt41a;pt38a; pt39a;pt30b
urc_sq_vcctx0	NONE	pr9b;pr9a
urc_sq_vcctx1	NONE	pr9a
urc_sq_vcctx2	pt46a;pt45a	pt43a;pt46b;pt43b;pt42a
urc_sq_vcctx3	pt46a;pt45a;pt43a	pt40b;pt46b;pt43b;pt42a;pt41a
r_vccpll	pt44b;pt44a;pt42b;pr12b;pt33b	pt46b;pr12a;pt45b;pr19b;pt41b;pr22b;pt38b;pr23a;pr21a;pr19a;pr14b
l_vccpll	pl45a;pl47a	pl42a;pl38b;pl40a;pl45b;pl67b;pl63a;pl60a;pl49b
xres	pt42b;pr12b;pt33b;pr21a;pr19a;pr14b	pr12a;pt44b;pt44a;pt45b;pr19b;pt41b;pr22b;pt38b;pr23a;pr25a;pr23b;pr16a;pr22a
Device=ecp2m-50; PKG=fpbga484		
urc_sq_vccrx0	pr14a	pr13a;pr14b;pr13b
urc_sq_vccrx1	pr14a;pr13a	pr12b;pr14b;pr13b;pr12a
urc_sq_vccrx2	pt55a;pt48b;pt48a	pt54b;pt45b;pt45a;pt55b;pt52b;pt49a;pt42b;pt38a
urc_sq_vccrx3	pt45b;pt48b;pt48a;pt45a	pt54b;pt54a;pt50a;pt39b;pt55a;pt39a;pt52b;pt49a; pt42b;pt38a;pt38b
urc_sq_vcctx0	pr13a;pr12b;pr9a	pr13b;pr12a;pr9b
urc_sq_vcctx1	pr12b;pr9a	pr13a;pr13b;pr12a;pr9b
urc_sq_vcctx2	NONE	pt55a;pt55b;pt52b
urc_sq_vcctx3	pt55a	pt48b;pt55b;pt52b;pt49a
vccpll	pr63b;pb66b	pr53b;pr55a;pr63a;pb64b;pb70b;pb66a;pb63b
xres	pr29a;pr29b;pr33b	pr9a;pr9b;pr11b;pr33a;pr36a;pr36b
Device=ecp2m-50; PKG=fpbga672		
urc_sq_vccrx0	NONE	pr9b;pr9a
lrc_sq_vccrx0	NONE	NONE
urc_sq_vccrx1	NONE	pr9b;pr9a
lrc_sq_vccrx1	NONE	NONE
urc_sq_vccrx2	pt52a;pt49b;pt49a	pt44b;pt46b;pt54a;pt43b;pt52b;pt51a;pt50a;pt47a; pt48a
lrc_sq_vccrx2	pb57a;pb50b;pb49a	pb59b;pb58a;pb51a;pb42b;pb33b;pb58b;pb43b; pb44b;pb44a
urc_sq_vccrx3	pt46b;pt49b;pt49a;pt43b	pt44b;pt44a;pt45b;pt52a;pt40b;pt51a;pt50a;pt47a; pt48a;pt39b
lrc_sq_vccrx3	pb50b;pb49a;pb43b;pb44b	pb58a;pb51a;pb42b;pb33b;pb19b;pb57a;pb33a; pb37a;pb44a;pb37b
urc_sq_vcctx0	NONE	pr9b;pr9a
lrc_sq_vcctx0	NONE	pb50a

Special_Pad	3x3	5x5
urc_sq_vcctx1	NONE	pr9a
lrc_sq_vcctx1	NONE	pb50a
urc_sq_vcctx2	pt55a;pt54a	pt52a;pt55b;pt52b;pt51a
lrc_sq_vcctx2	pb61b;pb58b	pb63b;pb59b;pb58a;pb57a
urc_sq_vcctx3	pt55a;pt54a;pt52a	pt49b;pt55b;pt52b;pt51a;pt50a
lrc_sq_vcctx3	pb61b;pb58b;pb57a	pb63b;pb59b;pb58a;pb51a;pb50b
l_vccpll	pl49a;pl51a	pl46a;pl44b;pl42b;pl44a;pl49b;pl72b;pl68a;pl65a; pl53b
r_vccpll	pt53b;pt53a;pt51b;pr12b;pt42b	pt55b;pr12a;pt54b;pr23b;pt50b;pr26b;pt47b;pr27a; pr25a;pr23a;pr14b
xres	pt51b;pr12b;pt42b;pr25a;pr23a;pr14b	pr12a;pt53b;pt53a;pt54b;pr23b;pt50b;pr26b;pt47b; pr27a;pr29a;pr27b;pr19a;pr26a
Device=ecp2m-50; PKG=fpbga900		
urc_sq_vccrx0	NONE	pr20b;pr20a
lrc_sq_vccrx0	NONE	NONE
urc_sq_vccrx1	NONE	pr12b;pr20b;pr20a;pr12a
lrc_sq_vccrx1	NONE	NONE
urc_sq_vccrx2	pt68b;pt66b;pt65b	pt64b;pt64a;pt65a;pt68a;pt73a;pt67b;pt67a;pt66a
lrc_sq_vccrx2	pb55a;pb67b;pb56a	pb57a;pb58b;pb51a;pb55b;pb62a;pb62b;pb54b
urc_sq_vccrx3	pt64a;pt65a;pt66b;pt65b	pt64b;pt54b;pt54a;pt50b;pt68b;pt50a;pt67b;pt67a; pt66a;pt47a
lrc_sq_vccrx3	pb67b;pb56a;pb62a;pb62b	pb58b;pb51a;pb42a;pb55a;pb52b;pb54a;pb56b; pb54b;pb50b
urc_sq_vcctx0	pr12b;pt72b	pr20a;pr12a;pt72a
lrc_sq_vcctx0	NONE	pb64a
urc_sq_vcctx1	pr12b;pt72b	pr12a;pt72a
lrc_sq_vcctx1	NONE	pb64a
urc_sq_vcctx2	pt73b;pt70b;pt68a	pt68b;pt71b;pt73a;pt67b
lrc_sq_vcctx2	pb57b;pb55b	pb57a;pb55a
urc_sq_vcctx3	pt70b;pt68a;pt68b	pt73b;pt66b;pt71b;pt73a;pt67b;pt67a
lrc_sq_vcctx3	pb57b;pb55b;pb55a	pb57a;pb58b;pb67b
vccpll	NONE	NONE
xres	pr9b;pr13b;pt71a	pt71b;pt73a;pr9a;pt70a;pr11a;pr13a;pr14a;pr14b
Device=ecp2m-70; PKG=fpbga900		
llc_sq_vccrx0	pb50b;pb49b;pb49a;pb58a	pb47b;pb39b;pb40a;pb53b;pb50a;pb53a;pb51b; pb61a;pb59a;pb58b
lrc_sq_vccrx0	NONE	NONE
ulc_sq_vccrx0	pt51a;pt54b;pt50b;pt37b	pt57b;pt51b;pt57a;pt55b;pt55a;pt30a;pt54a;pt37a; pt30b
urc_sq_vccrx0	pr25b;pr25a	pr14b;pr30b;pr30a;pr14a
llc_sq_vccrx1	pb50b;pb49b;pb53a	pb39b;pb40a;pb53b;pb30a;pb48a;pb49a;pb58a; pb58b
lrc_sq_vccrx1	NONE	NONE
ulc_sq_vccrx1	pt50b;pt37b;pt30a	pt51b;pt51a;pt54b;pt37a;pt30b
urc_sq_vccrx1	pr25b;pr25a;pr14b	pr12b;pr30b;pr30a;pr14a;pr12a
llc_sq_vccrx2	pb34b;pb34a	pb37b;pb37a;pb38a
lrc_sq_vccrx2	pb64a;pb76b;pb65a	pb66a;pb67b;pb60a;pb64b;pb71a;pb71b;pb63b

Special_Pad	3x3	5x5
ulc_sq_vccrx2	pl9b;pl9a;pl14b	pt47b;pl12b;pl12a;pl14a;pl17a
urc_sq_vccrx2	pt77b;pt75b;pt74b	pt73b;pt73a;pt74a;pt77a;pt82a;pt76b;pt76a;pt75a
llc_sq_vccrx3	pb34a	pb37a;pb34b
lrc_sq_vccrx3	pb76b;pb65a;pb71a;pb71b	pb67b;pb60a;pb51a;pb64a;pb61b;pb63a;pb65b; pb63b;pb59b
ulc_sq_vccrx3	pl9a;pl14b	pl9b;pl12a;pl14a;pl17a
urc_sq_vccrx3	pt73a;pt74a;pt75b;pt74b	pt73b;pt63b;pt63a;pt59b;pt77b;pt59a;pt76b;pt76a; pt75a;pt56a
llc_sq_vcctx0	pb53a;pb48a;pb48b	pb40a;pb53b;pb30a;pb41b;pb49b;pb41a
lrc_sq_vcctx0	NONE	pb73a
ulc_sq_vcctx0	pt30a;pt39a	pt37b;pt43a;pt30b;pt39b
urc_sq_vcctx0	pr14b;pr12b;pt81b	pr25a;pr30a;pr14a;pr12a;pt81a
llc_sq_vcctx1	pb48a;pb48b;pb41a	pb53b;pb30a;pb41b;pb53a
lrc_sq_vcctx1	NONE	pb73a
ulc_sq_vcctx1	pt39a;pt43a	pt30a;pt39b
urc_sq_vcctx1	pr12b;pt81b	pr14b;pr14a;pr12a;pt81a
llc_sq_vcctx2	pb38b;pb38a	pb37b;pb37a;pb34b
lrc_sq_vcctx2	pb66b;pb64b	pb66a;pb64a
ulc_sq_vcctx2	pt47a;pt47b	pl9b;pt46b;pl12b;pl12a
urc_sq_vcctx2	pt82b;pt79b;pt77a	pt77b;pt80b;pt82a;pt76b
llc_sq_vcctx3	pb38b;pb38a;pb34b	pb37b;pb37a;pb34a
lrc_sq_vcctx3	pb66b;pb64b;pb64a	pb66a;pb67b;pb76b
ulc_sq_vcctx3	pt47a;pt47b;pl9b	pl9a;pt46b;pl12b;pl12a;pl14a
urc_sq_vcctx3	pt79b;pt77a;pt77b	pt82b;pt75b;pt80b;pt82a;pt76b;pt76a
vccpll	NONE	NONE
xres	pr9b;pr13b;pt80a;pr15a;pr15b	pt80b;pt82a;pr9a;pt79a;pr11a;pr13a;pr20a;pr20b
Device=ecp2m-100; PKG=fpbga900		
llc_sq_vccrx0	pb59b;pb58b;pb58a;pb67a	pb56b;pb48b;pb49a;pb62b;pb59a;pb62a;pb60b; pb70a;pb68a;pb67b
lrc_sq_vccrx0	NONE	NONE
ulc_sq_vccrx0	pt60a;pt63b;pt59b;pt46b	pt66b;pt60b;pt66a;pt64b;pt64a;pt30a;pt63a;pt46a; pt30b
urc_sq_vccrx0	pr29b;pr29a	pr14b;pr34b;pr34a;pr14a
llc_sq_vccrx1	pb59b;pb58b;pb62a	pb48b;pb49a;pb62b;pb30a;pb57a;pb58a;pb67a; pb67b
lrc_sq_vccrx1	NONE	NONE
ulc_sq_vccrx1	pt59b;pt46b;pt30a	pt60b;pt60a;pt63b;pt46a;pt30b
urc_sq_vccrx1	pr29b;pr29a;pr14b	pr12b;pr34b;pr34a;pr14a;pr12a
llc_sq_vccrx2	pb34b;pb34a	pb37b;pb37a;pb38a
lrc_sq_vccrx2	pb73a;pb94b;pb74a	pb75a;pb76b;pb69a;pb73b;pb80a;pb80b;pb72b
ulc_sq_vccrx2	pl9b;pl9a;pl14b	pt56b;pl12b;pl12a;pl14a;pl17a
urc_sq_vccrx2	pt95b;pt93b;pt92b	pt91b;pt91a;pt92a;pt95a;pt100a;pt94b;pt94a;pt93a
llc_sq_vccrx3	pb34a	pb37a;pb34b
lrc_sq_vccrx3	pb94b;pb74a;pb80a;pb80b	pb76b;pb69a;pb60a;pb73a;pb70b;pb72a;pb74b; pb72b;pb68b
ulc_sq_vccrx3	pl9a;pl14b	pl9b;pl12a;pl14a;pl17a

Special_Pad	3x3	5x5
urc_sq_vccrx3	pt91a;pt92a;pt93b;pt92b	pt91b;pt72b;pt72a;pt68b;pt95b;pt68a;pt94b;pt94a; pt93a;pt65a
llc_sq_vcctx0	pb62a;pb57a;pb57b	pb49a;pb62b;pb30a;pb50b;pb58b;pb50a
lrc_sq_vcctx0	NONE	pb82a
ulc_sq_vcctx0	pt30a;pt48a	pt46b;pt52a;pt30b;pt48b
urc_sq_vcctx0	pr14b;pr12b;pt99b	pr29a;pr34a;pr14a;pr12a;pt99a
llc_sq_vcctx1	pb57a;pb57b;pb50a	pb62b;pb30a;pb50b;pb62a
lrc_sq_vcctx1	NONE	pb82a
ulc_sq_vcctx1	pt48a;pt52a	pt30a;pt48b
urc_sq_vcctx1	pr12b;pt99b	pr14b;pr14a;pr12a;pt99a
llc_sq_vcctx2	pb38b;pb38a	pb37b;pb37a;pb34b
lrc_sq_vcctx2	pb75b;pb73b	pb75a;pb73a
ulc_sq_vcctx2	pt56a;pt56b	pl9b;pt55b;pl12b;pl12a
urc_sq_vcctx2	pt100b;pt97b;pt95a	pt95b;pt98b;pt100a;pt94b
llc_sq_vcctx3	pb38b;pb38a;pb34b	pb37b;pb37a;pb34a
lrc_sq_vcctx3	pb75b;pb73b;pb73a	pb75a;pb76b;pb94b
ulc_sq_vcctx3	pt56a;pt56b;pl9b	pl9a;pt55b;pl12b;pl12a;pl14a
urc_sq_vcctx3	pt97b;pt95a;pt95b	pt100b;pt93b;pt98b;pt100a;pt94b;pt94a
vccpll	NONE	NONE
xres	pr9b;pr13b;pt98a;pr15a;pr15b	pt98b;pt100a;pr9a;pt97a;pr11a;pr13a;pr24a;pr24b