LatticeECP2/M Density Migration

August 2007 Technical Note TN1160

Introduction

Due to the programmable nature of FPGA devices, parts are chosen based on estimates of a system's design requirements. Choices of which FPGA to implement a design with revolve around:

- The cost of the device
- The amount of power the device uses
- The amount of physical space it will take on the completed circuit board
- How much logic the device can hold

Usually an estimate must be made on how much the device can hold vs. how much logic the design requires. This leads to either over-estimating or under-estimating how large the device needs to be. Even in cases where the right size device is chosen, it is possible for feature enhancements to push a design past the FPGA's capacity. It is therefore desirable to know what options exist with respect to putting larger or smaller devices onto a circuit board to cover these contingencies. The focus of this document, and supporting data files, is to describe how each LatticeECP2™ and LatticeECP2M™ device differs from the larger/smaller devices inside the same physical package. The data provided is useful for helping to design using LatticeECP2/M FPGAs in a way that mitigates the risks involved with under- or over-estimating device density requirements.

Migration Support Files

For easy density migration, different LatticeECP2/M devices are placed within footprint-compatible packages. For example, the LatticeECP2M has three different logic densities (6K, 12K and 20K LUTs) placed into the 256 fpBGA package.

Since different logic density devices may have slightly different capabilities, it is important to understand the differences in the way the pin resources of each device density are brought out for use.

Migration support files are provided to describe how to design in a way to permit migration between devices residing in the same package footprint. These files are text files describing how internal bond pads are connected to the pins of a given package. The files are all presented from the perspective of moving from a chip with a small number of LUTs toward a device with a larger number of LUTs (i.e., low density to high density). The comparisons for pin migration are based on the primary pin functionality. If the secondary functions (dual function) are used, the user should also compare the secondary functions in addition to the pin migration information presented in this document.

Each file can contain up to three discrete sections, or alternately indicate there are no changes. The three sections are:

- New pins
- Removed pins
- Pins with a change of function

New Pins Section

The New Pins section describes the addition of new input/output pins. The first column is the BGA pin name or the quad flat pack pin number. The first column is sorted alphanumerically in ascending order. The second column describes the function the pin performs. Information about what the pin does is found in the LatticeECP2/M Family Data Sheet.

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```
                          New Pins
-------------------------------------------------------------------
Pin Name                  Function
-------------------------------------------------------------------
AE25                      LRC_SQ_VCCIB0
AD23                      LRC_SQ_VCCIB1
...
```

Removed Pins Section

The Removed Pins section shows the input/output pins that are not present on the larger device. The list is sorted in an ascending alphanumeric order.

```
                          Removed Pins
-------------------------------------------------------------------
Pin Name
-------------------------------------------------------------------
AB21
AC20
AC21
```

Changed Function Section

It is possible for the larger device to have changed features of a pin that is bonded in the smaller device. This can either be a simple change of the internal bond location (i.e., PR2A changes to PR5A) or it can be a complete reassignment of a general I/O capability to a fixed function (i.e., PB41A changes to a SERDES data input pin, as shown in the example below).

```
                      Function Change
-------------------------------------------------------------------
Pin Name    Old Function              New Function
-------------------------------------------------------------------
AE14        PB41A                     LRC_SQ_HDINN3
AF14        PB47A                     LRC_SQ_HDINP3
AF15        PB47B                     LRC_SQ_HDINP2
```

No Changes

It is also possible that there are no changes between a smaller device and a larger device. In this event, the support file will have a single line reading:

```
“No changes between packages”
```

File Naming Convention

The support files for the LatticeECP2/M migration data are given in the following naming scheme. The filenames are designed to make it easy to find the migration information for each device.

```
Device Family         Die size transition          Package
ecp                   6_to_12                      tqfp144
ecp2m                 20_to_35                     fp484
```

The example above shows the major components of the filename. The filename `ecp2m-20_to_35_fp484.txt` indicates this file is for the LatticceECP2M family. The contents describe the I/O differences between the 20K LUT and 35K LUT devices. Finally, the 484 fpBGA device package type is described.

LatticeECP2M SERDES Migration

The LatticeECP2M family of devices, besides having a greater embedded memory density, provides a few members with high-speed serializer/deserializer (SERDES) hardware. The hardware converts general-purpose input/output logic into dedicated SERDES input/output logic. The shift in logic also affects the way supply voltages are distributed within the LatticeECP2M silicon die. Another change that can occur is for some GPIO to become dedicated microprocessor interface I/O. It is likely for a larger LatticeECP2M device to have fewer GPIO than a less dense device in the same device form factor.

The changes to the LatticeECP2M device caused by adding the SERDES blocks require the designer to be more diligent in designing a printed circuit board. Migrating between devices in the SERDES-capable LatticeECP2M family is done for two reasons:

- A larger/smaller amount of logic is being implemented
- An increase/decrease in the number of SERDES channels is desired

How the design is implemented depends on why the density change is occurring.

Logic Density Migration

A design that is changing due to a change in logic density is fairly straightforward. The design is implemented such that either no SERDES channel is being used, or only a common SERDES channel is being used.

No SERDES I/O

In the case where none of the SERDES logic is being used it is only necessary to provide a supply voltage to the SERDES hardware. The supply voltage used to power the LatticeECP2M core can be used to power the SERDES hardware. Independent supplies, or techniques for providing isolated supply voltages to the SERDES hardware are not required since any noise injected into the SERDES hardware will have no impact.

Single Common SERDES I/O

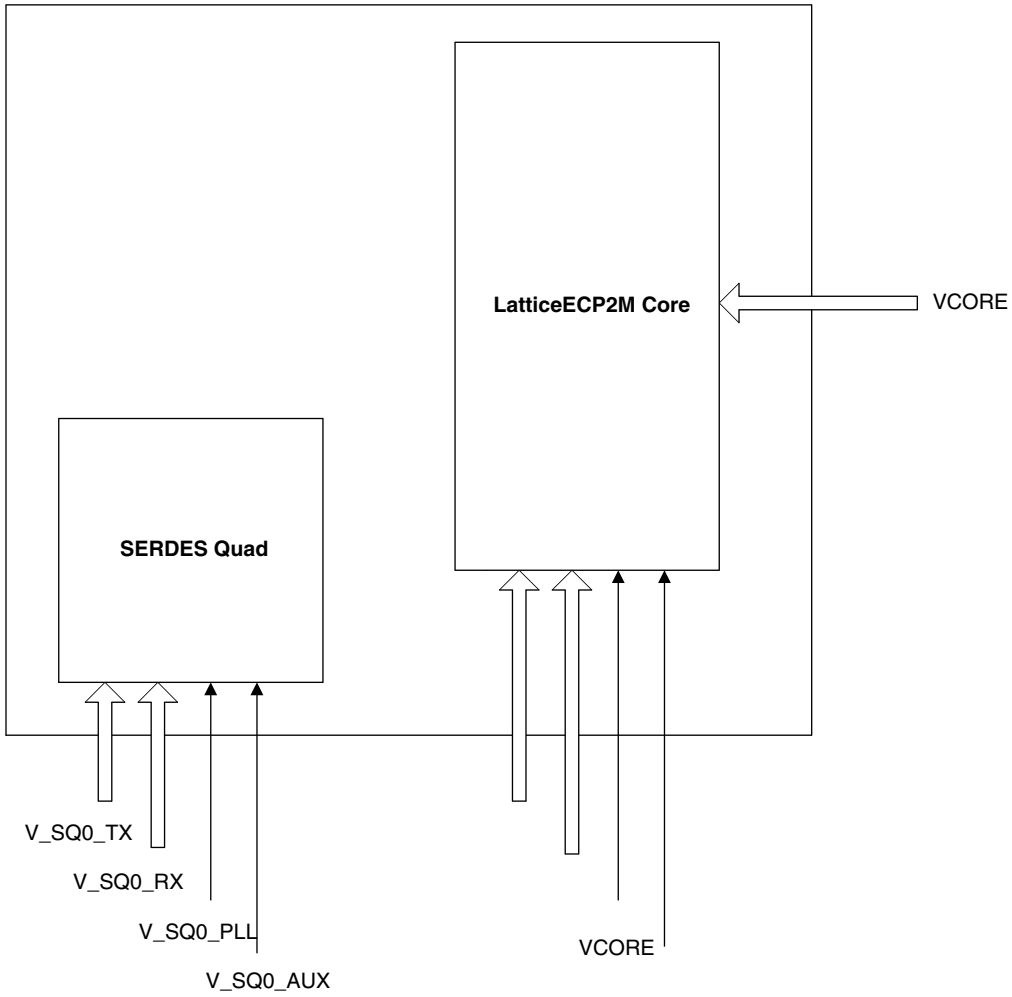
It is possible the design requires the use of a SERDES channel, but does not require use of additional SERDES channels. Migrating to a larger LatticeECP2M device may entail the undesirable addition of a second (or more) SERDES hardware blocks. In this case, it is important that the power supply for the common SERDES block continue to be properly isolated from the LatticeECP2M core voltage supply. The additional SERDES blocks still need to be powered, however. The power supply voltage for the LatticeECP2M core can be used to power the unused SERDES blocks without need for additional isolation/noise suppression.

Change in SERDES Channel Usage

The LatticeECP2M designer may be interested in developing a circuit board with the ability to be expanded, or to fill multiple roles. The design may use a single SERDES block in one incarnation, and two SERDES blocks in another. The functionality change can be accomplished by a change in the support logic assembled onto the board. Switching LatticeECP2M devices in this instance is more challenging.

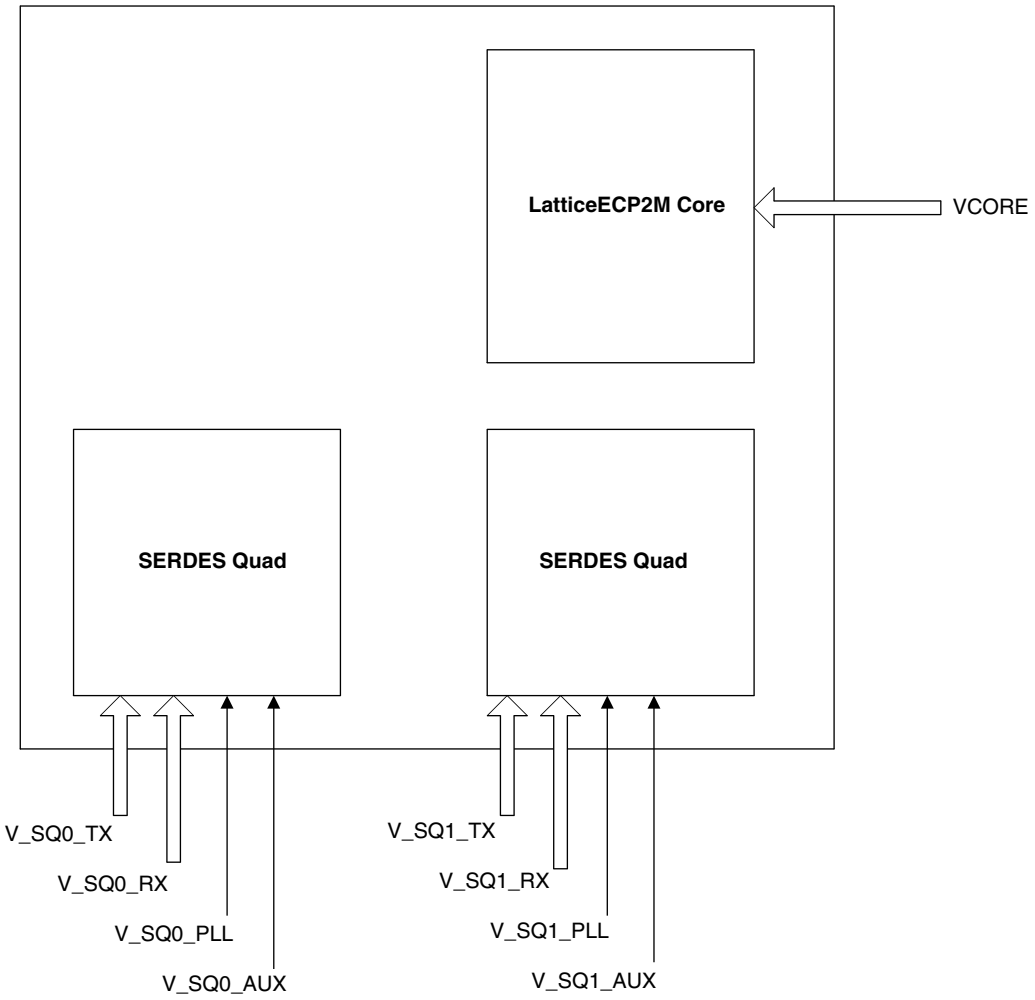
For example, when changing from an LatticeECP2M-35 to an LatticeECP2M-50 there is a net gain of one SERDES block. This means that some GPIO, and some VCC inputs change function. In particular, the VCC inputs change to SERDES VCC inputs. This means VCC landing pads on a board originally intended for the LatticeECP2M-35 must change connectivity for the LatticeECP2M-50.

Figure 1. LatticeECP2M-35 Core Power and SERDES Power



The SERDES quad in the LatticeECP2M-35 has power supply voltages isolated from the LatticeECP2M core logic supply. If a LatticeECP2M-50 is placed onto a circuit board originally designed for a LatticeECP2M-35, the new SERDES quad will be powered by the same supply voltage as the core logic. This is permissible as long as the new SERDES quad is not used. The new SERDES quad can be seen in Figure 2.

Figure 2. LatticeECP2M-50 Core Power and SERDES Power



As can be seen in the diagram above, the SERDES quads have independent supply inputs. The natural desire for a design implemented with the LatticeECP2M-50 is to connect the quiet and isolated SERDES power supply to both the SERDES quads. This is convenient from the point of view of creating an isolated and quiet supply plane for the circuit board. This technique is permissible as long as the LatticeECP2M-50 is the only device to reside on the PCB.

However, consider what will happen in the event a LatticeECP2M-35 is placed on the board. In that event, the isolated and quiet SERDES power supply will be short circuited to the LatticeECP2M core voltage inside the LatticeECP2M device. Thus, any noise in the LatticeECP2M core logic is translated into noise in the SERDES quad supply. This is detrimental to the performance of the SERDES PLL, and therefore detrimental to the performance of the SERDES quad as a whole.

Best design practices dictate any of the VCC inputs that have the possibility of being connected/disconnected to/from a SERDES quad be designed in such a way that they can be isolated from the other SERDES quads, and from the LatticeECP2M core supply.

Conclusion

The LatticeECP2/M device families are designed for density migration within each device family and footprint compatible package. The LatticeECP2 family provides a straightforward migration path. The LatticeECP2M, due to the addition of the high-speed SERDES function, requires the design engineer to carefully account for the changes

between device densities. This is especially true when the number of SERDES channels changes between migration options. It is, therefore, important for a designer who plans on using the LatticeECP2M in different device densities to carefully account for all discrepancies that may affect successful implementation of the design. The information provided with this technical note should help identify the differences between the different device densities.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2007	01.0	Initial release.