LatticeSC/M Broadcom® 2.5 GbE Physical Layer Interoperability Over CX-4

August 2007 Technical Note TN1156

Introduction

This technical note describes a 1000BASE-X physical layer Gigabit Ethernet interoperability test between a LatticeSC/M device and the Broadcom BCM56580 network switch. The test was limited to the physical layer (up to GMII) of the Gigabit Ethernet protocol stack.

Specifically, the document discusses the following topics:

- Overview of LatticeSC™ and LatticeSCM™ devices and Broadcom BCM56580 network switch
- 1000BASE-X physical layer interoperability setup and results

Two significant aspects of the interoperability test need to be highlighted:

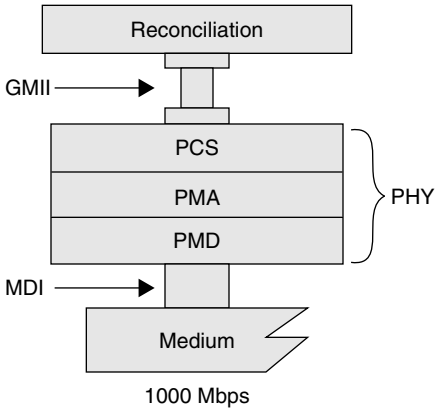
- The BCM56580 uses a CX-4 HiGig™ port, whereas the LatticeSC Communications Platform Evaluation Board provides an SMA connector. A CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards. The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels (10 Gbps bandwidth total), but only one SMA channel (channel 0) was connected to the LatticeSC side.
- The 1000BASE-X physical layer interoperability ran at a 2.5-Gbps data rate (3.125-Gbps aggregated rate). Both Lattice and Broadcom support this rate by running a faster speed reference clock that extends the bandwidth capability of 1-Gigabit Ethernet.

Gigabit Ethernet Physical Layer

The IEEE 802.3-2002 Gigabit Ethernet standard is organized along architectural lines, emphasizing the large-scale separation of the system into two parts: the Media Access Control (MAC) sublayer of the Data Link Layer and the Physical Layer.

Figure 1 highlights the sub-layers that constitute the Gigabit Ethernet Physical Layer.

Figure 1. Gigabit Ethernet Physical Layer



According to the 802.3-2002 standard, two important compatibility interfaces are defined within what is architecturally the Physical Layer:

- **Medium Dependent Interfaces (MDI)**. To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in Clause 8 (and beyond) in the IEEE 802.3-2002 standard, and to the procedures that define correct behavior of a station. Local Area Network requires complete compatibility at the Physical Medium interface (that is, the physical cable interface). In the LatticeSC/M and Broadcom interoperability, the physical medium is a CX-4 to SMA conversion board.
- **Gigabit Media Independent Interface (GMII).** The GMII is designed to connect a gigabit-capable MAC or repeater unit to a gigabit PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended because it allows maximum flexibility in intermixing PHYs and DTEs at gigabit speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.

The 1000BASE-X Gigabit Ethernet standard specifies a 1-Gbps data rate (1.25-Gbps aggregated rate). Some Ethernet switch devices offer a 2.5 Gbps (3.125 Gbps aggregated) option for switched applications based on the 1000BASE-X standard. This applies to the LatticeSC/M device and the Broadcom BCM56580 network switch.

Also, the LatticeSC/M and BCM56580 interoperability exercises the whole physical layer, including GMII.

LatticeSC/M and flexiPCS Overview

LatticeSC/M Features

The LatticeSC/M family, equipped with ASIC-based system level building blocks, was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII, and CSIX. Furthermore, the devices in this family feature clock multiply, divide, and phase shift PLLs, numerous DLLs and dynamic glitch-free clock MUX that are required in today's high-end system designs.

All LatticeSC/M devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic called flexiPCS. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES.

flexiPCS Gigabit Ethernet Features

The Gigabit Ethernet mode of the flexiPCS (flexible Physical Coding Sublayer) block supports full 1000BASE-X compatibility, from the Serial I/O to the GMII interface of the IEEE 802.3-2002 Gigabit Ethernet standard. The flexiPCS also supports a 2.5-Gbps data rate (3.125-Gbps aggregated rate) by running a faster speed reference clock that extends the bandwidth capability of 1-Gigabit Ethernet.

The LatticeSC/M flexiPCS in Gigabit Ethernet mode supports the following operations:

Transmit Path (from LatticeSC/M device to line):

- Cyclic Redundancy Check (CRC) generation and insertion into Gigabit Ethernet frame
- Transmit State Machine, which performs 8-bit data encapsulation and formatting, including the auto-negotiation code word insertion and outputting the correct 8-bit code/data word and k control characters according to the IEEE 802.3-2002 specification
- 8b/10b Encoding.

Receive Path (from line to LatticeSC/M device):

- Word alignment based on IEEE 802.3-2002 defined alignment characters
- 8b/10b decoding

- Link State Machine functions compliant with the IEEE 802.3-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine including Auto-Negotiation support compliant with the IEEE 802.3-2002 specification
- Cyclic Redundancy Code (CRC) checking

Broadcom BCM56580 Overview

BCM56580 Features

The BCM56580 network switch is a high-density 2.5-Gigabit Ethernet switching chip solution with 16 ports, plus four dedicated 10-GbE/HiGig stacking/uplink ports. Additionally, the BCM56580 integrates all the SERDES required to interface to applicable copper and fiber physical interfaces. The integrated SERDES functionality includes 2.5 Gbps SERDES interfaces and 1 Gbps SERDES PHY interfaces. The integrated SERDES complies with the CX-4 and PICMG3.1 standards, which ensure interoperability with Ethernet line cards in an advanced TCA chassis.

BCM56580 10-GbE/HiGig Ports

The BCM56580 has four dedicated 10-GbE/HiGig stacking/uplink ports. Each of these ports supports 10-GbE, 2.5-GbE, or 1-GbE.

A HiGig port interface includes an integrated 4-channel SERDES at 3.125 Gbps.

In 10 Gbps modes (e.g., XAUI), each HiGig port transmits and receives data on all four channels at 3.125 Gbps.

When configured in 2.5-Gigabit Ethernet, only channel 0 of a HiGig port is used.

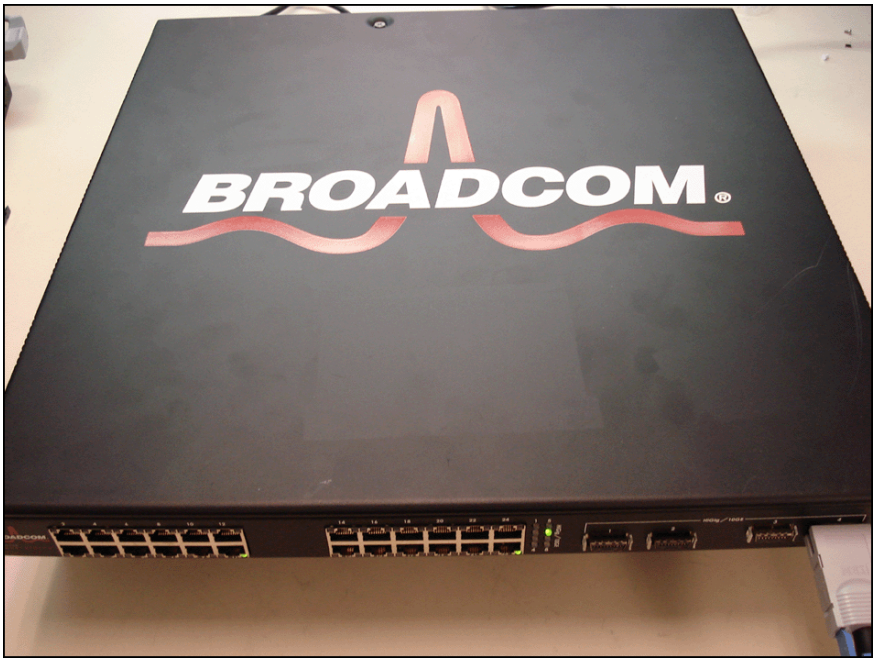
Test Equipment

Below is the equipment used in the interoperability tests:

Broadcom BCM56580 Network Switch

Figure 2 shows the BCM56580 network switch.

Figure 2. Broadcom BCM56580 Network Switch



One can configure the Broadcom ports by connecting its serial port to a PC and starting a HyperTerminal session. Figure 2 shows a serial cable connected to the serial port at the back of the BCM56580.

Figure 2 also shows a CX-4 connector inserted into one of the four 10 GbE/HiGig ports available on the front right side of the BCM56580.

This port, referred to as xe0 (the other ports are xe1, xe2, and xe3), was selected for the interoperation with the LatticeSC/M device. It was configured in 2.5-Gigabit Ethernet mode. In this mode, only channel 0 of the port was used.

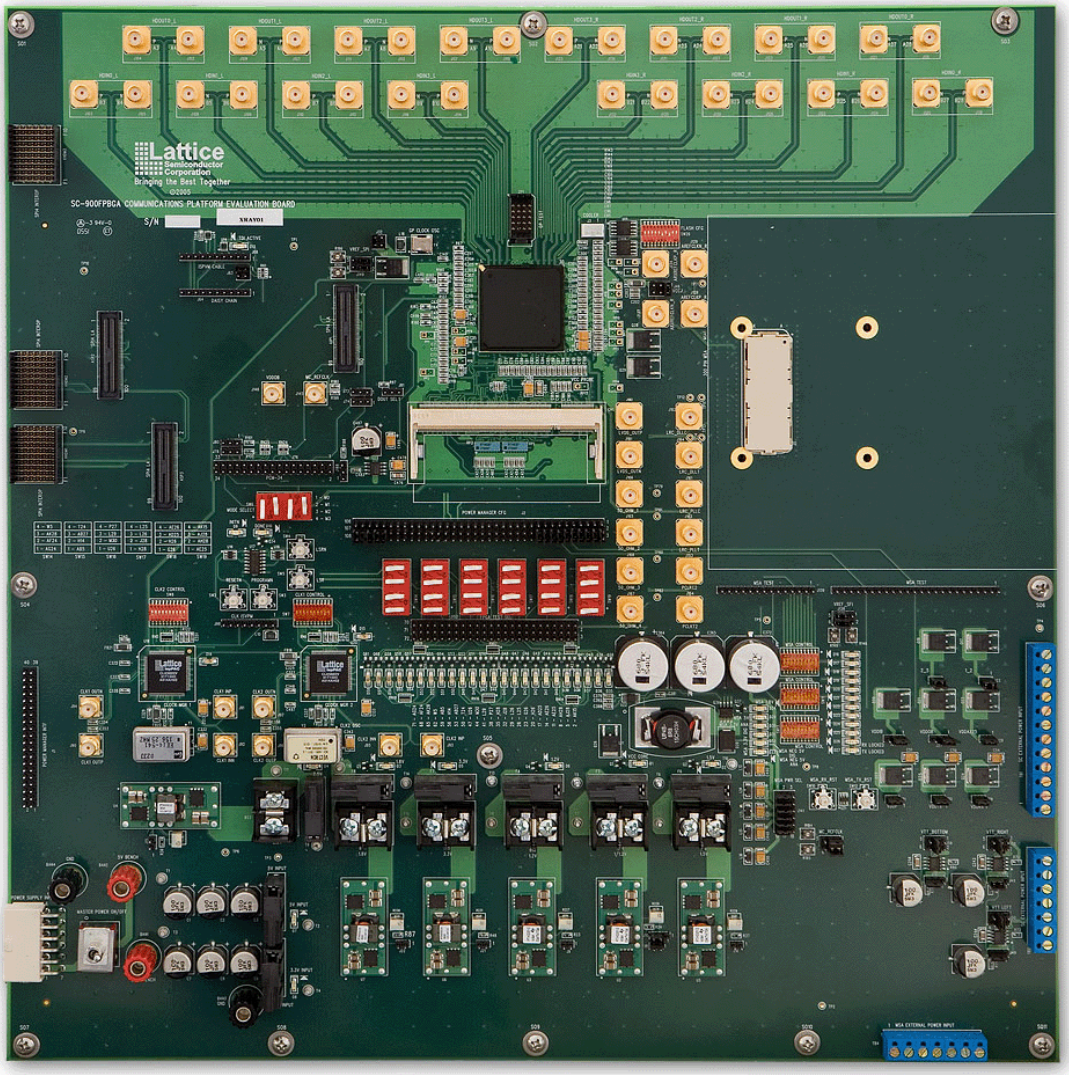
LatticeSC Communications Platform Evaluation Board

The LatticeSC Communications Platform Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC/M FPGA or aid in the development of custom designs. Each LatticeSC Communications Platform Evaluation Board contains, among others:

- LFSC3GA25E-6F900C FPGA device
- SMA test points for high-speed SERDES and Clock I/O
- Onboard power connections and power sources
- Onboard interchangeable clock oscillator
- Onboard reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- Onboard Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 3 shows the LatticeSC Communications Platform Evaluation Board.

Figure 3. LatticeSC Communications Platform Evaluation Board



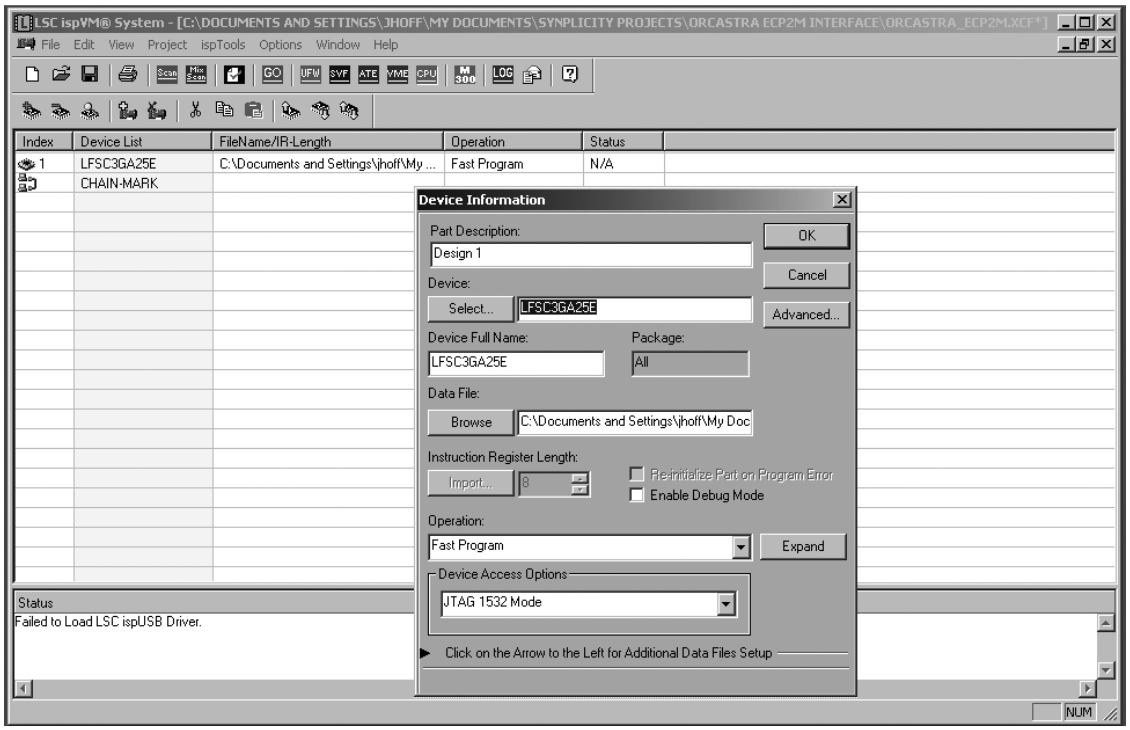
ispVM System

The ispVM® System is included with Lattice's ispLEVER® software and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice Semiconductor and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM system is used in this interoperability test to download the LatticeSC/M bitstream, which configures the flexiPCS in 1-Gigabit Ethernet mode.

Figure 4 shows a screen shot of the ispVM system.

Figure 4. ispVM System



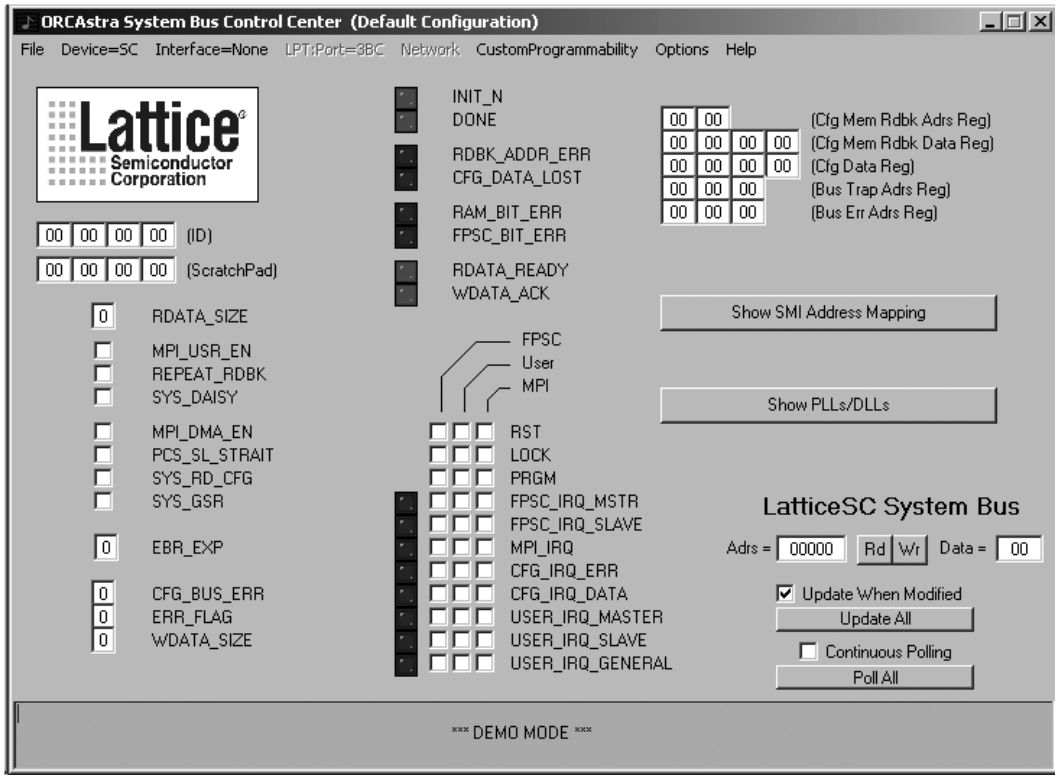
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy recompile process or making changes to their board.

Configurations created in the GUI can be saved to memory and reloaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeSC/M.

Figure 5 is a screen shot of ORCAstra System.

Figure 5. ORCAstra System



Interoperability Testing

This section provides details on the 1000BASE-X 2.5-Gigabit Ethernet Physical Layer interoperability between a LatticeSC/M device and the Broadcom BCM56580 network switch. This interoperability tests the correct processing of 2.5 Gigabit Ethernet data from the BCM56580 network switch to the LatticeSC/M flexiPCS GMII interface and then back in the other direction. Particularly, the test verifies the ability to transfer packets across the system in an asynchronous way.

Test Setup

Figure 6 shows the LatticeSC Communications Platform Evaluation Board and Broadcom Board connections.

Figure 7 is a block diagram of the test setup.

The setup includes:

- The Broadcom BCM56580 network switch
- The LatticeSC Communications Platform Evaluation Board
  - In 2.5 Gigabit Ethernet, the LatticeSC Communications Platform Evaluation Board uses an on-board 156.25-MHz differential oscillator to provide the reference clock to the LatticeSC/M flexiPCS. The flexiPCS multiplies the reference clock by 20 to achieve a 3.125-Gbps aggregated rate.
- A PC for software control/monitoring
- A CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards (see Figure 6). The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels or 16 SMA connectors for a total bandwidth of 10 Gbps (12.5-Gbps aggregated rate). However, for 2.5 Gigabit Ethernet, only one differential TX/RX channel (channel 0 with 4 SMA connectors) was connected to the

LatticeSC side (as shown in Figure 6).

- Cables
  - SMA for LatticeSC/M flexiPCS channel 0
  - SMA for Agilent clock generator
  - CX-4 for BCM56580 HiGig port xe0
  - ispVM JTAG cable for downloading LatticeSC bitstream and ORCAstra GUI access
  - Serial Cable for BCM56580 HyperTerminal access

Figure 6. Board Connections

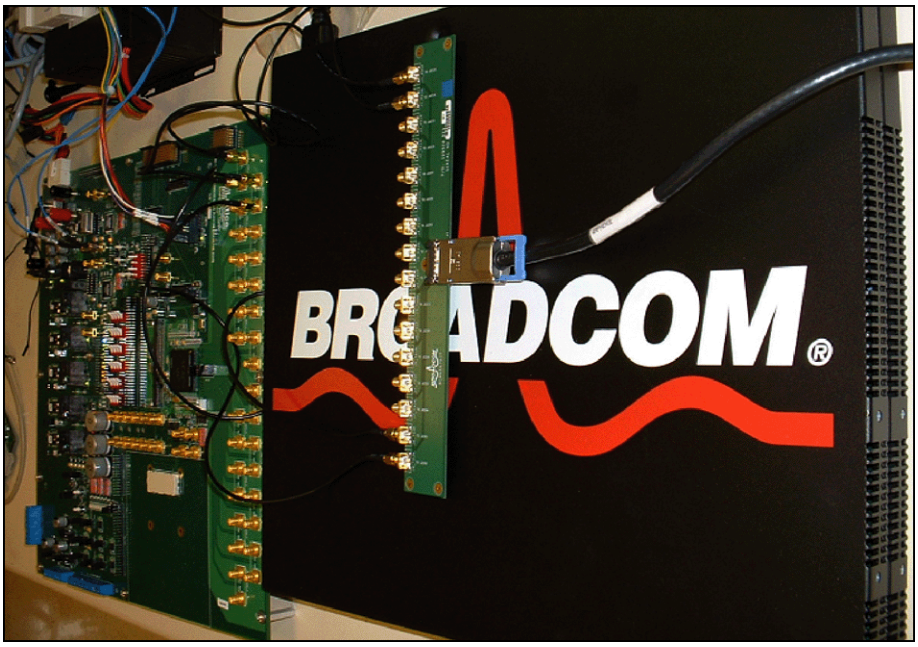
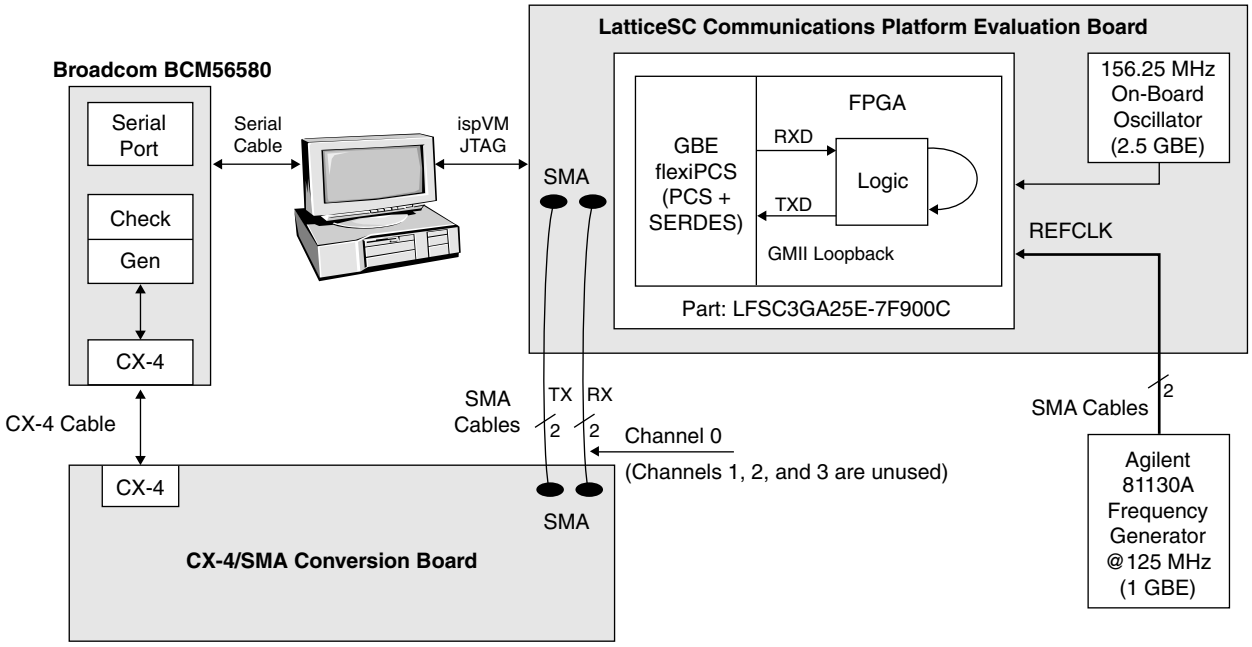


Figure 7. Test Setup Block Diagram



Test Description

This section describes how each interoperability partner is set up for Gigabit Ethernet physical layer interoperability.

BCM56580

The BCM56580 switch generates and checks full protocol compliant Gigabit Ethernet packets. The BCM56580 is configured in 2.5-Gigabit Ethernet.

Figure 8 illustrates the sequence of events performed in a HyperTerminal from start-up to configure HiGig port 0 (xe0) of BCM56580 in 2.5-Gigabit Ethernet, while disabling auto-negotiation. This means that only one channel (channel 0) on this port is used.

Figure 8. Configuring BCM56580 Port 0 in 2.5 Gigabit Ethernet

```
BCM.0>  pw start
BCM.0> port xe0 speed=2500 an=off
BCM.0> ps
        ena/  speed/  link    auto    STP        lrn  inter   max  loop
port  link  duplex  scan  neg?   state    pause  discrd  ops   face frame  back
 xe0  up   2.5G FD    SW   No   Forward          None    FA  XGMII 16360

BCM.0> tx 100000000 pbm=xe0 len=200 sm=   00:00:00:00:00:01 dm=00:00:00:00:00:02
.
.
BCM.0> show counters
RUC.xe0          :           100,000,000        +100,000,000
RDBGC0.xe0       :            99,997,820         +99,997,820
GR255.xe0        :           100,000,000        +100,000,000
GRPKT.xe0        :           100,000,000        +100,000,000
GRBYT.xe0        :        20,000,000,000     +20,000,000,000
GT255.xe0        :           100,000,000        +100,000,000
GTPKT.xe0        :           100,000,000        +100,000,000
GTBYT.xe0        :        20,000,000,000     +20,000,000,000
BCM.0>
```

LatticeSC Communications Platform Evaluation Board

The on-board 156.25-MHz clock oscillator sources the LatticeSC/M PCS reference clock for 2.5-Gigabit Ethernet. The flexiPCS multiplies the reference clock by 20 to achieve a 2.5-Gbps data rate (3.125-Gbps aggregated rate).

In the RX direction, The LatticeSC/M SERDES recovers the 1000BASE-X packets from the BCM56580 device, and the flexiPCS converts them into GMII format.

The GMII loopback logic in the FPGA portion loops the GMII data back into the TX direction. The LatticeSC/M device then transmits the 1000BASE-X packets back to the BCM56580 device.

Results

As shown in Figure 8, the HiGig port 0 (xe0) of BCM56580 was configured for 2.5-Gigabit Ethernet.

The HyperTerminal “tx” command generated 100 million 200-byte Ethernet packets from the BCM56580 to the LatticeSC Communications Platform Evaluation Board.

The “show counter” command was then used to monitor the status of BCM56580 TX and RX packet (GTPKT.xe0 and GRPKT.xe0) and byte (GTBYT.xe0 and GRBYT.xe0) counters. Figure 8 does not show any error counters. This is an indication that the error counters have remained at a zero value during the test. Additionally, the Lattice ORCAstra System GUI (shown in Figure 5) was monitored for proper flexiPCS Gigabit Ethernet link state machine synchronization.

The results showed that all 100 million Ethernet packets (20 billion bytes) were successfully transmitted to the LatticeSC/M and recovered at the BCM56580 error-free.

Summary

In conclusion, the LatticeSC/M FPGA family offers users built-in 1000BASE-X 2.5 Gigabit Ethernet Physical Layer support and is fully interoperable with Broadcom BCM56580 network switch.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.