

Introduction

This technical note describes a physical layer 10-Gigabit Ethernet and HiGig (10 Gbps) interoperability test between a LatticeSC/M device and the Broadcom BCM56800 network switch. The test was limited to the physical layer (up to XGMII) of the 10-Gigabit Ethernet protocol stack.

Specifically, the document discusses the following topics:

- Overview of LatticeSC™ and LatticeSCM™ devices and Broadcom BCM56800 network switch
- Physical layer interoperability setup and results

Two significant aspects of the interoperability test need to be highlighted:

- The BCM56800 uses a CX-4 HiGig port, whereas the LatticeSC Communications Platform Evaluation Board provides an SMA connector. A CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards. The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels (10 Gbps bandwidth total). All four SMA channels (Quad 360) were connected to the LatticeSC side.
- The physical layer interoperability ran at a 10-Gbps data rate (12.5-Gbps aggregated rate).

XAUI Interoperability

XAUI is a high-speed interconnect that offers reduced pin count and the ability to drive up to 20" of PCB trace on standard FR-4 material. In order to connect a 10-Gigabit Ethernet MAC to an off-chip PHY device, an XGMII interface is used. The XGMII is a low-speed parallel interface for short range (approximately 2") interconnects.

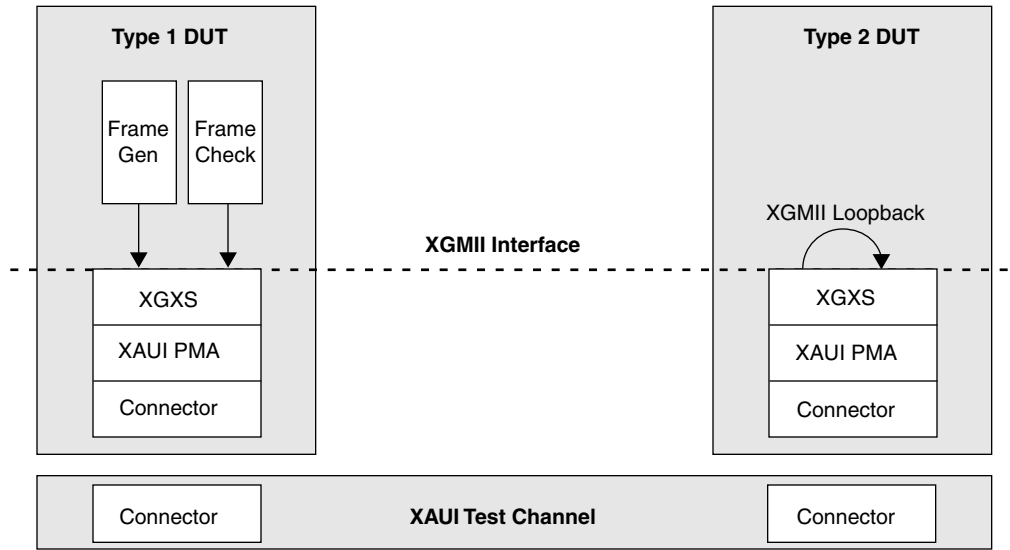
XAUI interoperability is based on the 10-Gigabit Ethernet standard (IEEE Standard 802.3ae-2002). Two XAUI link partners can be directly plugged into a XAUI backplane. Both boards are capable of generating and checking packets.

The board that sources packets is capable of keeping a detailed count of the number of packets transmitted while the sink board is capable of keeping detailed statistics on the number of packets received and errors associated with the packets. The XAUI backplane is also called the XAUI test channel. A typical test setup is shown in Figure 1.

Each reference station must be a line card that is directly plugged into the XAUI test channel. Both DUTs are required to have their own clock domain. Synchronous clocking (distributing a single clock to the two DUTs) is not allowed. Local management indicators on the DUT (reference stations) that provide information on link level errors, such as CRC errors, are also needed. A DUT is called a Type #1 device if it is capable of transmitting and checking packets.

A DUT is called a Type #2a device if it receives packets and does a RX to TX loopback through XGMII and sends the packets back to the transmitting station, which is a Type #1 device. The Type #1 device then checks the received packets for errors. Figure 1 shows a setup where one DUT is of Type #1 and the other is of Type #2a.

The LatticeSC/M and BCM56800 interoperability exercises the whole physical layer, including XGMII.

Figure 1. Typical XAUI Interoperability Test Setup

HiGig Protocol

The HiGig Protocol, as defined by Broadcom, provides a standard mechanism for interconnecting switches for a single system defining an efficient way to forward frames for Unicast, Broadcast, Multicast (Layer 2 and IP), and Control Traffic. The HiGig Protocol implements HiGig frames, which are formed by tagging standard Ethernet frames with a 12-byte HiGig header.

LatticeSC/M and flexiPCS Overview

LatticeSC/M Features

The LatticeSC/M family, equipped with ASIC-based system level building blocks, was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, Hyper-Transport, SPI4.2, SFI-4, UTOPIA, XGMII, and CSIX. Furthermore, the devices in this family feature clock multiply, divide, and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUX that are required in today's high-end system designs.

All LatticeSC/M devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic called flexiPCS™. The flexiPCS logic can be configured to support numerous industry-standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES.

LatticeSC flexiPCS in XAUI Mode

The XAUI mode of the flexiPCS (Physical Coding Sublayer) block supports full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard. XAUI Mode supports 10-Gigabit Ethernet as well as 10-Gigabit Fibre Channel applications.

Transmit Path Functionality (From LatticeSC Device to Line)

- Transmit State Machine that performs translation of XGMII idles to proper IIAII, IIKII, IIRII characters according to the IEEE 802.3ae-2002 specification
- 8b10b encoding

Receive Path Functionality (from Line to LatticeSC Device):

- Word alignment based on IEEE 802.3-2002 defined alignment characters
- 8b10b decoding
- Link State Machine functions incorporating operations defined in PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine compliant with the IEEE 802.3ae-2002 specification

Broadcom BCM56800 Overview**BCM56800 Features**

The BCM56800 network switch is a high-density, 10-Gigabit Ethernet switching chip solution with 20 ports. Each of these flexible ports supports 10-Gigabit Ethernet or 1-Gigabit Ethernet. Additionally, the BCM56800 integrates all the SERDES required to interface to applicable copper and fiber physical interfaces. The integrated SERDES functionality includes 10 Gbps XAUI interfaces and 1 Gbps SGMII PHY interfaces. The integrated SERDES complies with the CX-4 standard and PICMG3.1 standard, which ensures interoperability with Ethernet line cards in an Advanced TCA chassis.

BCM56800 10 GbE/HiGig Ports

The BCM56800 has 20 10-GbE/1-GbE ports. The BCM56800 is based on StrataXGS® field-proven, robust architecture. It has integrated high-performance SERDES – integrated XAUI SERDES for all 20 10-GbE ports, and it uses single SERDES lane per port at GbE speeds. The device supports 200 Gbps switching capacity at line rate.

Test Equipment

Below is the equipment used in the interoperability tests.

Broadcom BCM56800 Network Switch

Figure 2 shows the BCM56800 network switch.

Figure 2. Broadcom BCM56800 Network Switch



One can configure the Broadcom ports by connecting its serial port to a PC and starting a HyperTerminal session. Figure 2 shows a serial cable connected to the serial port at the back of the BCM56800.

Figure 2 also shows a CX-4 connector inserted into one 10 GbE/HiGig port available on the front right side of the BCM56800.

This port, referred to as xe0/hg0, was selected for the interoperation with the LatticeSC/M device. It was configured in XAUI and HiGig modes.

Agilent 81130A Pulse/Data Generator

The Agilent 81130A pulse/data generator was used to supply an external 156.25-MHz reference clock source to the LatticeSC/M flexiPCS.

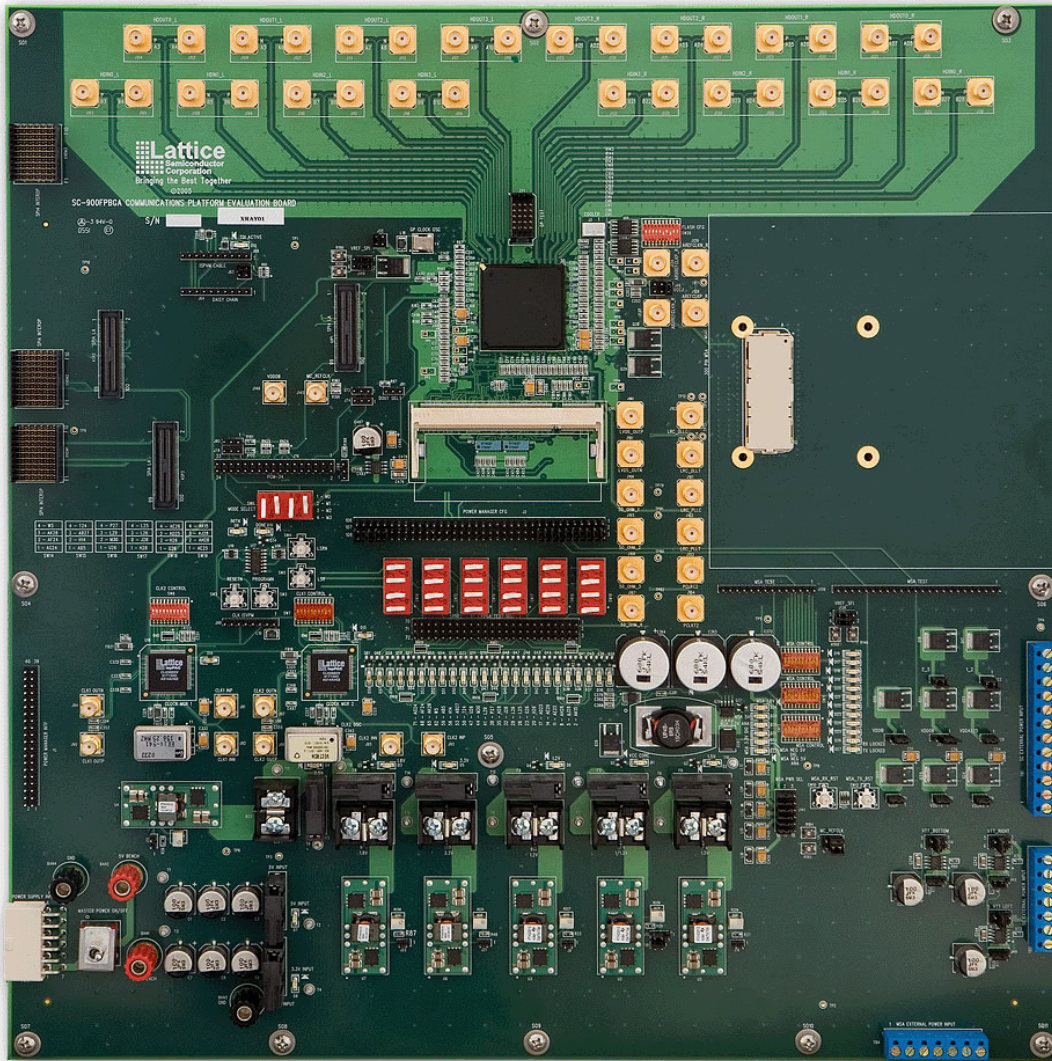
For more information on this module, refer to Agilent's website: www.agilent.com.

LatticeSC Communications Platform Evaluation Board

The LatticeSC Communications Platform Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC/M FPGA or aid in the development of custom designs. Each LatticeSC Communications Platform Evaluation Board contains, among others:

- LFSC3GA25E-6F900C FPGA device
- SMA test points for high-speed SERDES and Clock I/O
- Onboard power connections and power sources
- Onboard interchangeable clock oscillator
- Onboard reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- Onboard Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 3 shows the LatticeSC Communications Platform Evaluation Board.

Figure 3. LatticeSC Communications Platform Evaluation Board

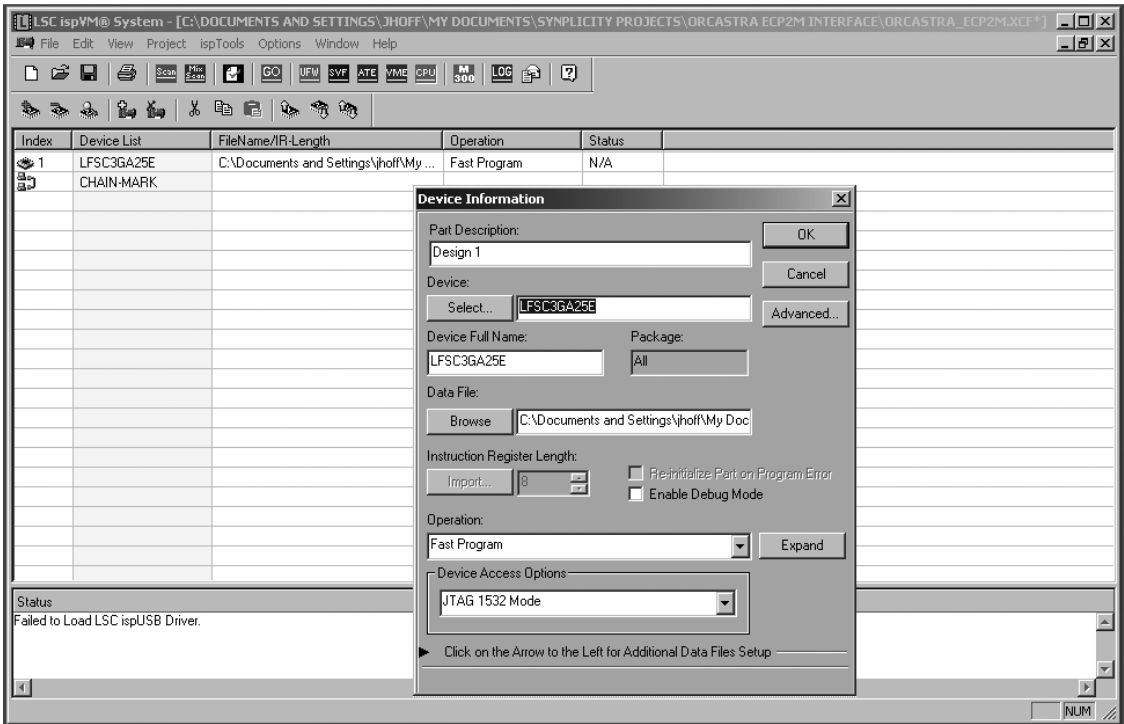
ispVM System

The ispVM[®] System is included with Lattice's ispLEVER[®] software and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP devices using JEDEC and Bitstream files generated by Lattice Semiconductor and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE[™], ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM system is used in this interoperability test to download the LatticeSC/M bitstream, which configures the flexiPCS in 10-Gigabit Ethernet mode (XAUI).

Figure 4 shows a screen shot of the ispVM system.

Figure 4. ispVM System



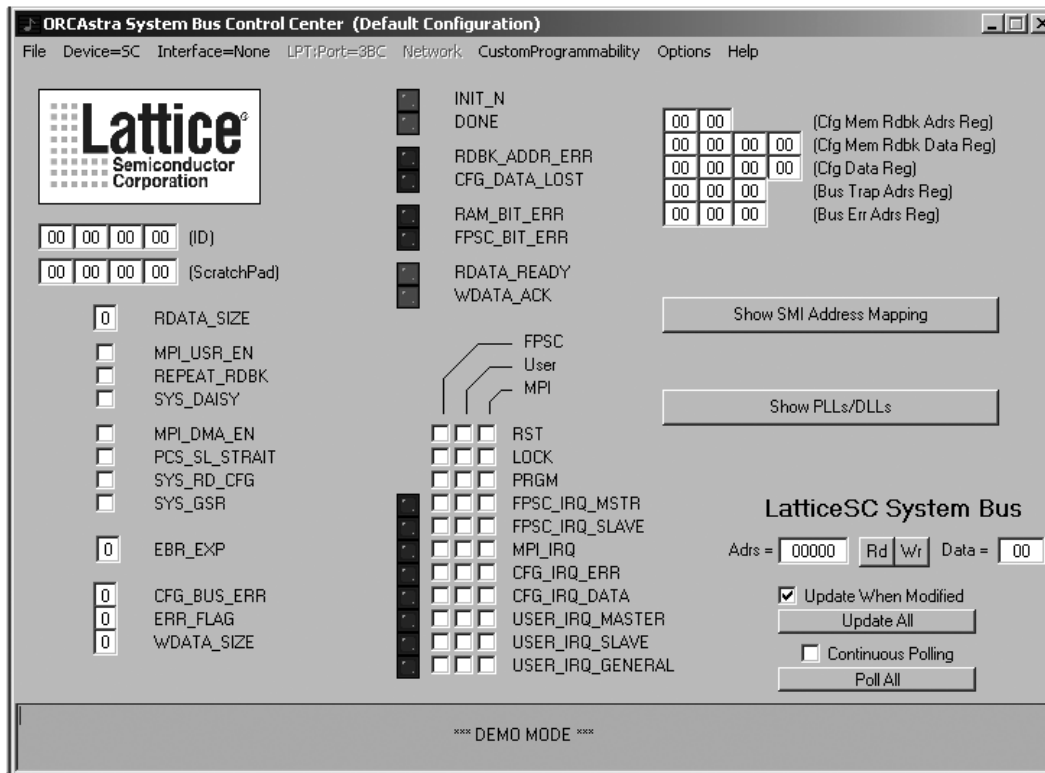
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy recompile process or making changes to their board.

Configurations created in the GUI can be saved to memory and reloaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeSC/M.

Figure 5 is a screen shot of ORCAstra system

Figure 5. ORCAstra System



Interoperability Testing

This section provides details on the 10-Gigabit Ethernet./HiGig (10 Gbps) Physical Layer interoperability between a LatticeSC/M device and the Broadcom BCM56800 network switch. This interoperability tests the correct processing of XAUI/HiGig (10 Gbps) data from the BCM56800 network switch to the LatticeSC/M flexiPCS XGMII interface and then back in the other direction. Particularly, the test verifies the ability to transfer packets across the system in an asynchronous way.

Test Setup

Figure 6 shows the LatticeSC/M and Broadcom boards connections.

Figure 7 is a block diagram of the test setup.

The setup includes:

- The Broadcom BCM56800 network switch
- The LatticeSC Communications Platform Evaluation Board. In 10-Gigabit Ethernet, the Agilent 811130A Data/Pulse Generator provides an external 156.25-MHz reference clock to the LatticeSC/M flexiPCS. The flexiPCS multiplies the reference clock by 20 to achieve a 12.5-Gbps aggregated rate (10 Gbps data rate). Note that an on-board 156.25-MHz differential oscillator can also be used to provide a reference clock to the LatticeSC/M flexiPCS SERDES.
- A PC for software control/monitoring
- A CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards (see Figure 6). The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels, or 16 SMA connectors for a total bandwidth of 10 Gbps (12.5-Gbps aggregated rate). All four differen-

tial TX/RX channels were connected to the LatticeSC side (as shown in Figure 6).

- Cables
 - 16 SMA for LatticeSC/M flexiPCS channels 0 through 4
 - Two SMAs for Agilent clock generator
 - CX-4 for BCM56800 HiGig port xe0/hg0
 - ispVM JTAG cable for downloading LatticeSC bitstream and ORCAstra GUI access
 - Serial cable for BCM56800 HyperTerminal access

Figure 6. Board Connections

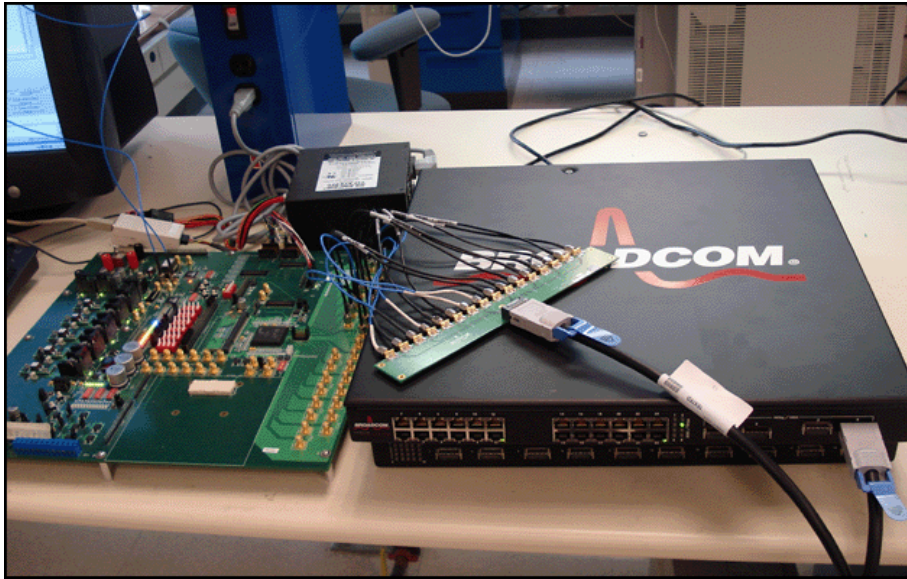
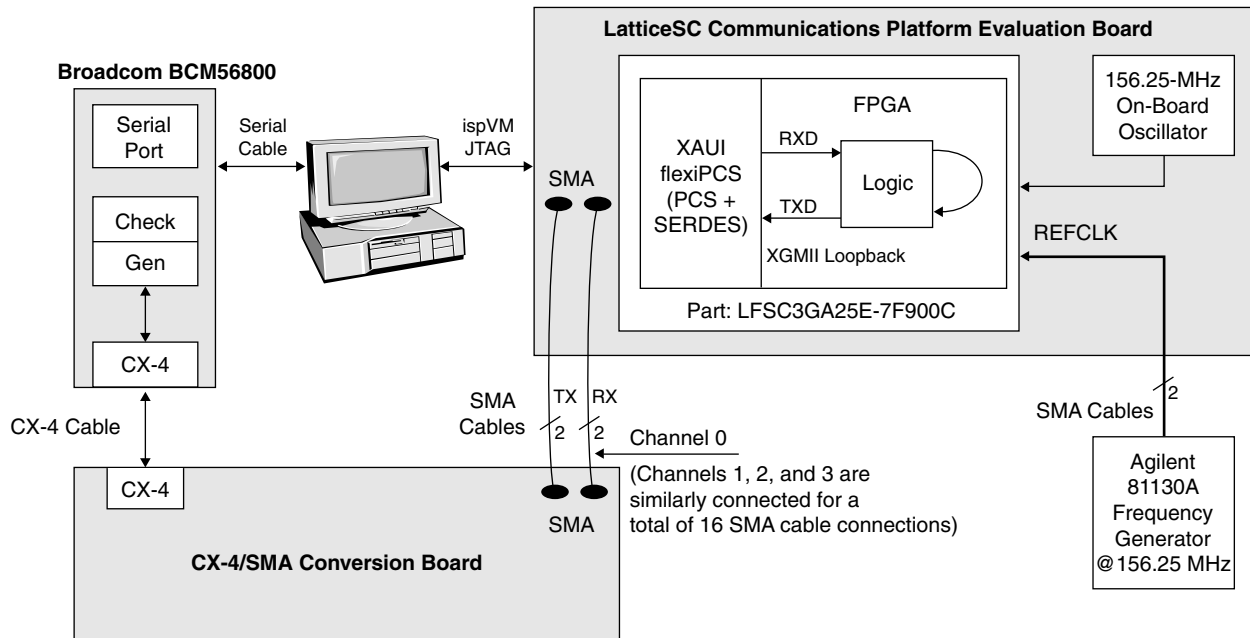


Figure 7. Test Setup Block Diagram



Test Description

This section describes how each interoperability partner is set up for 10-Gigabit Ethernet physical layer interoperability.

BCM56800

The BCM56800 switch generates and checks full protocol-compliant 10-Gigabit Ethernet or HiGig (10 Gbps) packets. The BCM56800 is configured in either XAUI or HiGig mode.

Figure 8 illustrates the sequence of events performed in a HyperTerminal from start-up to configure HiGig port 0 (xe0) of BCM56800 in XAUI mode.

Figure 9 illustrates the sequence of events performed in a HyperTerminal from startup to configure HiGig port 0 (hg0) of BCM56800 in HiGig (10 Gbps) mode.

Figure 8. Configuring BCM56800 Port 0 in XAUI

```

BCM.0> conf add pbmp_xport_hg=00000000
BCM.0> conf add pbmp_xport_xe=0xffffffff
BCM.0> conf save
BCM.0> rc
rc: unit 0 device BCM56800_A0
BCM.0> ps
      ena/  speed/  link  auto    STP          lrn  inter  max  loop
port link duplex scan neg?  state  pause  discrd ops  face frame back
xe0  up   10G FD   SW   Yes  Forward          None   FA  XGMII 16360

BCM.0> tx 140261441 pbm=xe0 len=9000 sm=0    0:00:00:00:00:01 dm=00:00:00:00:00:02
BCM.0> show counters
RUC.xe0      :          140,261,441          +140,261,441
RDBGCO.xe0   :          140,261,441          +140,261,441
ITPKT.xe0    :          140,261,441          +140,261,441
ITOVR.xe0    :          140,261,441          +140,261,441
IT9216.xe0   :          140,261,441          +140,261,441
ITBYT.xe0    :      1,262,352,969,000  +1,262,352,969,000
IR9216.xe0   :          140,261,441          +140,261,441
IRPKT.xe0    :          140,261,441          +140,261,441
IROVR.xe0    :          140,261,441          +140,261,441
IRBYT.xe0    :      1,262,352,969,000  +1,262,352,969,000
BCM.0>

```

Figure 9. Configuring BCM56800 Port 0 in HiGig (10 Gbps)

```

BCM.0> conf add pbmp_xport_hg=0000001
BCM.0> conf add pbmp_xport_xe=0xfffffE
BCM.0> conf save
BCM.0> rc
rc: unit 0 device BCM56800_A0
BCM.0> ps
      ena/  speed/  link  auto    STP          lrn  inter  max  loop
port link duplex scan neg?  state pause discrd ops  face frame back
hg0  up   10G FD   SW   Yes Forward          None  FA  XGMII 16360

BCM.0> tx 10000000 pbm=hg0 len=9000 sm= 00:00:00:00:00:01 dm=00:00:00:00:00:02
BCM.0> show counters
RUC.hg0      :          10,000,000          +10,000,000
RDBG0.hg0    :          10,000,000          +10,000,000
ICTRL.hg0    :          10,000,000          +10,000,000
ITPKT.hg0    :          10,000,000          +10,000,000
ITOVR.hg0    :          10,000,000          +10,000,000
IT9216.hg0   :          10,000,000          +10,000,000
ITBYT.hg0    :          90,080,000,000      +90,080,000,000
IR9216.hg0   :          10,000,000          +10,000,000
IRPKT.hg0    :          10,000,000          +10,000,000
IROVR.hg0    :          10,000,000          +10,000,000
IRBYT.hg0    :          90,080,000,000      +90,080,000,000
BCM.0>

```

LatticeSC Communications Platform Evaluation Board

The on-board 156.25-MHz clock oscillator sources the LatticeSC/M PCS reference clock for XAUI. The flexiPCS multiplies the reference clock by 20 to achieve a 10-Gbps data rate (12.5-Gbps aggregated rate).

In the RX direction, The LatticeSC/M SERDES recovers the packets from the BCM56800 device and the flexiPCS converts them into XGMII format.

The XGMII loopback logic in the FPGA portion loops the XGMII data back into the TX direction. The LatticeSC/M device then transmits the packets back to the BCM56800 device.

XAUI Results

As shown in Figure 8, HiGig port 0 (xe0) of BCM56800 was configured for XAUI.

The HyperTerminal “tx” command generated 140,261,441 packets, 9000 bytes each from the BCM56800 to the LatticeSC Communications Platform Evaluation Board.

The “show counter” command was then used to monitor the status of BCM56800 TX and RX packet (GTPKT.xe0 and GRPKT.xe0) and byte (GTBYT.xe0 and GRBYT.xe0) counters. Figure 8 does not show any error counters. This is an indication that the error counters have remained at a zero value during the test. Additionally, the Lattice ORCAstra System GUI (shown in Figure 5) was monitored for proper flexiPCS 10-Gigabit Ethernet link state machine synchronization.

The results showed that all 140,261,441 Ethernet packets (1,262,352,969,000 bytes) were successfully transmitted to the LatticeSC/M and recovered at the BCM56800 error-free.

HiGig (10 Gbps) Results

As shown in Figure 9, HiGig port 0 (hg0) of BCM56800 was configured for HiGig (10 Gbps).

The HyperTerminal “tx” command generated 10,000,000 packets, 9000 bytes each from the BCM56800 to the LatticeSC Communications Platform Evaluation Board.

The “show counter” command was then used to monitor the status of BCM56800 TX and RX packet (GTPKT.hg0 and GRPKT.hg0) and byte (GTBYT.hg0 and GRBYT.hg0) counters. Figure 8 does not show any error counters. This is an indication that the error counters have remained at a zero value during the test. Additionally, the Lattice ORCAstra System GUI (shown in Figure 5) was monitored for proper flexiPCS 10-Gigabit Ethernet link state machine synchronization.

The results showed that all 10,000,000 Ethernet packets (90,080,000,000 bytes) were successfully transmitted to the LatticeSC/M and recovered at the BCM56800 error-free.

Summary

In conclusion, the LatticeSC/M FPGA family offers users built-in XAUI Physical Layer support and is fully inter-operable with Broadcom BCM56800 network switch in both XAUI and HiGig (10 Gbps) modes.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.