LatticeSC/M Broadcom® HiGig+™ 12 Gbps Physical Layer Interoperability Over CX-4

August 2007 Technical Note TN1154

Introduction

This technical note describes a physical layer HiGig+ 12 Gbps interoperability test between a LatticeSC/M device and the Broadcom BCM56802 network switch. The test was limited to the physical layer (up to XGMII) of the 10 Gigabit Ethernet protocol stack.

Specifically, the document discusses the following topics:

- Overview of LatticeSC™ and LatticeSCM™ devices and Broadcom BCM56802 network switch
- Physical layer interoperability setup and results

Two significant aspects of the interoperability test need to be highlighted:

- The BCM56802 uses a CX-4 HiGig+ port, whereas the LatticeSC Communications Platform Evaluation Board provides an SMA connector. So a CX-4 to SMA conversion board was used as a physical medium interface to create a physical link between both boards. The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels (12 Gbps bandwidth total). All four SMA channels (Quad 360) were connected to the LatticeSC side.
- The physical layer interoperability ran at a 12 Gbps data rate (15 Gbps aggregated rate). On the LatticeSC/M side, this was achieved by overclocking the SERDES reference clock to 187.5 MHz instead of 156.25 MHz. The Broadcom side automatically auto-negotiates to 12 Gbps when the LatticeSC/M device is running at this rate.

HiGig™ Protocol

The HiGig Protocol, as defined by Broadcom, provides a standard mechanism for interconnecting switches for a single system, defining an efficient way to forward frames for Unicast, Broadcast, Multicast (Layer 2 and IP), and Control Traffic. The HiGig protocol implements HiGig frames, which are formed by tagging standard Ethernet frames with a 12-byte HiGig header. The Broadcom proprietary HiGig+ protocol enables advanced features such as port trunking and mirroring across devices. Although based on a XAUI physical layer, HiGig+ offers a choice of 10 Gbps or 12 Gbps speeds.

LatticeSC/M and flexiPCS™ Overview

LatticeSC/M Features

The LatticeSC/M family, equipped with ASIC-based system level building blocks, was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide and phase shift PLLs, numerous DLLs and dynamic glitch-free clock MUX that are required in today's high-end system designs.

All LatticeSC/M devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic called flexiPCS. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES

LatticeSC flexiPCS in XAUI Mode

The XAUI mode of the flexiPCS block supports full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard. XAUI mode supports 10-Gigabit Ethernet as well as 10-Gigabit Fibre Channel applications.

Transmit Path Functionality (From LatticeSC Device to Line)

- Transmit State Machine that performs translation of XGMII idles to proper ||A||, ||K||, ||R|| characters according to the IEEE 802.3ae-2002 specification
- 8b10b encoding

Receive Path Functionality (From Line to LatticeSC Device)

- Word Alignment based on IEEE 802.3-2002 defined alignment characters
- 8b10b decoding
- Link State Machine functions incorporating operations defined in PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine compliant with the IEEE 802ae.3-2002 specification

Broadcom BCM56802 Overview

BCM56802 Features

The BCM56802 is a 16-port, 10-Gigabit Ethernet/HiGig+ multilayer switch chip. Each of these flexible ports supports 10-Gigabit Ethernet or 1-Gigabit Ethernet.

The BCM56802 supports sixteen HiGig2™/HiGig+/HiGig/10-GbE/1-GbE ports. This device is based on the StrataXGS® field-proven, robust architecture. Additionally, the BCM56802 includes integrated high-performance SERDES. The integrated SERDES functionality includes integrated XAUI SERDES for all 16 ports, and GbE SERDES per port for 1-Gigabit Ethernet. This device supports 196 Gbps switching capacity at line rate, and includes support for eight classes of service (CoS) plus two additional classes for Flow Control and system management per port.

BCM56802 Ports

The BCM56802 has 16 10-GbE/1-GbE ports. The BCM56802 is based on StrataXGS field-proven, robust architecture. It has integrated high-performance SERDES – integrated XAUI SERDES for all 16 10-GbE ports, and it uses single SERDES lane per port at GbE speeds. The device supports 192 Gbps switching capacity at line rate.

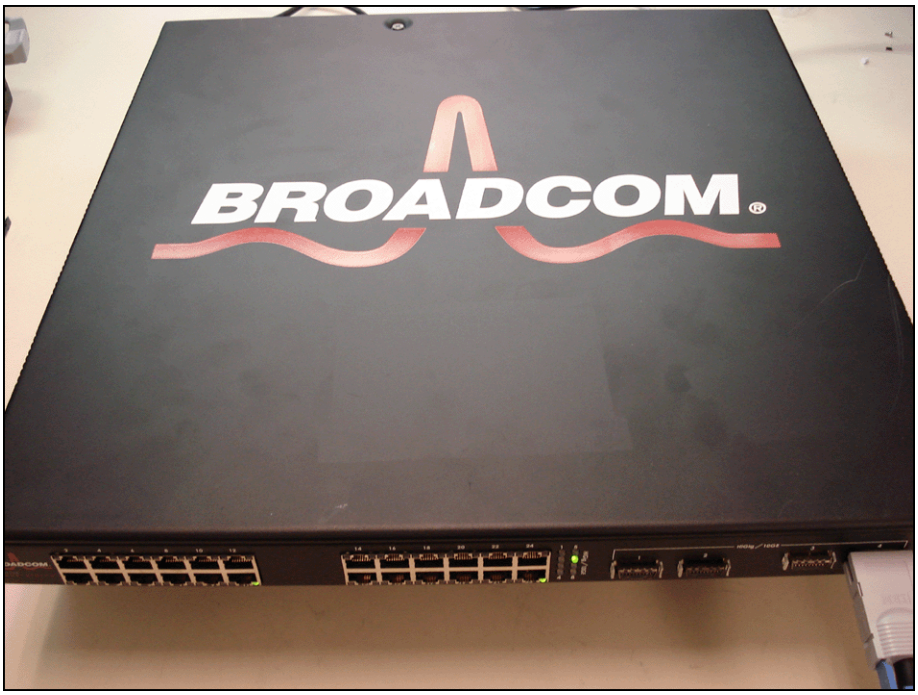
Test Equipment

Below is the equipment used in the interoperability tests.

Broadcom BCM56802 Network Switch

Figure 1 shows the BCM56802 network switch prototype development board (BCM956601K23REF).

Figure 1. Broadcom BCM56802 Network Switch Prototype Development Board



One can configure the Broadcom ports by connecting its serial port to a PC and starting a HyperTerminal session. A serial cable is connected to the serial port at the back of the BCM56802.

Figure 1 also shows a CX-4 connector inserted into one HiGig+ port available on the front right side of the BCM56802. This port, referred to as hg4, was selected for the interoperation with the LatticeSC/M part. It was configured in XAUI mode.

Agilent 81130A Pulse/Data Generator

The Agilent 81130A pulse/data generator was used to supply an external 187.5-MHz reference clock source to the LatticeSC/M flexiPCS.

For more information on this module, refer to Agilent's website: www.agilent.com.

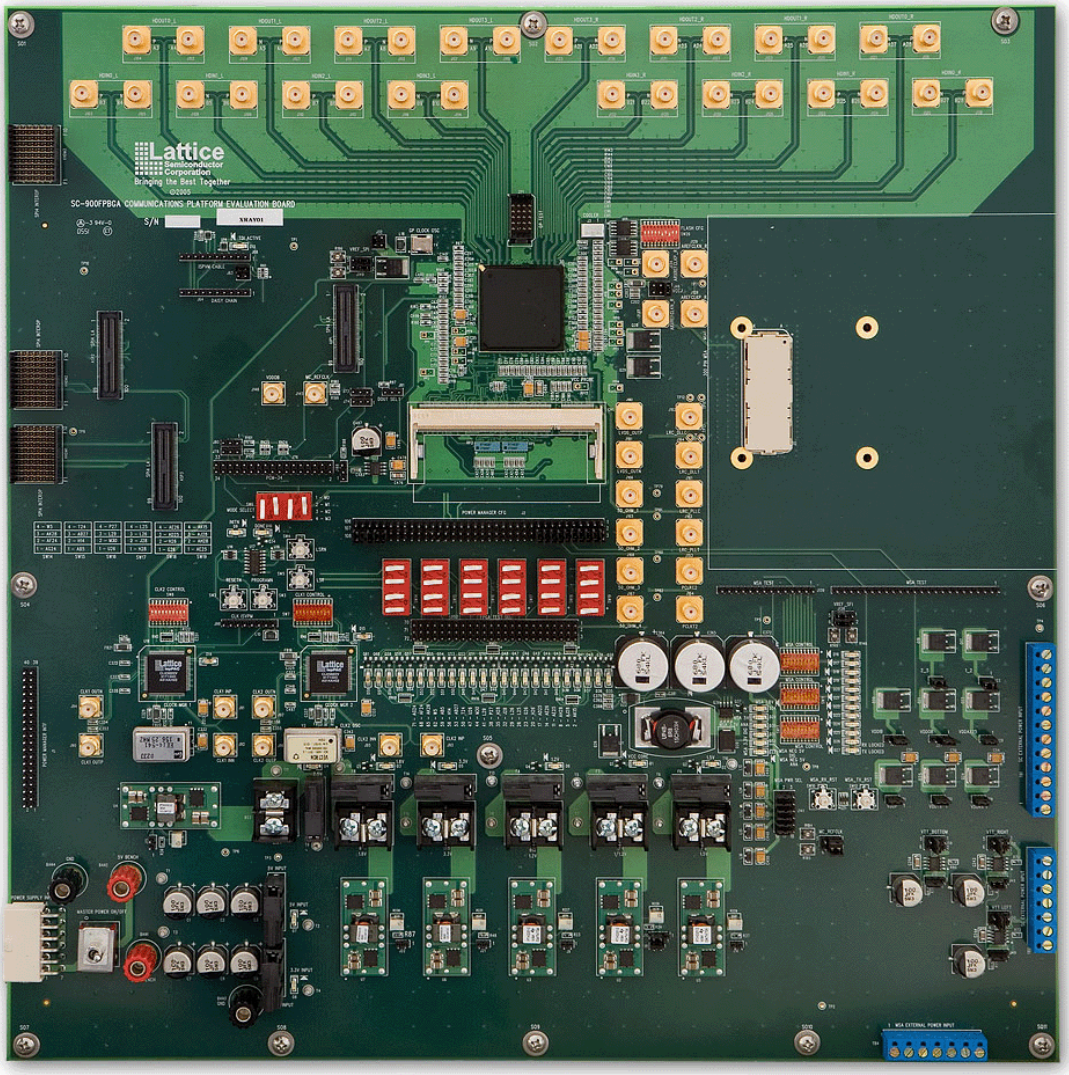
LatticeSC Communications Platform Evaluation Board

The LatticeSC Communications Platform Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC/M FPGA or to aid in the development of custom designs. Each LatticeSC Communications Platform Evaluation Board contains among others:

- LFSC3GA25E-6F900C FPGA device
- SMA test points for high-speed SERDES and clock I/O
- Onboard power connections and power sources
- Onboard interchangeable clock oscillator
- Onboard reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- Onboard Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 2 shows the LatticeSC Communications Platform Evaluation Board.

Figure 2. LatticeSC Communications Platform Evaluation Board



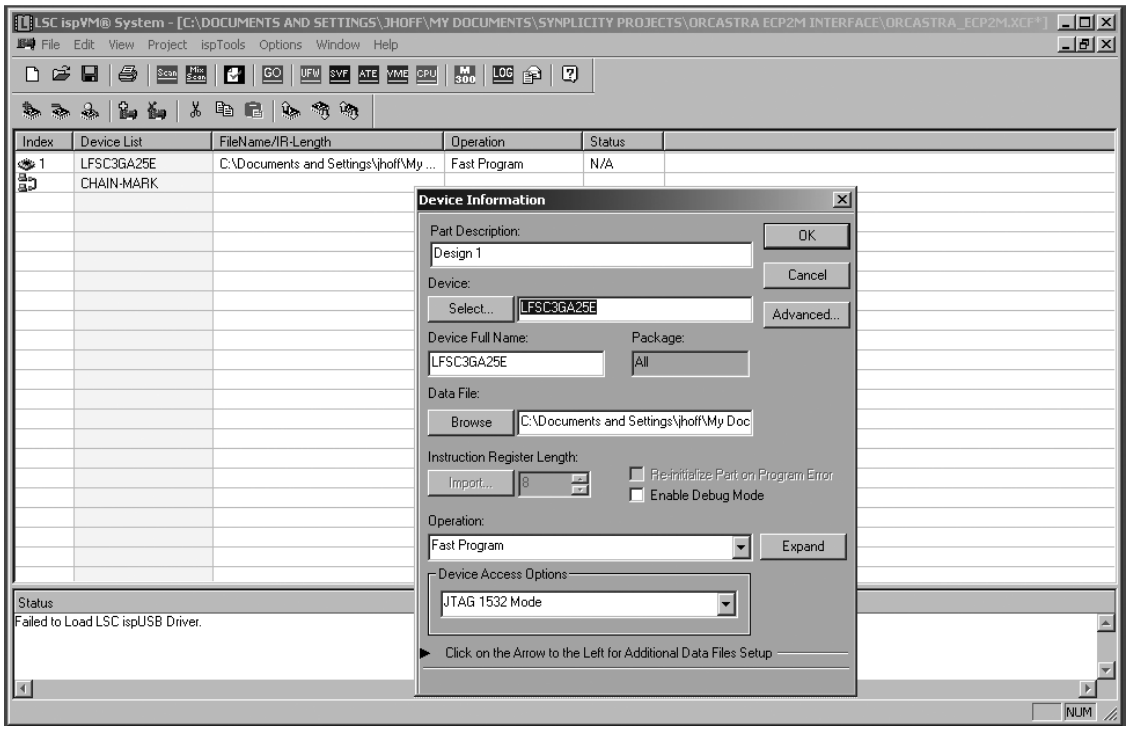
ispVM System

The ispVM® System is included with Lattice's ispLEVER® software and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice Semiconductor and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeSC/M bitstream, which configures the flexiPCS in 10-Gigabit Ethernet mode (XAUI).

Figure 3 shows a screen shot of the ispVM System.

Figure 3. ispVM System



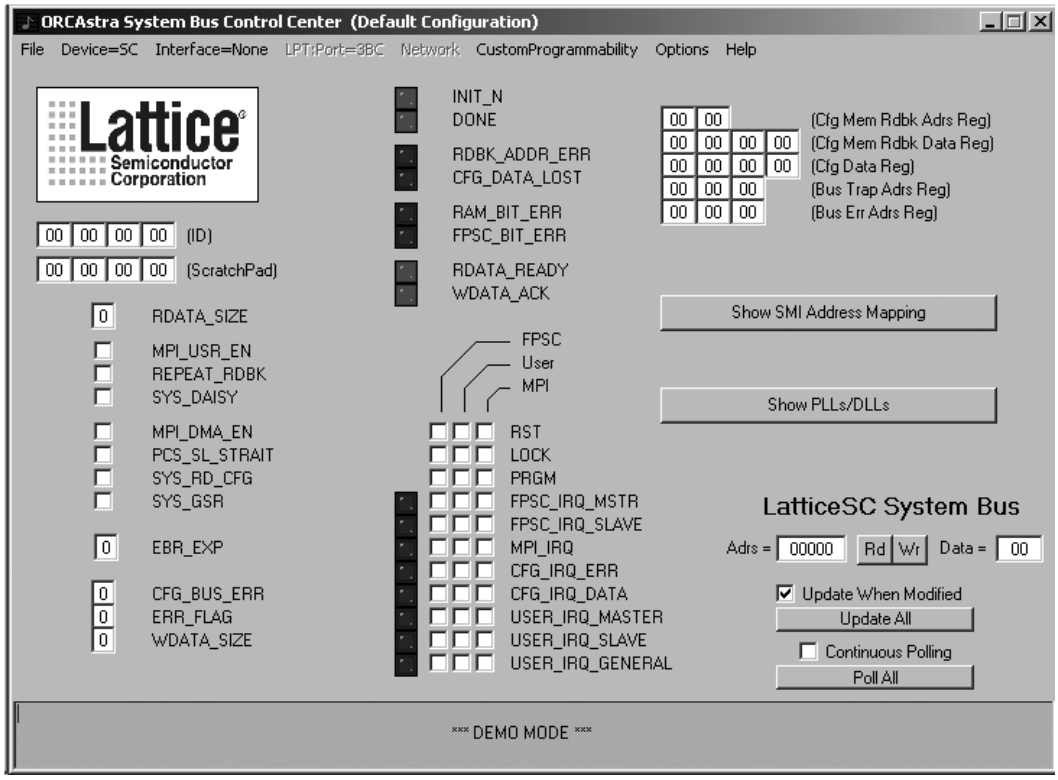
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy recompile process or making changes to their board.

Configurations created in the GUI can be saved to memory and reloaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeSC/M.

Figure 4 is a screen shot of ORCAstra System software.

Figure 4. ORCAstra System



Interoperability Testing

This section provides the details of the HiGig+ (12 Gbps) Physical Layer interoperability between a LatticeSC/M device and the Broadcom BCM56802 network switch. This interoperability tests the correct processing of HiGig+ (12 Gbps) data from the BCM56802 network switch to the LatticeSC/M flexiPCS XGMII interface and then back in the other direction. Particularly, the test verifies the ability to transfer packets across the system in an asynchronous way.

Test Setup

Figure 5 shows the LatticeSC Communications Platform Evaluation Board and Broadcom board connections.

Figure 6 is a block diagram of the test setup.

The setup includes:

- The Broadcom BCM56802 network switch.
- The LatticeSC Communications Platform Evaluation Board. In 10-Gigabit Ethernet, the Agilent 811130A Data/Pulse Generator provides an external 187.5-MHz reference clock to the LatticeSC/M flexiPCS. The flexiPCS multiplies the reference clock by 20 to achieve a 15-Gbps aggregated rate (12-Gbps data rate).
- A PC for software control/monitoring.
- A CX-4 to SMA conversion board was used as a physical Medium interface to create a physical link between both boards (see Figure 5). The SMA side of the CX-4 to SMA conversion board has four differential TX/RX channels, or 16 SMA connectors for a total bandwidth of 12 Gbps (15-Gbps aggregated rate). All four differential TX/RX channels were connected to the LatticeSC side (as shown in Figure 5).

- Cables:
  - 16 SMA for LatticeSC/M flexiPCS channels 0 through 4
  - Two SMAs for Agilent clock generator
  - CX-4 for BCM56802 HiGig+ port hg4
  - ispVM JTAG cable for downloading LatticeSC bitstream and ORCAstra GUI access
  - Serial cable for BCM56802 HyperTerminal access

Figure 5. Board Connections

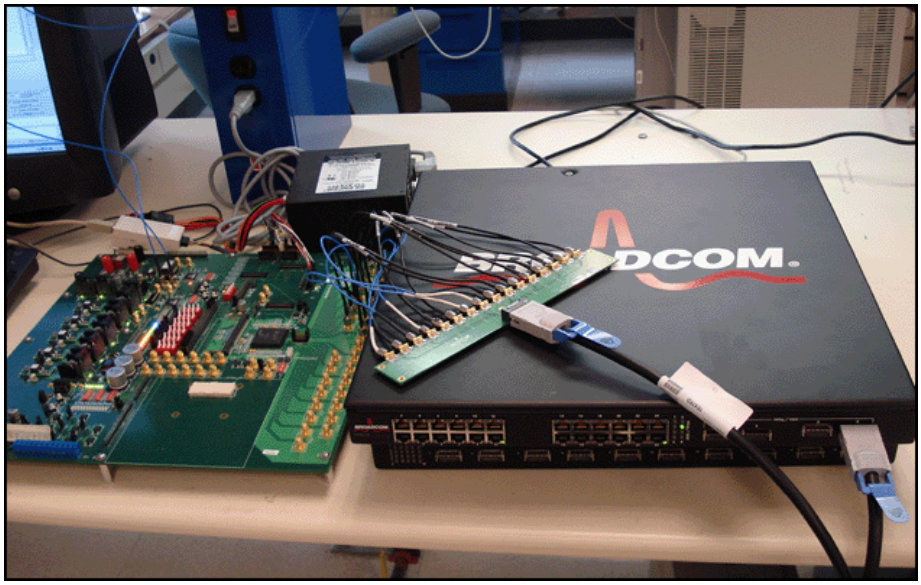
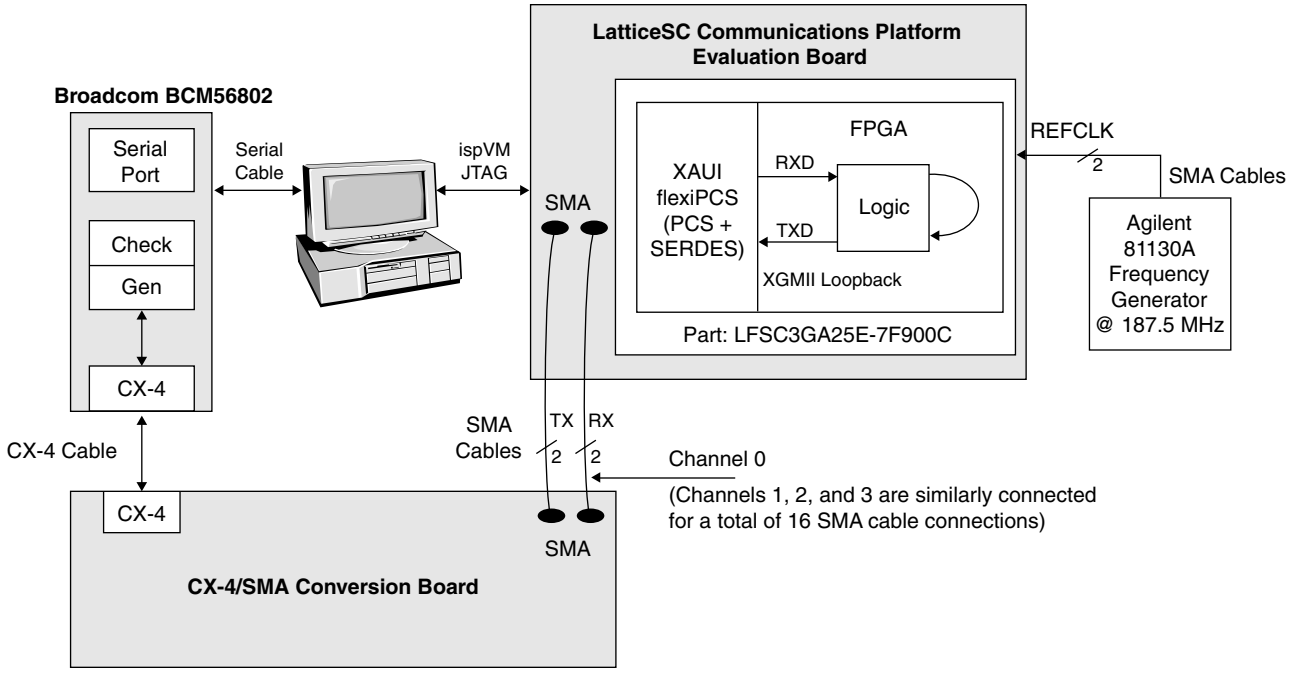


Figure 6. Test Setup Block Diagram



Test Description

This section describes how each interoperability partner is set up for HiGig+ Physical layer interoperability.

BCM56802
The BCM56802 switch generates and checks full protocol-compliant HiGig+ (12 Gbps) packets. The BCM56802 is configured in HiGig+ mode.

Figure 7 illustrates the sequence of events performed in a HyperTerminal from start-up to configure HiGig+ port 4 (hg4) to transmit and check HiGig+ packets.

Figure 7. Configuring BCM56802 port 0 in HiGig+

```
BCM.0> rc
rc: unit 0 device BCM56802_A0
BCM.0> ps
      ena/  speed/  link  auto    STP          lrn  inter   max  loop
port  link  duplex  scan  neg?   state   pause  discrd  ops   face frame  back
hg4   up    12G FD    SW   Yes  Forward          None    FA  XGMII 16360
BCM.0> tx 121692430 pbm=hg4 len=9000 sm=00:00:00:00:00:01 dm=00:00:00:00:00:02
BCM.0> show counters
RUC.hg4          :            121,692,430        +121,692,430
ITPKT.hg4        :            121,692,430        +121,692,430
ITOVR.hg4        :            121,692,430        +121,692,430
IT9216.hg4       :            121,692,430        +121,692,430
ITBYT.hg4        :      1,096,205,409,440  +1,096,205,409,440
IR9216.hg4       :            121,692,430        +121,692,430
IRPKT.hg4        :            121,692,430        +121,692,430
IROVR.hg4        :            121,692,430        +121,692,430
IRBYT.hg4        :      1,096,205,409,440  +1,096,205,409,440
BCM.0>
```

LatticeSC Communications Platform Evaluation Board
The Agilent 81130A clock generator provides the 187.5 MHz clock oscillator source to the LatticeSC/M PCS reference clock for XAUI. The flexiPCS multiplies the reference-clock by 20 to achieve a 12-Gbps data rate (15-Gbps aggregated rate).

In the RX direction, The LatticeSC/M SERDES recovers the packets from the BCM56802 device, and the flexiPCS converts them into XGMII format.

The XGMII loopback logic in the FPGA portion loops the XGMII data back into the TX direction. The LatticeSC/M device then transmits the packets back to the BCM56802 device.

HiGig+ (12 Gbps) Results

As shown in Figure 7, HiGig+ port 4 (hg4) of BCM56802 was configured to transmit HiGig+ packets.

The HyperTerminal “tx” command generated 121,692,430 packets, 9000 bytes each from the BCM56802 to the LatticeSC Communications Platform Evaluation Board.

The “show counter” command was then used to monitor the status of the BCM56802 TX and RX packets (GTPKT.hg4 and GRPKT. hg4) and byte (GTBYT. hg4 and GRBYT. hg4) counters. Figure 7 does not show any error counters. This is an indication that the error counters have remained at a zero value during the test. Additionally, the Lattice ORCAstra System GUI (shown in Figure 4) was monitored for proper flexiPCS 10-Gigabit Ethernet link state machine synchronization.

The results show that all 121,692,430 HiGig+ packets (1,096,205,409,440 bytes) were successfully transmitted to the LatticeSC/M and recovered at the BCM56802 error-free.

Summary

In conclusion, the LatticeSC/M FPGA family offers users a built-in XAUI Physical Layer support and is fully interoperable with Broadcom BCM56802 network switch in XAUI HiGig+ (12 Gbps) mode.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
June 2007	01.0	Initial release.