PCI Express SIG Compliance Overview for Lattice Semiconductor FPGAs

August 2007 Technical Note TN1166

Introduction

The PCI Express compliance testing is offered by the PCI Special Interest Group (PCI SIG). The Compliance Workshop Program offers standardized device testing and comprehensive criteria for PCI Express systems, peripherals, and components. The program provides FPGA manufacturers the opportunity to test a SERDES-based FPGA and the needed Intellectual Property (IP) on a compliant add-in card with other members' PCI Express products. This forum allows for the delivery of devices and IP that are compliant with PCI Express standards. Successful completion of PCI Express compliance testing provides our customers with a level of confidence when using Lattice's FPGAs to build PCI Express solutions. It assists FPGA designers to achieve interoperability while minimizing risk and reducing time to market in designs that use complex, high performance PCI Express interfaces with Lattice FPGAs.

The PCI SIG Compliance Program, which is open to all members of the PCI SIG, is a voluntary compliance program. Testing is completed to insure devices meet the PCI SIG specifications and provides a vehicle to test with many other manufacturers of PCI Express products. The goal is to promote the development of high-quality products that offer reliable and hassle-free operation.

Device manufacturers use the PCI SIG as a means to ultimately be included on the PCI SIG Integrators List. Products that implement PCI SIG technologies and are referenced on the Integrators List show that they fulfill the stringent requirements and will provide a robust solution. The PCI SIG compliance program is made up of several mandatory test procedures (called Gold Tests) as well as an interoperability program.

This goal of this technical note is to demystify the process and provide an understanding of the PCI SIG Compliance Program. Data collected in the Lattice PCI Express laboratory is presented and milestones for emerging Lattice PCI Express products are highlighted.

End-point Add-in Cards

In a typical PCI Express implementation, a CPU is connected to a root device and is responsible for configuring and enumerating all plug-and-play PCI Express end-point devices in a system. Because the PCI Express system is point-to-point, a switch device is necessary to grow the number of devices or end-points in a system. Although only one root exists in any system, there are one or more end-point devices. A standard PC motherboard provides several expansion PCI Express slots that accept add-in PCBs. FPGA based end-point designs provide a high level of integration enabling high-performance, fully compliant PCI Express systems in a single device. Hence, these are becoming increasingly popular for add-in card designs.

PCI Express end-point add-in cards developed by Lattice provide the physical means to test devices at the compliance workshop. The form-factor compliant printed circuit boards (shown in the figures below) are utilized to test the device performance and to exercise the IP used to implement the PCI Express functionality. The boards are tested for electrical compliance, subjected to link and transaction protocol tests, and checked for proper configuration space implementation. Participants pass or fail at the compliance workshop by attending testing sessions.

Figure 1. LatticeECP2M PCI Express x4 Evaluation Board

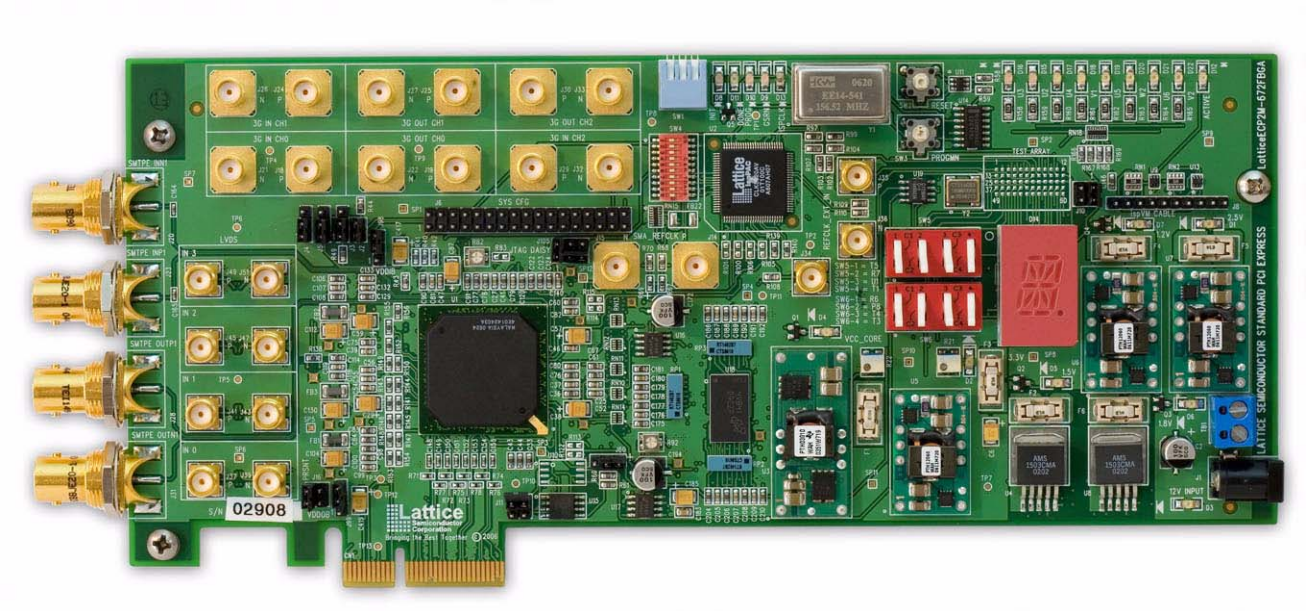


Figure 2. LatticeSCM80 PCI Express x8 Evaluation Board

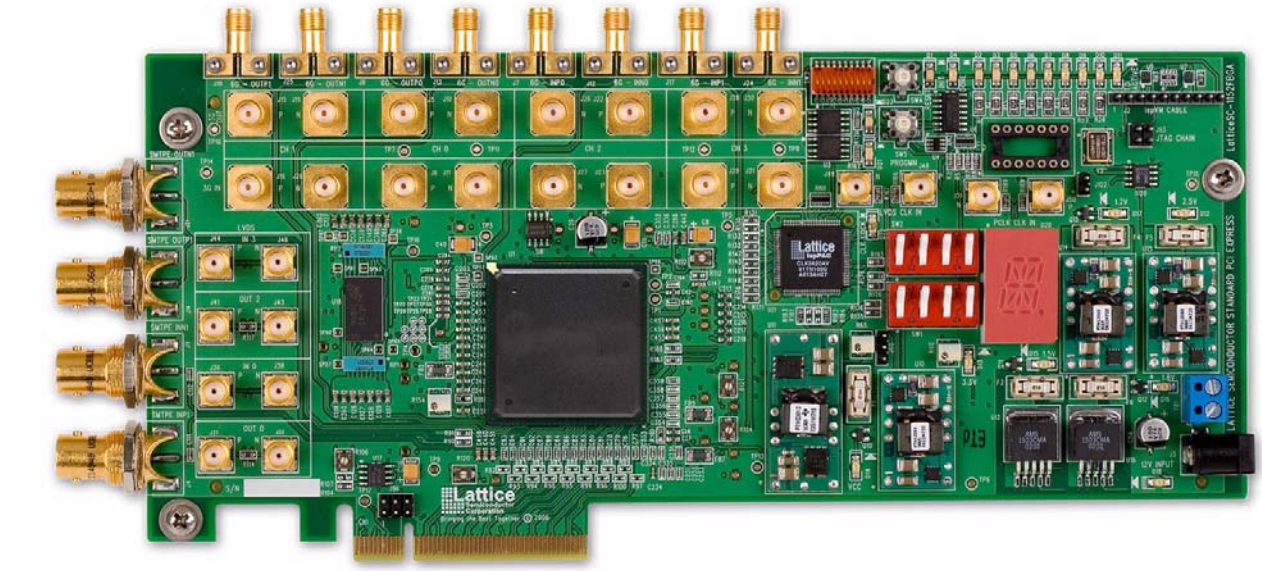
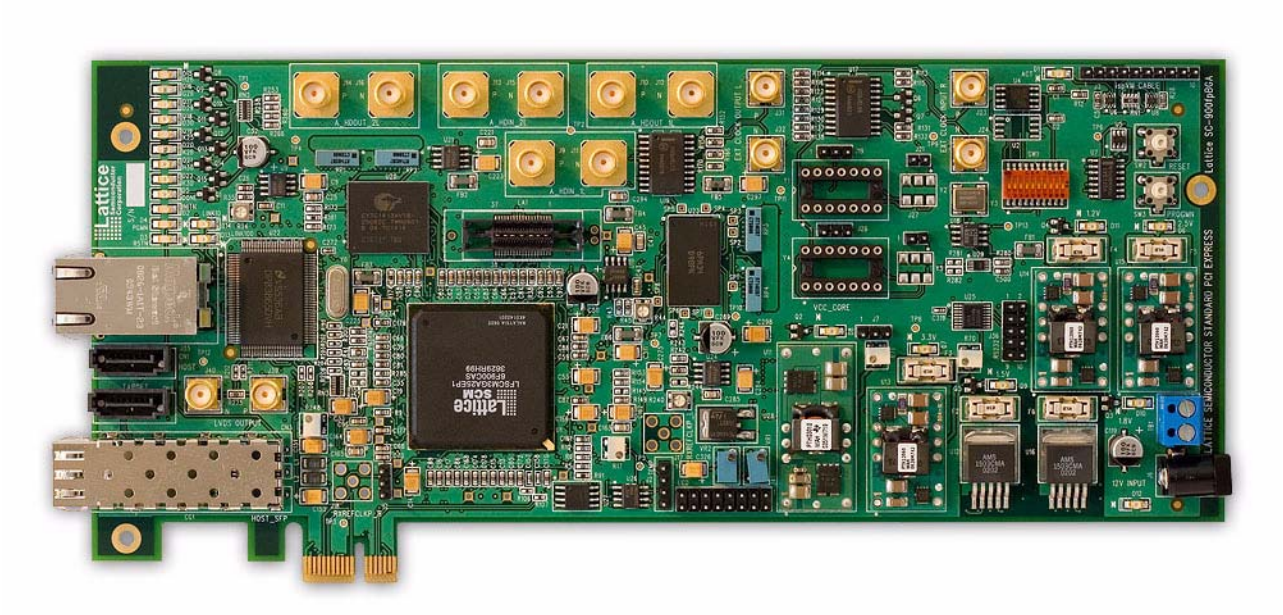


Figure 3. LatticeSCM25 PCI Express x1 Evaluation Board



The PCI SIG provides complete information about the compliance tests on their website at www.pcisig.com. There are also interoperability test sessions with other peer companies outside the mandatory tests. These interoperability sessions are used to test interoperability between the Lattice add-in boards and other PCI Express systems and will be discussed later in this technical note.

Compliance Testing

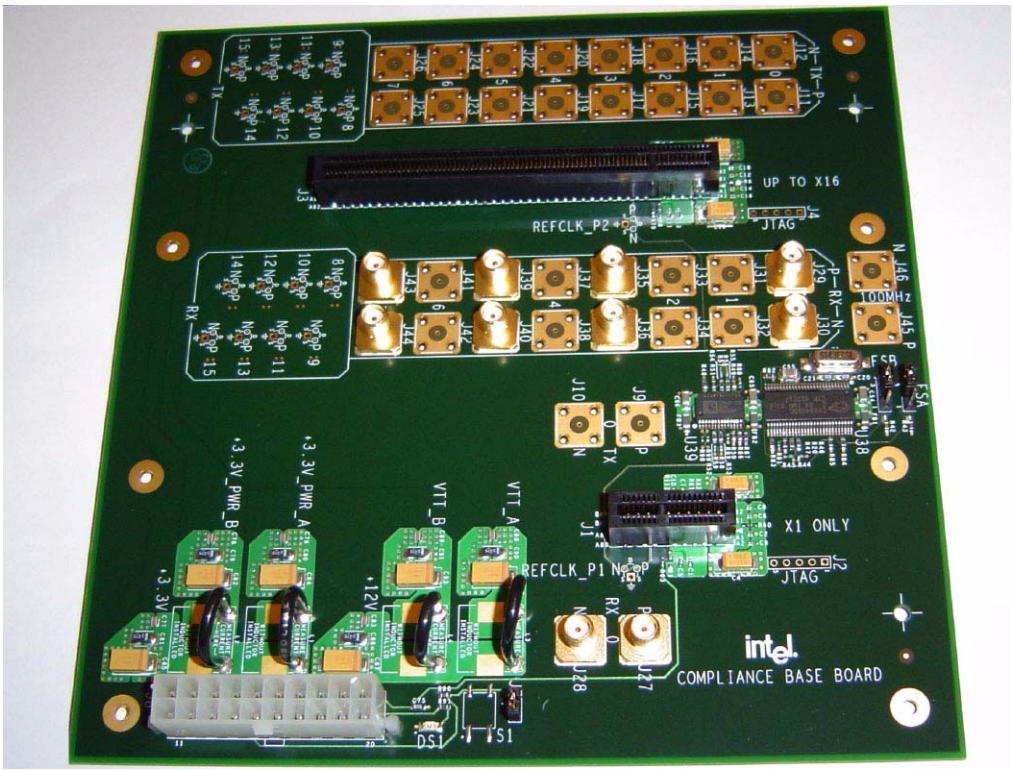
There are four test areas that make up PCI Express compliance testing for components tested on add-in cards.

- **Electrical Testing** – Examines device and add-in card signal quality for eye pattern, jitter and bit rate analysis.
- **Configuration Space Testing** (a.k.a. CV Testing) – Examines configuration space in PCI Express devices by verification of required fields and values.
- **Link and Transaction Protocol Testing** (a.k.a. PTC Testing) – Tests device behavior for link-level protocol and device behavior for transaction-level protocol. Link and transaction layers are exercised for protocol boundary conditions. Tests include error injection and check error-handling capabilities.
- **Interoperability Testing** – Tests conducted between workshop participants that show compatibility between PCI Express technologies.

PCI Express Electrical Testing

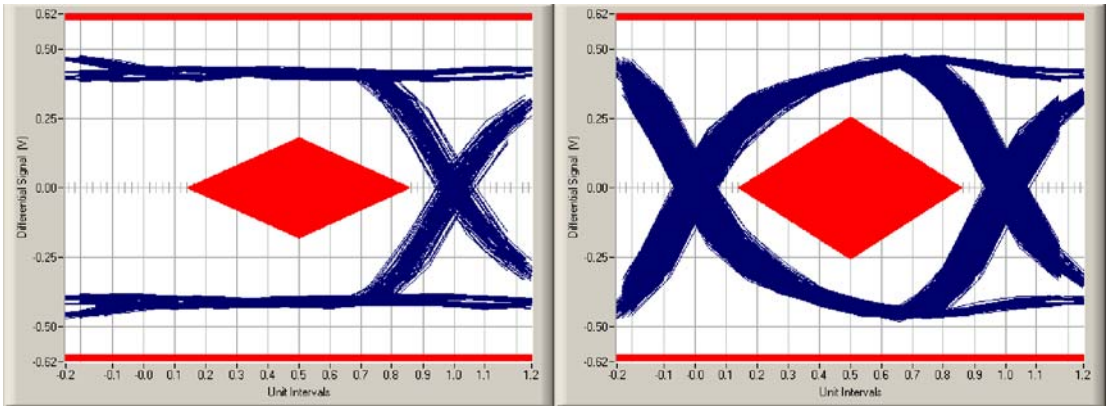
PCI Express Electrical Testing was developed to help verify product-level physical compliance to the PCI Express Base Specification(s). PCI Express Electrical Testing consists of a series of tests used to evaluate PCI Express root systems/motherboards and PCI Express add-in card products. Testing on FPGA add-in cards is done using a compliance baseboard (CBB) available from the PCI SIG. The CBB provides the physical means to connect the add-in card to a high-speed oscilloscope for measuring and analyzing the electrical performance of the device.

Figure 4. PCI Express Compliance Base Board



Once the data is gathered from the CBB, analysis software is used to post process the information and determine whether the device meets specification. The test criteria are specified in the *PCI Express Architecture PHY Electrical Test Considerations*, Revision 1.1, February 2007 documentation. The SIGTest Version 2.1 software package was used to analyze the captured data. The software checks for complete and correct compliance pattern transmission, signal quality and jitter compliance.

Figure 5. Example Results from Electrical SIGTEST of SCM80 Add-in Card



PCI Express Configuration Space Testing

The PCI Express Configuration Verifier (CV) test is a software application provided by PCI SIG that runs on a Windows XP PC and exercises access to the configuration space registers of the device under test. Its purpose is to check for compliance with the PCI specification for Type 1 configuration space registers. A detailed description of tests performed can be found in the document *Configuration Space Test Considerations,* revision 1.0, April 26, 2004. The tests are conducted with the add-in card placed in a PCI Express slot in the PC. The test software

accesses the add-in card and issues configuration read and write requests and checks for the correct response. The tests check the following:

- Configuration space registers can be read
- Read-only registers retain their value when written to
- Writable registers can be written to
- Registers have the correct default value after reset
- Capabilities lists are valid and correctly linked
- PCI Express 1.0a and/or 1.1 specific fields and capabilities are present

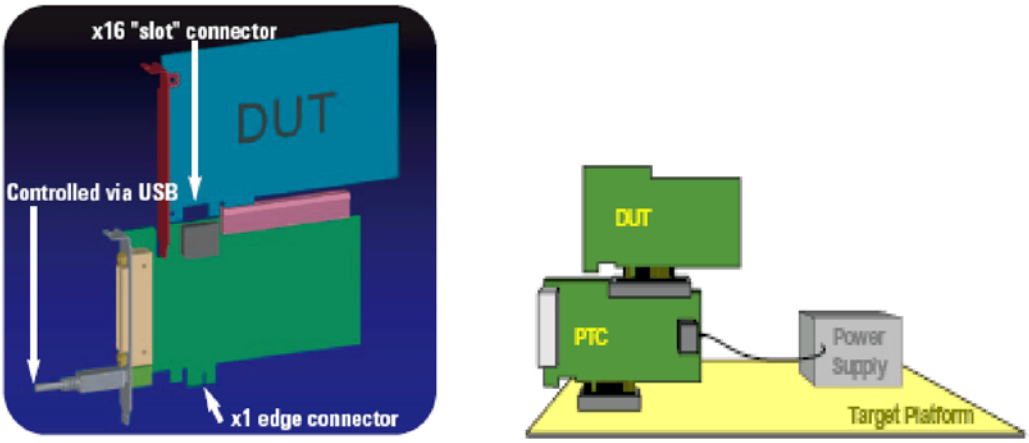
The test program also performs functional stress tests to ensure the end-point can retrain and relink in an acceptable amount of time. It also tests to make sure the card can properly handle hundreds of cycles of link-up/link-down and all registers are operational (i.e., the end-point firmware has not locked up).

In summary, the CV test suite verifies that the PCI Express end-point is truly functional in a PC and covers all aspects of hardware and operating system interaction. It shows that the card can be recognized by the PCI Express hardware and can be enumerated and configured by the operating system for access by software applications.

PCI Express Link and Transaction Protocol Testing

The PCI Express Link and Transaction Layer protocol testing was developed to test add-in card compliance to the Link and Transaction protocol specification requirements. The tests utilize an Agilent Protocol Test Card (PTC) and associated test software (Agilent Technologies E2969A Protocol Test Card for PCI Express). The tests include automated pre-canned compliance tests for the Transaction Layer and the Data Link Layer. The PTC carefully monitors the behavior of the DUT in response to certain error conditions. The PTC card is simply plugged into the PCI Express add-in card under test.

Figure 6. PTC Connection to Add-in Card



During link testing, the following tests are run using the PTC card. All of the following tests must be passed in order to be included on the Integrators List.

- **Reserved Fields** – Device ignores them
- **NAK Response** – Device will resend after receiving NAK
- **Replay Timers** – Device will resend packet if no response

- **Replay Count** – Device will resend multiple times when no response
- **Link Retrain** – Device will retrain if continued no response
- **Replay TLP Order** – Device replays TLPs in proper order
- **Bad CRC** – Device detects, drops, and logs (DLLPs and TLPs)
- **Undefined Packet** – Device ignores
- **Bad Sequence Number** – Device detects, drops, and logs
- **Duplicate TLP** – Device returns data once

PCI Express Interoperability

The interoperability test sessions are used to show consistent interoperability, as they provide advance warning of problems that users might encounter with PCI Express products. During these sessions, the participants set their own test procedures and must agree on what constitutes a pass or a fail. Participants are expected to demonstrate some degree of functionality to substantiate that their interface is functional with another vendor's products.

The PCI SIG recognizes that participants may bring designs that are not fully compliant or have unknown or undisclosed bugs. For this reason, to pass the interoperability tests, vendors must only demonstrate a success rate of 80%. If they have passed 100% of the PCI SIG mandatory tests (Gold Tests) and the 80% interoperability, the device is eligible to be included on the Integrators List. The Integrators List is proof a product has passed the rigorous PCI SIG tests and has demonstrated interoperability with others. This status implies that the device is viable for use in PCI Express systems.

The tables provided below outline the interoperability status of Lattice devices both from the PCI SIG compliance workshops and the Lattice PCI Express test lab. The status shows system details, the slot of the add-in board in the root system, operating system, and the status of the passing system must be able to boot and execute the Lattice Interoperability Demo.

Table 1. LatticeSCM25 Interoperability Results

System/Motherboard	Chip Set	Operating System	Slot (Physical)	Boot/Demo x1[1]
Intel D975DX	Intel 975X	XP Pro	x16-1	—
			x8	PASS
			x16-2	PASS
ASUS	Nvidia nForce4	XP Pro	x1 - 1	—
			x1 - 2	PASS
			x4-1	PASS
			x16-1	—
			x16-2	PASS
Dell	Intel	XP	x1	—
HP ProLiant		Server 2003	x16	PASS
Gigabyte	Nvidia nForce 590	XP Pro	x1-1	—
			x1-2	PASS
			x8	PASS
			x16-1	PASS
			x16-2	PASS
Intel 915GEVLK	Intel 915	Server 2003	x1-1	PASS
			x1-2	PASS
			x16	N/A

Table 1. LatticeSCM25 Interoperability Results (Continued)

System/Motherboard	Chip Set	Operating System	Slot (Physical)	Boot/Demo x1[1]
ASUS M2N32-WS	Nvidia nForce 590	XP Pro	x1-1	—
			x1-2	PASS
			x16-1	PASS
			x16-2	PASS
Intel B975XBX	i975	Win2K	x4	PASS
			x8	PASS
			x16	PASS
Dell Optiplex GX620	i945	XP	x1	PASS
			x16	N/A
ASUS P5RD1-VM	ATI	XP	x1	PASS
			x16	PASS
Dell Precision 470	Intel E7525	Linux	x4	PASS
Dell PowerEdge SC430	Intel E7230	Server2003	x1	PASS
			x8	PASS
			x4	PASS
ASUS P5RD1-V	ATI Radeon Express	XP	x1	PASS
			x1	PASS
			x16	PASS
			x1	PASS
ASUS P5LD2-VM	Intel i945G	XP	x1	PASS
			x16	N/A
ASUS M2N32-WS	Nvidia nForce 590	Server 2003	x1	PASS
			x16	PASS
			x16	PASS
			x1	—
HP Proliant DL145 Server	AMD	Server 2003	x16	PASS
VIA K8T890	VIA	XP	x1	PASS
			x1	PASS
			x16	PASS

1. A dash designates a physical limitation not permitting testing, N/A designates incompatibilty with the graphics slot.

Table 2. LatticeSCM80 Interoperability Results

System/Motherboard	Chip Set	Operating System	Slot (Physical)	Boot/Demo x4[1]	Boot/Demo x1[1]
Intel D975DX	Intel 975X	XP Pro	x16-1	—	—
			x8	PASS	PASS
			x16-2	PASS	PASS
ASUS	Nvidia nForce4	XP Pro	x1 - 1	—	—
			x1 - 2	—	PASS
			x4-1	PASS	PASS
			x16-1	—	—
			x16-2	PASS	PASS
Dell	Intel	XP	x1	—	—

Table 2. LatticeSCM80 Interoperability Results (Continued)

System/Motherboard	Chip Set	Operating System	Slot (Physical)	Boot/Demo x4[1]	Boot/Demo x1[1]
HP ProLiant		Server 2003	x16	PASS	PASS
Gigabyte	Nvidia nForce 590	XP Pro	x1-1	—	—
			x1-2	—	PASS
			x8	PASS	PASS
			x16-1	PASS	PASS
			x16-2	PASS	PASS
Intel 915GEVLK	Intel 915	Server 2003	x1-1	—	PASS
			x1-2	—	PASS
			x16	N/A	N/A
ASUS M2N32-WS	Nvidia nForce 590	XP Pro	x1-1	—	—
			x1-2	—	PASS
			x16-1	PASS	PASS
			x16-2	PASS	PASS
Intel B975XBX	i975	Win2K	x4	PASS	PASS
			x8	PASS	PASS
			x16	PASS	PASS
Dell Optiplex GX620	i945	XP	x1	—	PASS
			x16	N/A	N/A
ASUS P5RD1-VM	ATI	XP	x1	—	PASS
			x16	PASS	PASS
Dell Precision 470	Intel E7525	Linux	x4	PASS	PASS
Dell PowerEdge SC430	Intel E7230	Server2003	x1	—	PASS
			x8	PASS	PASS
			x4	PASS	PASS
ASUS P5RD1-V	ATI Radeon Express	XP	x1	—	PASS
			x1	—	PASS
			x16	PASS	PASS
			x1	PASS	PASS
ASUS P5LD2-VM	Intel i945G	XP	x1	—	PASS
			x16	N/A	N/A
ASUS M2N32-WS		Server 2003	x1	—	PASS
			x16	PASS	PASS
			x16	PASS	PASS
			x1	—	—
HP Proliant DL145 Server	AMD	Server 2003	x16	PASS	PASS
VIA K8T890	VIA	XP	x1	—	PASS
			x1	—	PASS

1. A dash designates a physical limitation not permitting testing, N/A designates incompatibilty with the graphics slot.

Table 3. LatticeECP2M Interoperability Results

System/Motherboard	Chip Set	Operating System	Slot (Physical)	Boot/Demo x4[1]	Boot/Demo x1[1]
Intel D975DX	Intel 975X	XP Pro, SP2	x16-1		
	NB: 975x		x8	PASS	PASS
	SB: 82801GH		x16-2	PASS	PASS
ASUS	nVdia nForce4	XP Pro, SP2	x1-1	—	
	NB: nVdia nForce4 SLI		x1-2	—	PASS
	SB: nVidia nForce4 PCI/ISA Bridge		x4-1	PASS	PASS
			x16-1		
			x16-2	PASS	PASS
HP ProLiant	nVdia nForce4	Server 2003, SP1	x16	PASS	PASS
	NB: nVdia nForce4				
	SB: nVidia nForce4 PISA Bridge				
Gigabyte	nVidia nForce 590	XP Pro, SP2	x1-1	—	
	NB: nVidia nForce 590 SLI		x1-2	—	PASS
	SB: MCP55		x8	PASS	PASS
			x16-1	PASS	PASS
			x16-2	PASS	PASS
Intel 915GEVLK	Intel 915	Server 2003	x1-1	—	PASS
	NB: 915		x1-2	—	PASS
	SB: ICH6/ICH6R		x16	N/A	N/A
ASUS M2N32-WS	nVidia nForce 590	XP Pro, SP2	x1-1	—	
	NB: nVidia nForce 590 SLI		x1-2	—	PASS
	SB: MCP55		x16-1	PASS	PASS
			x16-2	PASS	PASS
ASUS P5B	Intel 965	XP Pro, SP2	x1-1	—	PASS
	NB: 965		x1-2	—	PASS
	SB: ICH8		x1-3	—	PASS
			x16-1	PASS	PASS

1. A dash designates a physical limitation not permitting testing, N/A designates incompatibilty with the graphics slot.

Summary

PCI Express technology has become the standard infrastructure for next-generation computing. Hardware and system designers face many challenges when developing systems based on PCI Express. The solutions offered by Lattice have been tested both in-house and in PCI SIG workshops. The PCI SIG compliance testing results are listed below.

Table 4. PCI SIG Compliance Test Suite Results

	SCM25	SCM80	ECP2M	SCM25	SCM80	ECP2M	ECP2M
	x1	x4	x1	x1	x4	x1	x4
PCI SIG Test Suite	1.0a	1.0a	1.0a	1.1	1.1	1.1	1.1
PCI Express Electrical	Pass	Pass	Pass	Pass	Pass	Pass	Pass
PCI Express CV	Pass	Pass	Pass	Pass	Pass	Pass	Pass
PCI Express PTC	Pass	Pass	Pass	Pass	Pass	Pass	Pass
80% Interoperability	Pass	Pass	Pass	Pass	Pass	Pass	Pass

While the PCI SIG website provides some details, this document is designed to outline the procedures used by the PCI Express Compliance Workshop and convey a general understanding of the purpose of the PCI Express Integrators List. Table 5 outlines the Lattice FPGA devices listed on the PCI SIG Integrators List.

Table 5. Lattice PCI Express Products Listed on PCI SIG Integrators List

LatticeECP2M x4 End-point for PCI Express	Component/IP	PCI Express 1.1	PCI Express x4 End-point Controller
LatticeSCM End-point for PCI Express x1	Component/IP	PCI Express 1.1	PCI Express x1 End-point Controller
LatticeSCM End-point for PCI Express x4	Component/IP	PCI Express 1.1	PCI Express x4 End-point Controller
LatticeECP2M End-point for PCI Express x1	Component/IP	PCI Express 1.0a	PCI Express x1 End-point Controller
LatticeSCM End-point for PCI Express x1	Component/IP	PCI Express 1.0a	PCI Express x1 End-point Controller
LatticeSCM End-point for PCI Express x4	Component/IP	PCI Express 1.0a	PCI Express x4 End-point Controller

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2007	01.0	Initial release.