LatticeECP2M/Marvell Gigabit Ethernet Physical Layer Interoperability

July 2007 Technical Note TN1163

Introduction

This technical note describes a 1000BASE-X physical layer Gigabit Ethernet interoperability test between a LatticeECP2M™ device and the Marvell® Alaska® Ultra 88E1111/ 88E1112 devices. The test was limited to the physical layer (up to GMII) of the Gigabit Ethernet protocol stack.

Specifically, the document discusses the following topics:

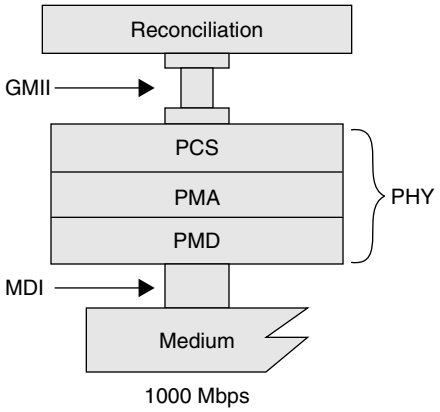
- Overview of LatticeECP2M devices Marvell Alaska Ultra 88E1111/ 88E1112 devices
- 1000BASE-X physical layer interoperability setup and results

Gigabit Ethernet Physical Layer

The IEEE 802.3-2002 Gigabit Ethernet standard is organized along architectural lines, emphasizing the large-scale separation of the system into two parts: the Media Access Control (MAC) sub-layer of the Data Link Layer and the Physical Layer.

Figure 1 highlights the sub-layers that constitute the Gigabit Ethernet Physical Layer.

Figure 1. Gigabit Ethernet Physical Layer



According to the 802.3-2002 standard, two important compatibility interfaces are defined within what is architecturally the Physical Layer:

- **Medium Dependent Interfaces (MDI)**. To communicate in a compatible manner, all stations shall adhere rigidly to the exact specification of physical media signals defined in Clause 8 (and beyond) in the IEEE 802.3-2002 standard, and to the procedures that define correct behavior of a station. Local Area Network requires complete compatibility at the Physical Medium interface (that is, the physical cable interface).
- **Gigabit Media Independent Interface (GMII)**. The GMII is designed to connect a gigabit-capable MAC or repeater unit to a gigabit PHY. While conformance with implementation of this interface is not strictly necessary to ensure communication, it is highly recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at gigabit speeds. The GMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the GMII. The GMII is optional.

The 1000BASE-X Gigabit Ethernet standard specifies a 1 Gbps data rate (1.25 Gbps aggregated rate).

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Also, the LatticeECP2M and Marvell Alaska interoperability exercises the whole physical layer, including GMII.

LatticeECP2M/PCS Overview

LatticeECP2M Features

The LatticeECP2/M family of FPGA devices has been optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP™ blocks and advanced configuration support, including encryption and dual-boot capabilities.

The LatticeECP2M family of devices features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and Gigabit Ethernet), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip-to-chip and small form factor backplane applications.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP2/M family of FPGA devices

LatticeECP2M Gigabit Ethernet Solution

The LatticeECP2M achieves Gigabit Ethernet compliance by combining both a PCS block and GbE soft IP in FPGA logic.

The LatticeECP2M Gigabit Ethernet Solution has the following features:

- Word Alignment based on IEEE 802.3-2002 defined alignment characters (PCS)
- 8b10b Encoding/Decoding (PCS)
- Link State Machine functions compliant with the IEEE 802.3-2002 specification (PCS)
- Clock Tolerance Compensation logic capable of accommodating clock domain differences (PCS)
- Management registers access through serial or parallel control interface
- 2-wire, CML differential 1000BASE-X Interface operating at 1.25Gbps (PCS)
- Transmit Gigabit Ethernet clock embedded in data stream (no external Gigabit Ethernet transmit clock) (PCS)
- Receive clock recovered from data stream (no external receive clock) (PCS)
- Transmit State Machine, which performs 8-bit data encapsulation and formatting, including the Auto-Negotiation code word insertion and outputting the correct 8-bit code/data word and k control characters according to the IEEE 802.3-2002 specification (GbE soft IP)
- Receive State Machine including Auto-Negotiation support compliant to the IEEE 802.3-2002 specification (GbE soft IP)

Marvell Alaska Ultra 88E1111/88E1112 Overview

88E1111/88E1112 Features

The Alaska Ultra 88E1111/88E1112 Gigabit Ethernet Transceivers are physical layer devices for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. They contain all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and CAT 5 unshielded twisted pair.

The 88E1111/88E1112 devices support the Gigabit Media Independent Interface (GMII), Reduced GMII (RGMII), Serial GMII (Gigabit Ethernet), the Ten-Bit Interface (TBI), and Reduced TBI (RTBI) for direct connection to a MAC/Switch port.

The 88E1111/88E1112 devices incorporate a 1.25GHz SERDES, which may be directly connected to a fiber-optic transceiver for 1000BASE-T/1000BASE-X media conversion applications. Additionally, the 88E1111/88E1112 devices may be used to implement 1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

The 88E1111/88E1112 devices use advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The devices achieve robust performance in noisy environments with very low power dissipation.

The Alaska Ultra 88E1111/88E1112 features include:

- 10/100/100BASE-T IEEE 802.3 compliant
- Support for GMII, TBI, RGMII, RTBI, and Gigabit Ethernet
- Integrated 1.25GHZ SERDES for 1000BASE-X fiber applications
- The 88E1112 device also supports 100BASE-FX
- Four RGMII timing modes
- Three energy detect modes as well as a low power COMA mode
- Three loopback modes for diagnostics
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- CRC checker, packet counter
- Automatic detection of fiber or copper media
- Virtual Cable Tester (VCT)
- Selectable MDC/MDIO interface or Two-Wire Serial Interface.

Test Equipment

The following sections describe the equipment used in the interoperability tests.

Spirent® SmartBits® 2000 Protocol Analyzer

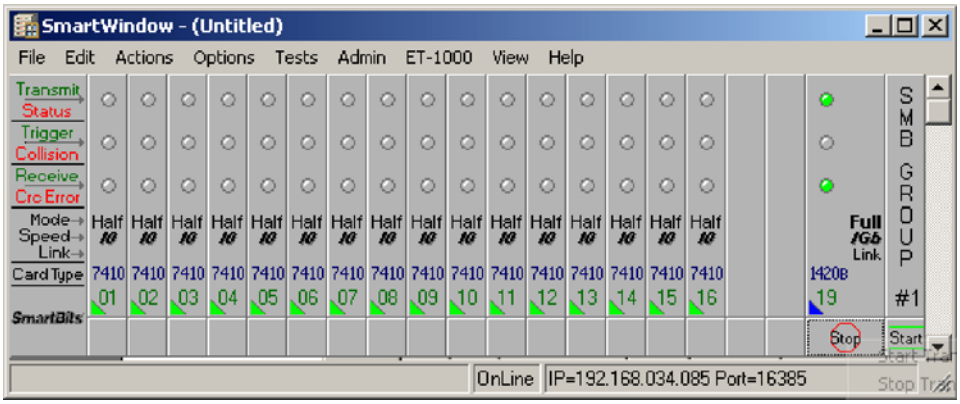
Spirent Communications' SmartBits 2000 (SMB-2000) has become the industry standard for measuring the performance limits of everything from an emerging technology in a development lab to the largest enterprise network. The SMB- 2000 is widely used to test a variety of network devices and complex network configurations, including 10/100 Mbps Ethernet, Gigabit Ethernet, ATM, and Frame Relay.

Figure 2 illustrates the SMB-2000 analyzer with a 1000BASE-T copper module (GX-1420B, right-most module with RJ45 cable attached).

Figure 3 illustrates the GUI command console for the SMB-2000. The GX-1420B module is also shown to the right of the screen.

Figure 2. SmartBits 2000 Protocol Analyzer with 1000BASE-T Module

Figure 3. SmartBits 2000 GUI Controls



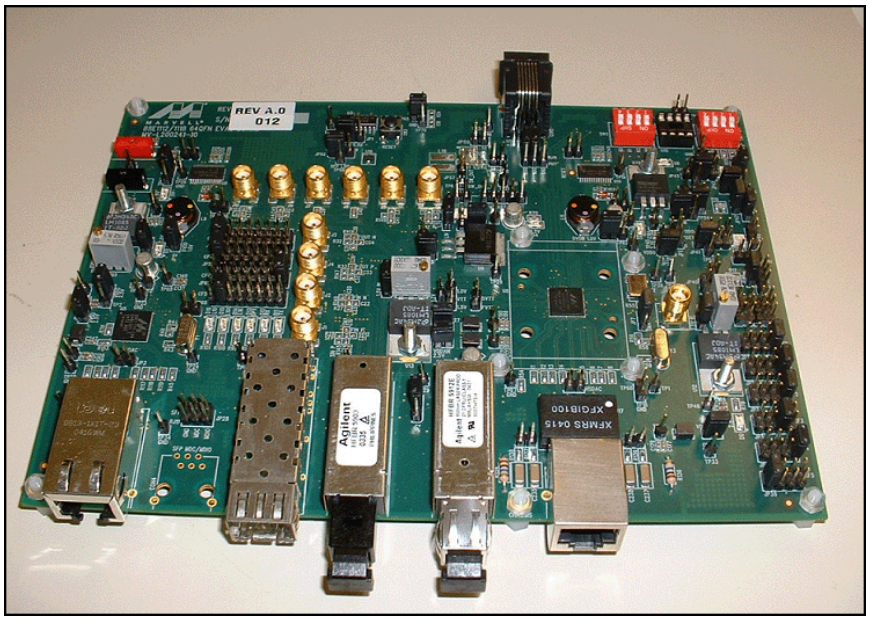
Marvell 88E1112 64-QFN Evaluation Board

The Marvell 88E1112 64-QFN Evaluation Board includes among others:

- 88E1111 device
- 88E1112 device
- On-board oscillator clock sources
- MDIO/MDC monitoring/control to both devices
- Gigabit Ethernet interface between the 88E1111 and the 88E1112
- RJ45 connector for MDI access to the 88E1111
- Two transmit SMAs and two receive SMAs for access to the 88E1112 SERDES

Figure 4 illustrates the 88E1112 64-QFN Evaluation Board.

Figure 4. Marvell 88E1112 64-QFN Evaluation Board



Marvell Alaska Virtual Cable Tester™ Software

The Alaska Virtual Cable Tester Software GUI controls the 88E1111/88E1112 parts and monitor status bits. Figure 5 shows the VCT GUI. The GUI is mainly used for 1000-BASE-T or 1000BASE-X modes.

In Gigabit Ethernet mode, the PHY Register Control Panel is used instead to control and monitor the 88E1112 registers. Figure 6 illustrates the Phy Register Control Panel.

Figure 5. Alaska Virtual Cable Tester Software GUI

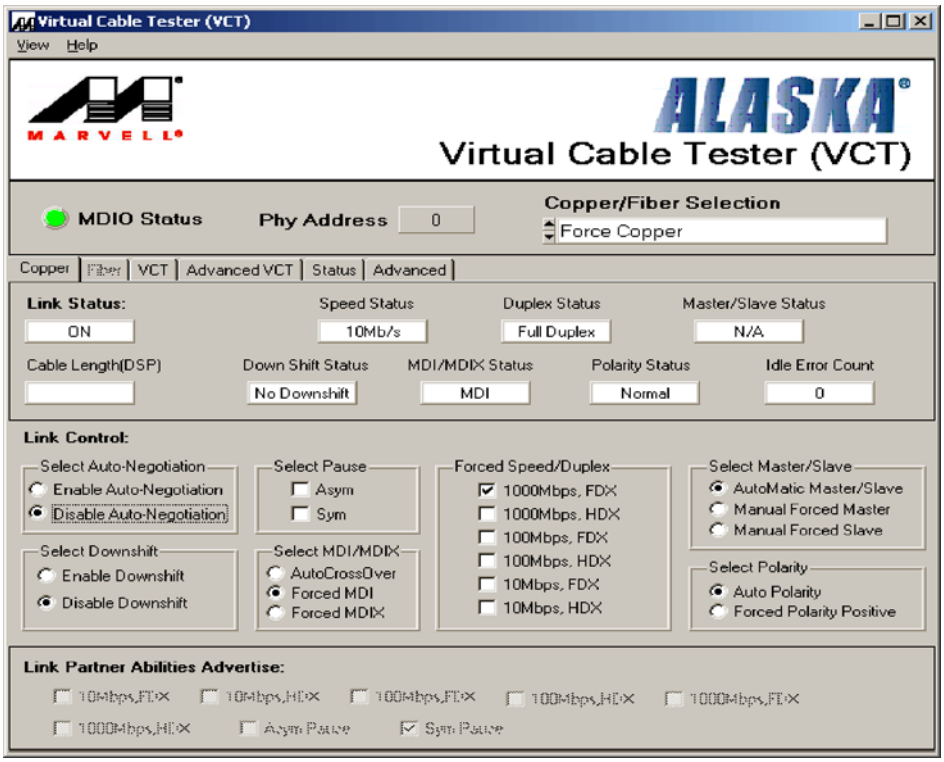
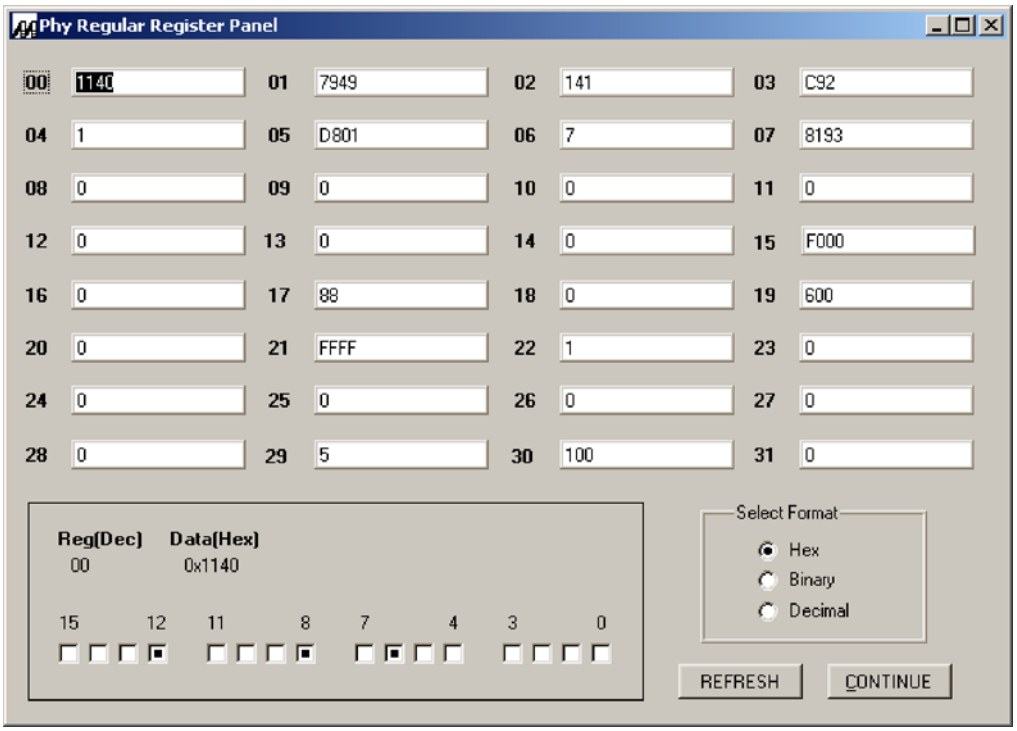


Figure 6. Phy Register Control Panel



Agilent 81130A Pulse/Data Generator

The Agilent 81130A pulse/data generator was used to supply an external 125 MHz reference clock source to the LatticeECP2M PCS.

For more information this module, please refer to the Agilent website at www.agilent.com.

LatticeECP2M SERDES Evaluation Board

The LatticeECP2M SERDES Evaluation Board features the LatticeECP2M LFE2M35-FF672 FPGA device. The stand-alone evaluation board provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces to PCI Express protocols.

The LatticeECP2M SERDES Evaluation Board includes provisioning to connect four high-speed SERDES channels via SMA connectors to test and measurement equipment. This interface is used to demonstrate XAUI type applications. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces. The board has several debugging and analyzing features for complete customer evaluations of the LatticeECP2M device.

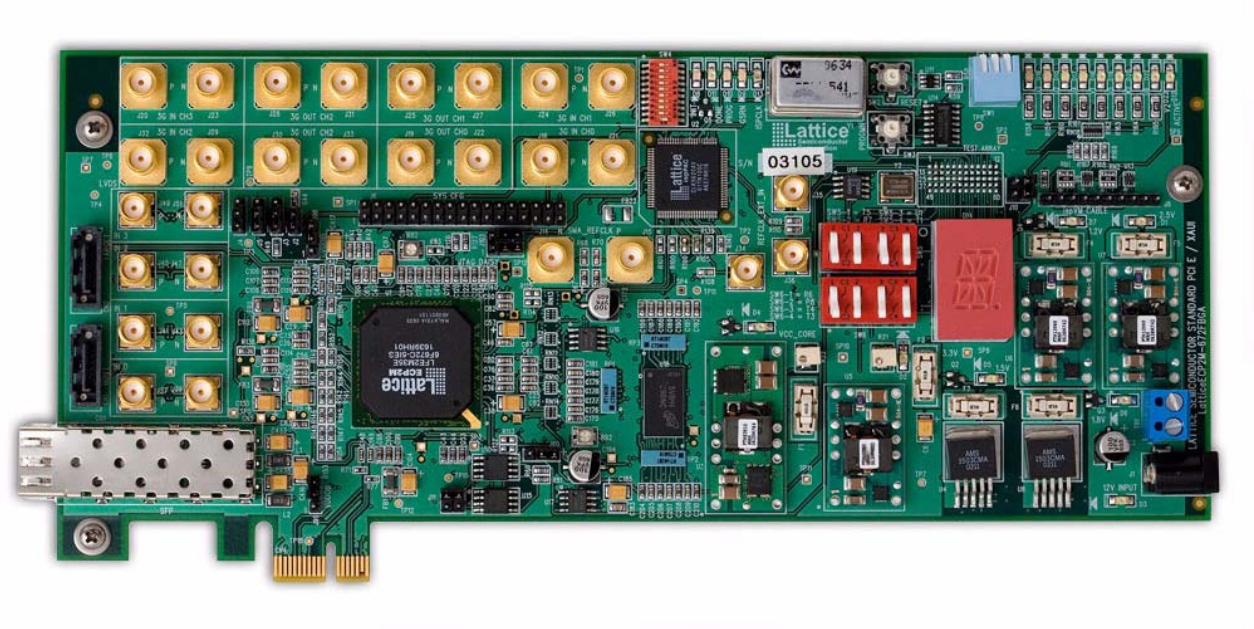
The board features:

- Four SERDES high-speed channels interfaced to SMA test points and clock connections SERDES interface to x1 PCI Express edge fingers
- DDR2 memory device
- SFP Transceiver cage and associated interface
- SATA-like connections to SERDES channels
- Power connections and power sources
- ispVM® programming support

- * On-board and external reference clock sources
  - Interchangeable clock oscillators
  - On-board reference clock management using Lattice ispClock™ devices
- ORCAstra Demonstration Software interface via standard ispVM JTAG connection
- Various high-speed layout structures

Figure 7 shows the LatticeECP2M evaluation board.

Figure 7. LatticeECP2M SERDES Evaluation Board



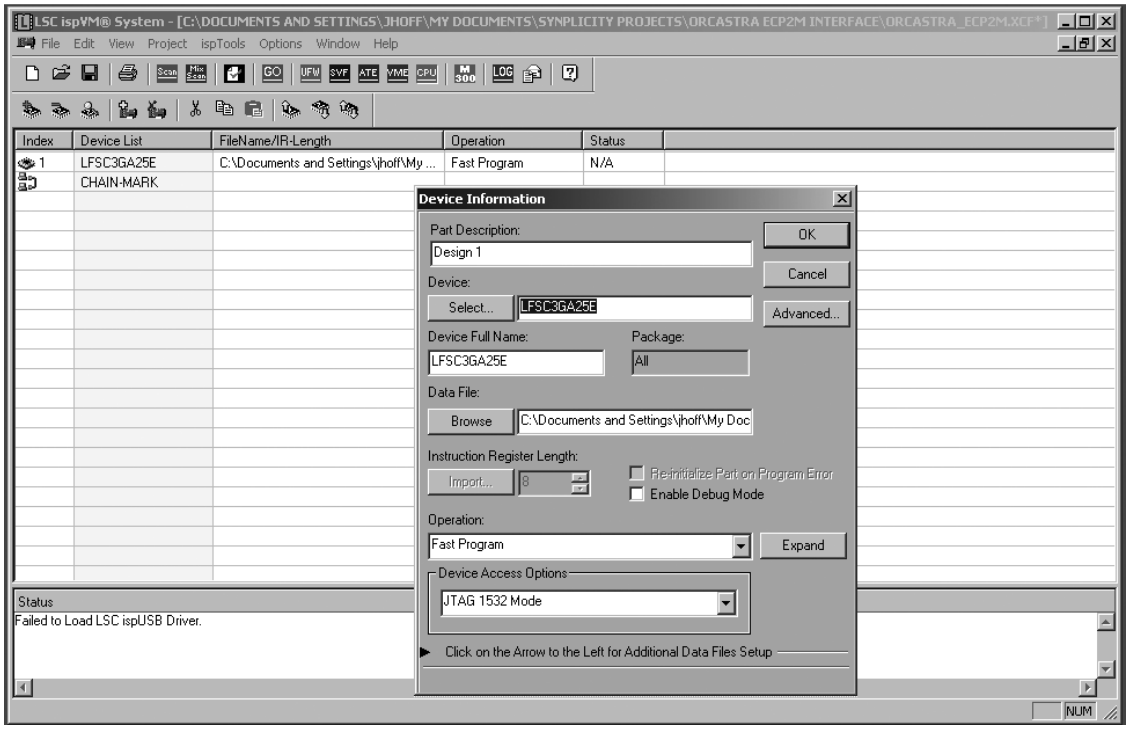
ispVM System

The ispVM System is included with Lattice's ispLEVER software and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice Semiconductor, and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeECP2M bitstream to configure the FPGA in Gigabit Ethernet mode.

Figure 8 shows an ispVM System screen shot.

Figure 8. ispVM System



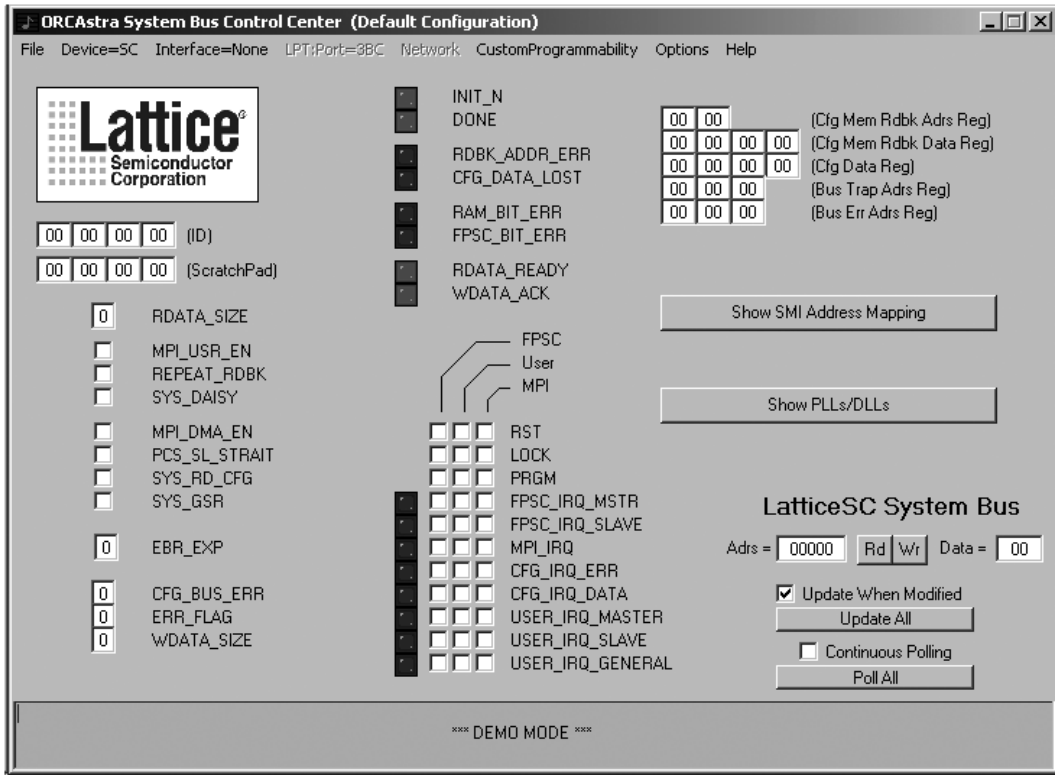
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA or FPSC by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the FPSC.

Figure 9 is an ORCAstra system screen shot.

Figure 9. ORCAstra System



Interoperability Testing

This section provides details on 1000BASE-X Gigabit Ethernet Physical Layer interoperability tests between the LatticeECP2M device and the Marvell 88E1111/ 88E1112 devices. The purpose of these tests is to confirm the correct processing of 1000BASE-T copper protocol from the SMB-2000, through the 88E1111/88E1112 devices, and ending at the LatticeECP2M GMII interface, and then back in the other direction. Particularly, the tests verify:

- The ability to auto-negotiate 1000BASE-X successfully
- The ability to transfer packets across the system in an asynchronous way

Test Setup

Figure 10 shows the board connections of the test setup. Figure 11 is a block diagram of the test setup.

The set-up includes:

- A Spirent SMB-2000 with a GX-1420B module
- The Marvell 88E1112 Evaluation Board (with the 88E1111/88E1112 devices)
- The LatticeECP2M SERDES Evaluation Board
- A PC for software control/monitoring
- The Agilent 811130A Data/Pulse Generator to provide an external 125 MHz reference clock to the LatticeECP2M PCS

Figure 10. Test Setup Board Connections

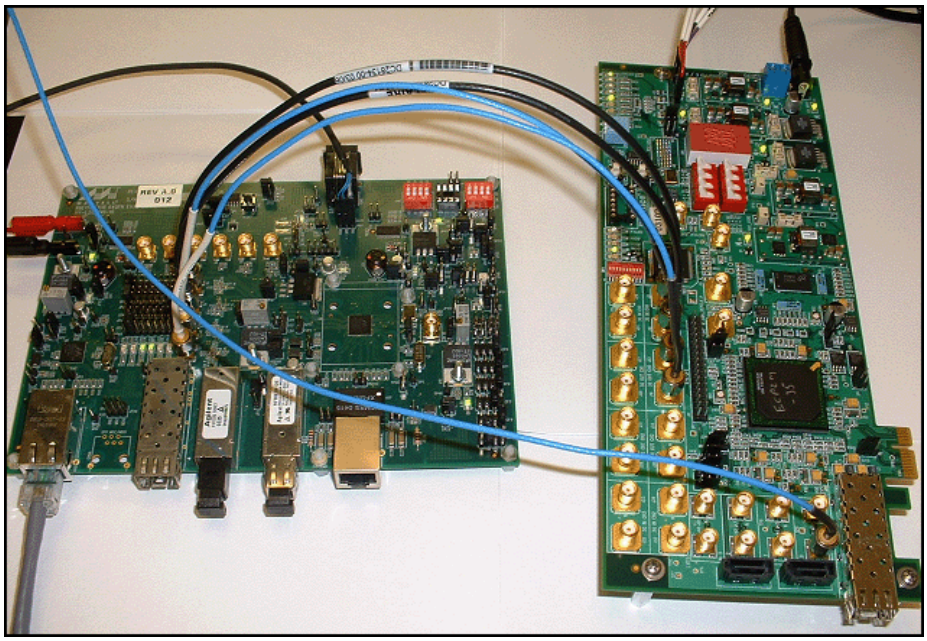
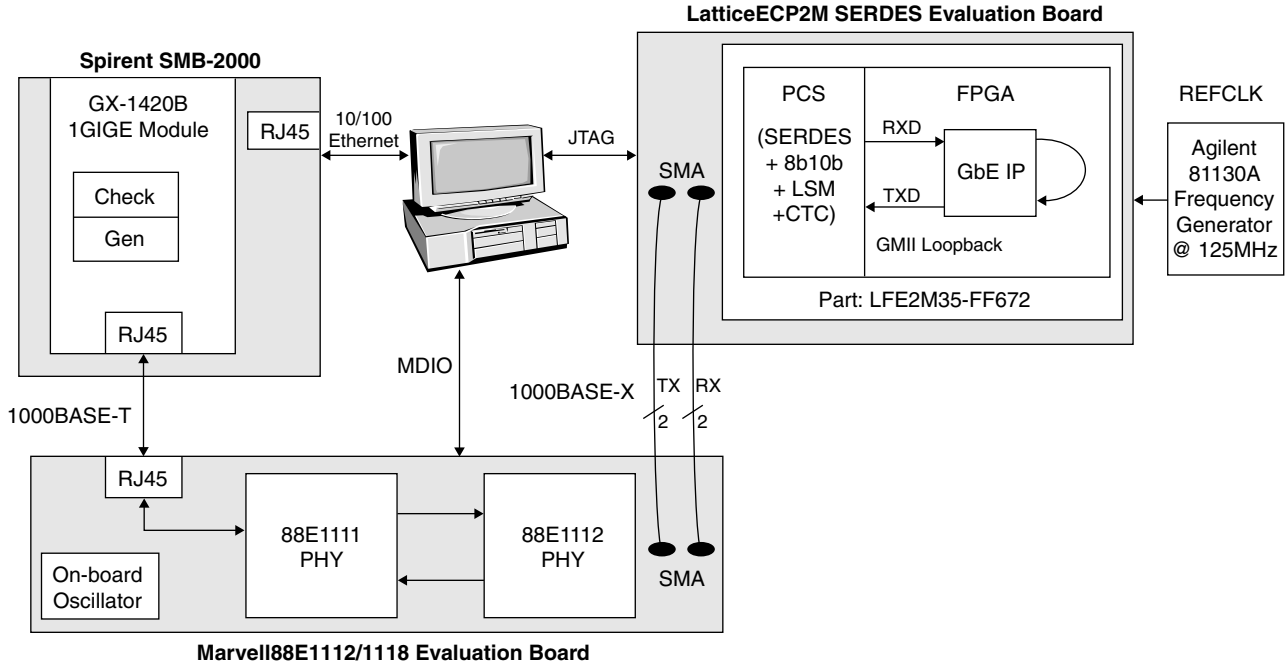


Figure 11. Test Setup Block Diagram



Test Description

This section describes how the Gigabit Ethernet Physical Layer Interoperability is achieved.

SMB-2000

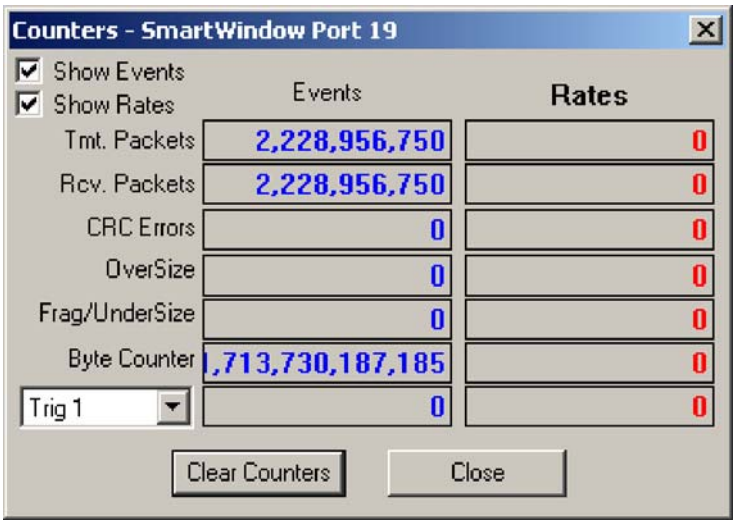
The GX-1420B module generates and checks full protocol compliant Gigabit Ethernet packets. The setup is as follows:

- Random source/destination addresses
- Random payload content
- Random payload length
- 0.096 µSec IPG GAP

Figure 12 illustrates the SMB-2000 counter window used to keep track of transmission and reception statistics.

The SMB-2000 connects to the Marvell 88E1112/ 88E1118 Evaluation Board via an RJ45 cable. It transmits the Gigabit Ethernet 1000BASE-T packets to the 88E1111 device in the TX direction, and checks them back from the 88E1111 device in the RX direction.

Figure 12. SMB-2000 Counter Window



Marvell 88E1112/88E111 Evaluation Board

In one direction, the 88E1111 device receives 1000BASE-T packets from the SMB-2000 and sends it to the 88E1112 device via its Gigabit Ethernet interface. In the other direction, the opposite flow of data occurs.

In one direction, the 88E1112 part receives Gigabit Ethernet packets from the 88E1111 and sends 1000BASE-X data to the LatticeECP2M board via SMAs on its Gigabit Ethernet interface. In the other direction, the opposite flow of data occurs.

The 88E1112 part also performs 1000BASE-X auto negotiation with the LatticeECP2M GbE IP solution.

LatticeECP2M Evaluation Board

In the RX direction, The LatticeECP2M PCS recovers 1000BASE-X Gigabit Ethernet packets from the 88E1112 device and the Gigabit Ethernet IP converts them into GMII format.

The GMII loopback logic in the FPGA portion loops the GMII data back into the TX direction. The LatticeECP2M device then transmits the 1000BASE-X Gigabit Ethernet packets back to the 88E1112 device.

The LatticeECP2M GbE IP also performs 1000BASE-X auto negotiation with the 88E1112 device.

Results

Correct auto-negotiation was verified by monitoring both the LatticeECP2M Gigabit Ethernet solution status signals and registers and the Marvell PHY Register Panel (see Figure 6).

The SmartBits SMB-2000 GX-1420B counter window (as shown in Figure 12) was monitored for error-free packet transmission and reception. Additionally, the Lattice ORCAstra System GUI was also monitored for proper link synchronization. The setup ran for over four hours, during which over two billion packets were transmitted/received error-free (see Figure 12).

Summary

In conclusion, the LatticeECP2M FPGA family offers users Gigabit Ethernet Physical Layer support and is fully inter-operable with Marvell 88E1111/88E1112 devices.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
July 2007	01.0	Initial release.