LatticeECP2/M Hardware Checklist

June 2013 Technical Note TN1162

Introduction

When designing complex hardware using the LatticeECP2/M FPGA, designers must pay special attention to critical hardware configuration requirements. This technical note steps through these critical hardware implementation items relative to the LatticeECP2/M device. The device family consists of FPGA LUT densities ranging from 6K to 100K. This technical note assumes that the reader is familiar with the LatticeECP2/M device features as described in the LatticeECP2/M Family Data Sheet.

The critical hardware areas covered in this technical note are:

- Power supplies as they relate to the LatticeECP2/M supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

Power Supplies

The V_{CC}, V_{CCIO8} and V_{CCAUX} power supplies determine the LatticeECP2/M internal “power good” condition. In addition to the three power supplies, there are $V_{CCIO0-7}$, V_{CCPLL} and V_{CCJ} supplies that power the I/O banks, PLL and JTAG port. All power supplies are required for proper device operation but since V_{CC}, V_{CCIO8} and V_{CCAUX} determine the device power-on condition, it is recommended that one of these supplies should be the final power supply to power up the LatticeECP2/M device after all other power supplies are stable. Table 18-1 shows the power supplies and the appropriate voltage levels for each supply.

Table 18-1. Power Supply Description and Voltage Levels

Supply	Voltage (Typical)	Description
V_{CC}	1.2V	Core power supply. A nominal trip point for Vcc power supply is 1.0V.
V_{CCAUX}	3.3V	Auxiliary power supply. A 3.3V supply that provides an internal reference to the input buffers. A nominal trip point for VCCAUX is 2.9V.
V_{CCPLL}	1.2V	Power supply for PLL. Available on larger devices only.
$V_{CCIO0-7}$	1.2V to 3.3V	I/O power supply. There are eight general purpose I/O banks and each bank has its own supply V_{CCIO0} - V_{CCIO7}.
V_{CCIO8}	1.2V to 3.3V	Configuration I/O bank power supply. A nominal trip point for V_{CCIO8} is 1.0V.
V_{CCJ}	1.2V to 3.3V	JTAG power supply for the TAP controller port.

LatticeECP2M SERDES/PCS Power Supplies

When using the SERDES with 1.5V VCCIB or VCCOB, the SERDES should not be left in a steady state condition with the 1.5V power applied and the 1.2V power not applied. Both the 1.2V and the 1.5V power should be applied to the SERDES at nominally the same time. The normal variation in ramp_up times of power supplies and voltage regulators is not a concern.

All VCCTX, VCCRX, VCCP and VCCAUX33 supply pins must always be powered to the recommended operating voltage range regardless of the SERDES use. When SERDES channels are not used, the required supplies can be connected to the standard FPGA 1.2V or 3.3V power supplies since the noise levels of these supplies are not critical. VCCIB and VCCOB could be left floating for unused SERDES channels. Unused channel outputs are tristated, with approximately 10 KOhm internal resistor connecting between the differential output pair.

VCCAUX33 supplies power to termination resistors. As a result, noise on VCCAUX33 is directly coupled with the high-speed I/O, HDIN/HDOUT. A clean FPGA core VCCAUX (power supply) can be used to supply the SERDES VCCAUX33. Unused SERDES channels are configured in power-down mode by default.

Table 18-2 shows the power supplies and the appropriate voltage levels for each supply.

Table 18-2. Power Supply Description and Voltage Levels

Supply	Voltage (Typical)	Description
V_{CCTX}	1.2V	Transmit power supply
V_{CCRX}	1.2V	Receive power supply
V_{CCP}	1.2V	PLL and reference clock buffer power
V_{CCIB}	1.2V/1.5V	Input buffer power supply
V_{CCOB}	1.2V/1.5V	Output buffer power supply
$V_{CCAUX33}$	3.3V	Termination resistor switching power supply

Power Supply Sequencing

There are three main power supplies that are required to power-up the LatticeECP2/M device for proper operation: V_{CC}, V_{CCAUX} and V_{CCIO8}. There is no specific power sequencing requirement for the LatticeECP2/M device family. If the user's system has the option to design for power sequencing, a practical sequencing is V_{CC} before V_{CCAUX} or V_{CCIO8}. V_{CC} should reach its minimum voltage value before V_{CCAUX} and V_{CCIO8} reach their minimum values. For the LatticeECP2/M "S" version only, V_{CC} must reach its valid minimum value before powering up V_{CCAUX}. Power sequencing considerations should also consider that common supplies are generally tied together to the same rail. For example, If there is a 3.3V V_{CCIO}, it should be tied to the same supply as the 3.3V rail for V_{CCAUX}, thus minimizing leakage.

Power Supply Ramp

For the LatticeECP2/M, it is important to make sure that the power supply ramp times stay within a reasonable range. Each power supply must follow a monotonically clean ramp between the trip points and the minimum required supply voltage. Slow power supply ramps in the tens of milliseconds to hundreds of milliseconds are critical to ensure that the transitions around trip points are monotonic.

Multiple transitions through the trip point may cause multiple internal power-on reset sequencing.

Power Estimation

Once the LatticeECP2/M device density, package and logic implementation is decided, power estimation for the system environment should be determined based on the software Power Calculator provided as part of the isp-LEVER® design tool. When estimating power, the designer should keep two goals in mind:

1. Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current or maximum DC and AC current for the given system's environmental conditions.
2. The ability for the system environment and LatticeECP2/M device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, LatticeECP2/M power requirements are taken into consideration early in the design phase.

Configuration

All LatticeECP2/M devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG™ port, which supports both byte-wide and serial configuration.

Table 18-3 shows the associated CFG pin definitions.

Table 18-3. Configuration Mode Selection

Configuration Mode	CF[2]	CFG[1]	CFG[0]	D[0]/SPIFASTN
SPI (Normal, 0x03)	0	0	0	Pull-Up
SPI (Fast, 0x0B)	0	0	0	Pull-Down
SPIm (Normal, 0x03)	0	1	0	Pull-Up
SPIm (Fast, 0x0B)	0	1	0	Pull-Down
Slave Serial	1	0	1	X
Slave Parallel	1	1	1	D0

The configuration port resides in I/O bank 8 and has dedicated/shared I/Os for configuration. Shared pins are available as a user I/O after configuration, if PERSISTENT is OFF.

V_{CCIO8} must match the supply voltage of the SPI Flash. For example, if the external SPI Flash operates at 3.3V, V_{CCIO8} must be tied to the 3.3V supply rail as well.

Table 18-4 lists the sysCONFIG pins. If any of these pins are used for configuration or user I/O, the designer must adhere to the requirements listed in TN1108, LatticeECP2/M sysCONFIG Usage Guide.

Table 18-4. Configuration Pin Descriptions

Pin Name	I/O Type	Pin Type	Description
CFG[2:0]	Input, weak pull-up	Dedicated	FPGA configuration mode selection
PROGRAMN	Input, weak pull-up	Dedicated	FPGA Configuration control and status signals
INITN	Bi-Directional Open Drain, weak pull-up	Dedicated	
DONE	Bi-Directional Open Drain with weak pull-up or Active Drive	Dedicated	
CCLK	Input or Output	Dedicated	Configuration clock
DI/CSSPI0N	Input, weak pull up	Dual-purpose	SPI control and data signals
DOUT/CSON	Output	Dual-purpose	
CSN	Input, weak pull up	Dual-purpose	
CS1N	Input, weak pull up	Dual-purpose	
WRITEN	Input, weak pull up	Dual-purpose	
BUSY/SISPI	Output, tri-state, weak pull-up	Dual-purpose	
D[0]/SPIFASTN	Input or Output, weak pull-up	Dual-purpose	
D[1:6]			
D[7]/SPID0			
TDI	Input, weak pull-up	Dedicated	JTAG
TDO	Output, weak pull-up		
TCK	Input with Hysteresis		
TMS	Input, weak pull-up		

JTAG Interface

The JTAG interface pins are referenced to V_{CCJ}. Typically, JTAG pins are referenced to a 3.3V supply. V_{CCJ} can support supplies from 1.2V to 3.3V. In cases where V_{CCJ} is connected to supplies other than 3.3V, validate that the JTAG interface cable or tester can support an I/O interface with the same I/O voltage standard.

I/O Interface and Critical Pins

There are nine I/O banks on every LatticeECP2/M device. V_{CCIO8} is the configuration I/O bank and as such, the configuration requirements should have the highest priority to determine the supply voltage levels.

I/O Pin Assignments Around V_{CCPLL}

The V_{CCPLL} provides a “quiet” supply for the internal PLLs. For the best PLL jitter performance, careful pin assignment will keep “noisy” I/O pins away from “sensitive” pins, as shown in the BGA ball locations identified in Figure 18-1. In this case, the sensitive pin is one of the V_{CCPLL} supply pins. The noisy”I/O pins generally have the highest switching frequency, the highest V_{CCIO} standard and the fastest output slew rates. For example, using Figure 18-1, one can identify the “keep out” ball locations for potentially noisy signals.

Figure 18-1. “Quiet” Pin Assignment Considerations for BGA Packages

5x5	5x5	5x5	5x5	5x5
5x5	3x3	3x3	3x3	5x5
5x5	3x3	Sensitive Pin	3x3	5x5
5x5	3x3	3x3	3x3	5x5
5x5	5x5	5x5	5x5	5x5

PLLCAP

An optional external capacitor can be used with both EXHPLLD and EPLLD to change the frequency response of the on-chip loop filter. When an external capacitor is used, it allows the PLLs to extend the low-end of their operating ranges. IPexpress™ checks the phase detector frequency to determine if an external capacitor is required. The allowable ranges for the PLL parameters with and without the external capacitor are described in the LatticeECP2/M Family Data Sheet.

Recommended optional external capacitor specifications:

- **Value:** 5.6 nF, +/- 20%
- **Type:** Ceramic chip capacitor, NPO dielectric
- **Package:** 1206 or smaller

Each device has two external capacitor pins, one for the left-side PLLs and one for the right-side PLLs. These pins are in fixed locations. They are dedicated function pins that are NOT shared with user I/Os. When an external capacitor pin is used by a PLL on one side of the device, it cannot be used by any other PLLs on the same side of the device. This means that a maximum of two PLLs per device, one on the left side and one on the right side, can have external capacitors attached.

Placing the capacitors at the PLLCAP pins only affects the PLL response when the software enables this feature. This allows a designer to provide the capacitors (or unpopulated PCB pads) to the PLLCAP pins to utilize the lower PLL frequencies if it becomes necessary for future changes to the design.

DDR/DDR2 Memory Interface Pin Assignments

The DDR Memory interface on the LatticeECP2/M device family is provided with a pre-engineered I/O register along with the precision I/O DLL timing control. There are two I/O DLLs specifically assigned to the two halves of the device. One I/O DLL supports I/O banks 2, 3 and 4; another I/O DLL supports I/O banks 5, 6 and 7.

In addition to the I/O DLL assignments, there are pre-defined data strobe (DQS) signals that can support a span of I/O pins as part of the memory data lanes. When assigning DDR memory interface I/O pins, the FPGA designer must insure that there are enough I/O pins to assign DDR memory data pins for each of the assigned DQS signals.

When interfacing to the DDR memory, the I/O type used is SSTL18 for DDR2 memory or SSTL25 for the DDR1 memory interface. The VREF required for these SSTL buffers should be assigned to VREF1 of the bank.

True-LVDS Output Pin Assignments

True-LVDS outputs are available on 50% of the I/O pins on the left and right sides of the device. The left- and right-side I/O banks are banks 2, 3, 6 and 7. When using the LVDS outputs, a 2.5V supply must be connected to these V_{CCIO} supply rails.

HSTL and SSTL Pin Assignments

These externally referenced I/O standards require an external reference voltage. Each of the LatticeECP2/M device family I/O banks allow up to two pre-defined V_{REF} pins. The V_{REF} pin(s) should get the highest priority when assigning pins.

PCI Clamp Pin Assignments

In LatticeECP2 devices, only the I/Os on the bottom banks have programmable PCI clamps. In LatticeECP2M devices, the I/Os on the left and bottom banks have the programmable PCI clamps. When the system design calls for a PCI clamp, those pins should be assigned to I/O banks 4 and 5 for LatticeECP2 and banks 4, 5, 6 and 7 for LatticeECP2M. For clamp characteristics, refer to the IBIS buffer models either on the Lattice website or ispLEVER design tool.

Checklist

	LatticeECP2/M Hardware Checklist Items	OK	N/A
1	**Power Supply**		
1.1	Core Supply VCC @1.2V		
1.2	Auxiliary Supply VCCAUX @3.3V		
1.3	PLL Supply VCCPLL @1.2V		
1.4	JTAG Supply VCCJ from 1.2V-3.3V		
1.5	I/O Supply VCCIO0-8 from 1.2V-3.3V		
1.6	10K +/-1% Pull down on XRES		
1.6	Supply Sequencing considerations		
1.7	Supply Ramp considerations		
1.8	Power Estimation		
1.9	Capacitor on PLLCAP pins (optional if using lower PLL frequencies)		
2	**Configuration**		
2.1	Consistency of VCCIO8 Supply when external SPI Flash is used		
2.2	Configuration control and status selections		
2.2.1	Pull-up or Pull-down on CFG2, CFG1, CFG0		
2.2.4	Pull-up on PROGRAMN, INITN, DONE		
2.2.5	Pull-up or pull-down on SPIFASTN (SPI mode)		
2.2.5	Pull-down on TCK		
2.2	JTAG Supply and default logic levels		

Checklist (Continued)

	LatticeECP2/M Hardware Checklist Items	OK	N/A
3	**I/O Pin Assignments**		
3.1	I/O pin assignments around VCCPLL		
3.2	DDR Memory pin assignment considerations		
3.3	True-LVDS pin assignment considerations		
3.4	HSTL and SSTL pin assignment considerations		
3.5	PCI clamp requirement considerations		
4	**LatticeECP2M SERDES**		
4.1	Transmitter power supply VCCTX@1.2V		
4.2	Receiver power supply VCCRX@1.2V		
4.3	TXPLL & reference clock buffer power VCCP@1.2V		
4.4	VCCIB & VCCOB (floating if Serdes are not used)@1.2V/1..5V		
4.5	Termination resistor switching power supply VCCAUX33@3.3V		

Technical Support Assistance

e-mail: techsupport@latticesemi.com

Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
July 2007	01.0	Initial release.
September 2007	01.1	Updated Power Supply Sequencing text section.
June 2013	01.2	Updated document with new corporate logo.
		Updated Technical Support Assistance information.