LatticeECP2M PRBS SERDES Demo User's Guide

June 2010 Technical Note TN1153

Introduction

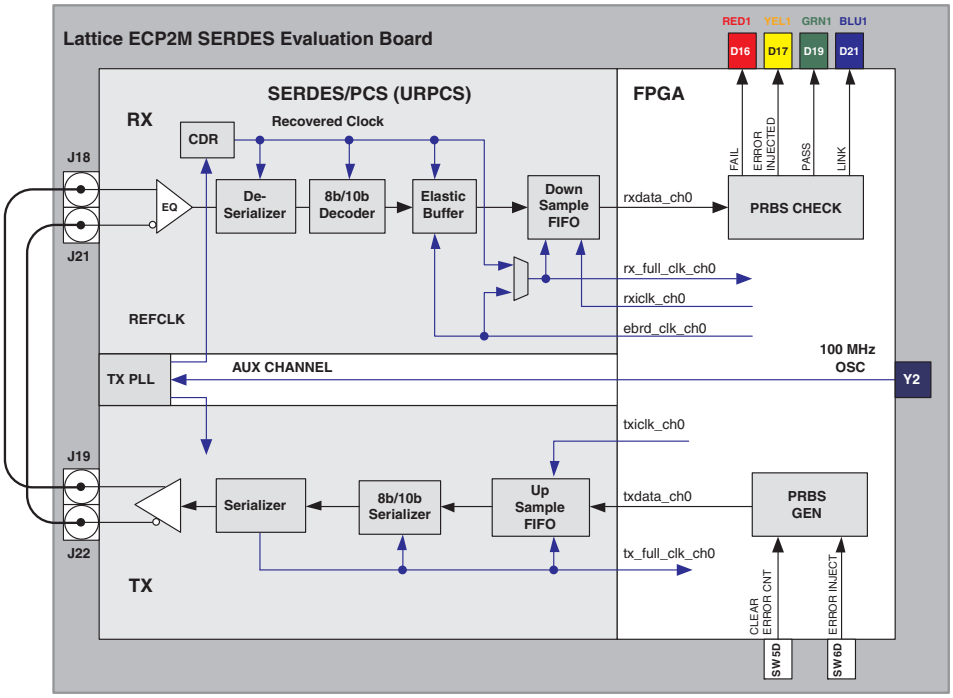
This demo illustrates the SERDES/PCS abilities of the LatticeECP2M™ FPGA family. It does this by embedding a simple pseudo-random pattern into an 8b10b-encoded PCS payload, then looping back the payload, and checking it for correctness. For this demo, the user will need:

- LatticeECP2M SERDES Demo Kit – Available in zip file format and can be downloaded free-of-charge at www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2mserdesevaluationboar.cfm
- LatticeECP2M SERDES Evaluation Board – With LFE2M-50E target device
- 12V power supply for the evaluation board (comes with the board)
- ispDOWNLOAD® cable (comes with the board)
- ispLEVER® 7.2 software (or later)
  Note: See Appendix A if you are using Lattice Diamond™ design software
- Lattice ispVM™ System software
- Two high quality coaxial data cables with SMA connectors – to be used for serial data loopback

Overview

This demo uses a pseudo-random bit stream (PRBS) generator to create a bitstream. The data is fed into the LatticeECP2M's PCS block as transmit payload. The PCS then 8b10b-encodes the data and transmits it out the LatticeECP2M's SERDES channel 0, where it is looped back. The data is received on channel 0, 8b10b-decoded in the PCS, then checked for correctness by the PRBS checker. Figure 1 shows the flow of the data and controls within the LatticeECP2M device and the LatticeECP2M SERDES Evaluation Board.

Figure 1. LatticeECP2M PRBS SERDES Demo Data/Control Flow



Component Descriptions

RESET Generator (txrx_reset_sm)

This module generates reset signals used in the SERDES/PCS block and FPGA logic. The correct reset sequence is critical in some designs where initial data values are used. For detailed information on reset sequence, please refer to TN1124, LatticeECP2M/SERDES PCS Usage Guide.

DPROM_256X9

This module stores idle patterns. The 256 x 9 (one bit is for the k_cntrl bit) data pattern is transmitted before the PRBS starts. The receiver uses the pattern to lock to incoming data and start CDR (Clock and Data Recovery).

PRBS Generator

The pseudorandom bit stream (PRBS) generator is a Verilog module that specifies a linear feedback shift register (LFSR). The PRBS generator uses a 7-bit polynomial (X7 + X6 +1) with an 8-bit interface to generate the bit sequence that is fed into the PCS. The sequence length is an optimal 127 (2^7 -1) patterns long. The PRBS generator can inject errors into the pattern sequence based upon the error_inject flip switch position.

PRBS Checker

The PRBS checker receives the pattern sequence from the PCS and checks it for correctness. The checker is, in essence, a pre-loaded LFSR that has the same polynomial as the generator. After reset, the checker is preloaded with the incoming sequence. A short time later, the checker is automatically enabled and it begins predicting the incoming sequence. If it detects a mismatch, the checker increments an error counter. If the error count is zero, then the PRBS checker drives the pass_LED. If the error count is non-zero, then the checker illuminates the fail_LED. The user can clear this error counter (thereby extinguishing the fail_LED and lighting the pass_LED) by cycling on the clr_error_cnt switch.

PCS

The Physical Coding Sublayer (PCS) performs the 8b10b encoding and serialization for the transmitted PRBS data. Likewise, 8b10b decodes and de-serializes the looped-back data. The PCS is configured for generic 8b10b SERDES, with only channel 0 enabled. The PCS is also configured for a 10x full clock rate. The SERDES bit clock rate is targeted for 1 GHz, which requires a 100 MHz reference clock. The on-board oscillator, Y2, is used as the reference clock source.

Note that in an original design effort, all of the PCS configuration parameters are available to the user via the Lattice IPexpress™ GUI. TN1124, LatticeECP2M/SERDES PCS Usage Guide, describes in detail on how to generate a PCS module in the IPexpress GUI.

DIV2

A PLL is used to generate a refclk divided-by-2 clock. This clock is used for various counters in the Reset State Machine.

Simulation Considerations

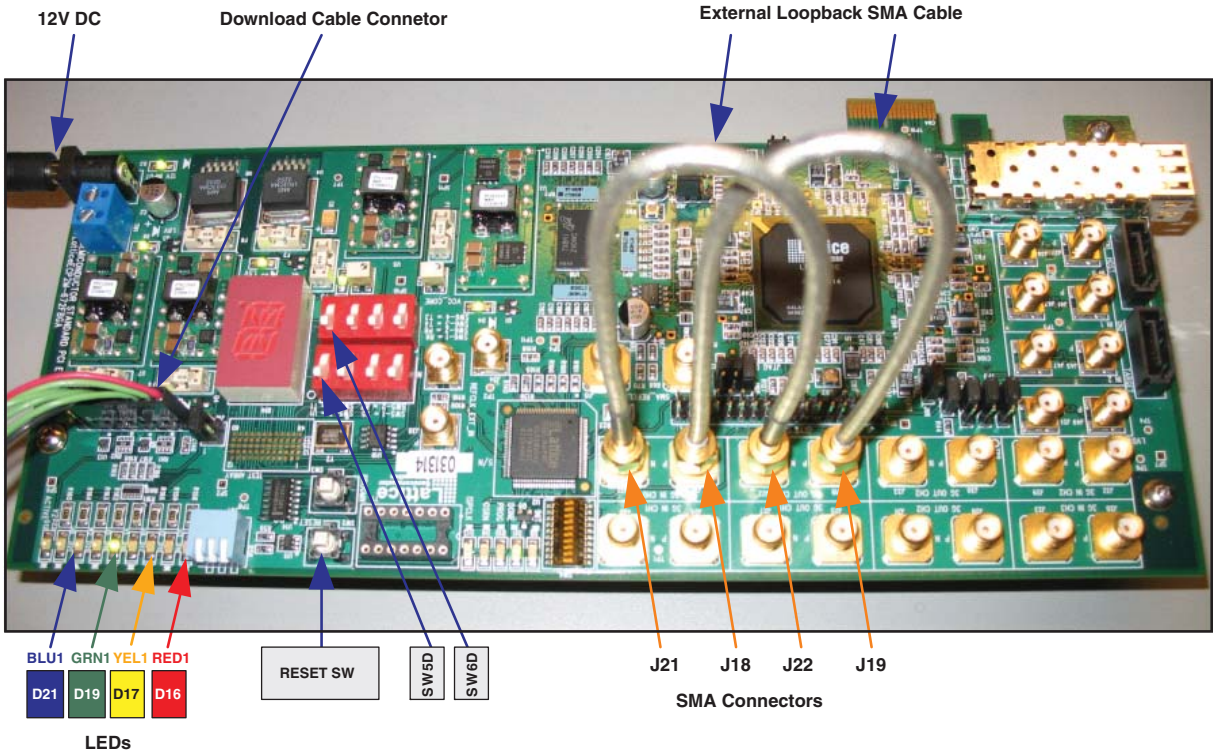
- A testbench is provided for simulation.
- The Aldec® Active-HDL® Lattice Edition simulator is used.
- The reset_generator module uses the idef attribute to distinguish synthesis and simulation.
- The behavioral functional simulation works with this reset_generator module.
- If users wish to run post-route simulation, the synthesis section of the reset_generator module must be removed.

Programming Instructions

1. Unzip the design into an appropriate design directory.
2. Start ispLEVER and open the design.
3. Generate the bitstream file. In ispLEVER Project Navigator, go to the **Processes** for current source pane and double-click on **Generate Bitstream Data**. ispLEVER will then go through the Build Database, Map Design, and Place and Route phases before generating the bitstream data.

Figure 2 shows the LatticeECP2M SERDES Evaluation Board configured for PRBS loopback on channel 0. The board is shown in a pass condition. Note that the activity and pass LEDs are both on while the fail LED and error_inject LEDs are both off. Also note that all flip-switches are in the off position (up).

Figure 2. LatticeECP2M SERDES Evaluation Board Configured for PRBS Loopback on Channel 0



For a detailed explanation of the PCS block and its configuration, see TN1124, LatticeECP2M/SERDES PCS Usage Guide.

For the following steps, please refer to Figures 1 and 2 for illustration.

4. **Connect the cables for external SERDES loopback.** Since the SERDES signaling is differential, there will be two coaxial cables to connect for the single channel. Connect J19 to J18 and J22 to J21.
5. **Connect the programming cable.** Connect the ispDOWNLOAD cable between your download computer and the LatticeECP2M SERDES Evaluation Board. The connection point on the board is a series of 10 pins labeled "ispVM CABLE". This connection is shown in Figure 2, but not in Figure 1. For details on this connection, please see the *LatticeECP2M SERDES Evaluation Board User's Guide.*
6. **Connect the power connector.** Be sure to use the 12V DC supply that came with the LatticeECP2M SERDES Evaluation board. Some LEDs should light up on the evaluation board.

7. **Start the ispVM System software**.

8. This demo uses Flash memory, U12, mounted on the circuit side of the board. In the main window (Figure 3) under **Edit**, select **Add Device** from the pull-down list. This will open the Device Information window (Figure 4).

Figure 3. ispVM Main Window

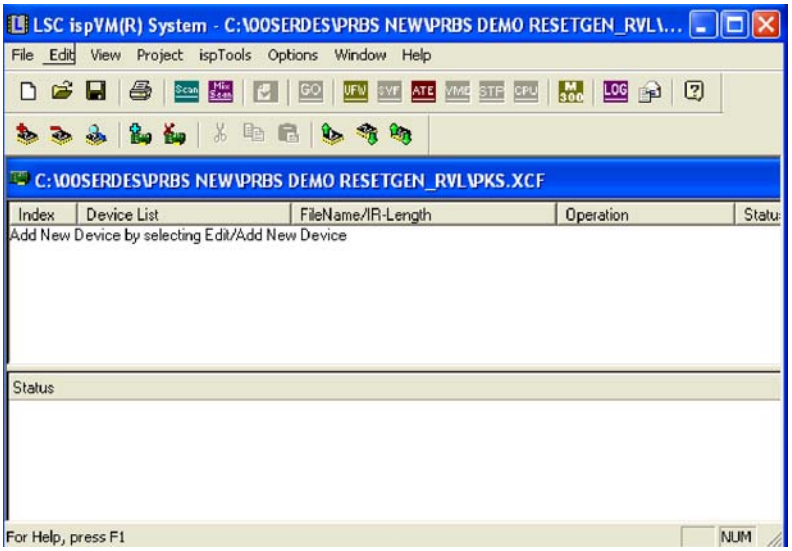
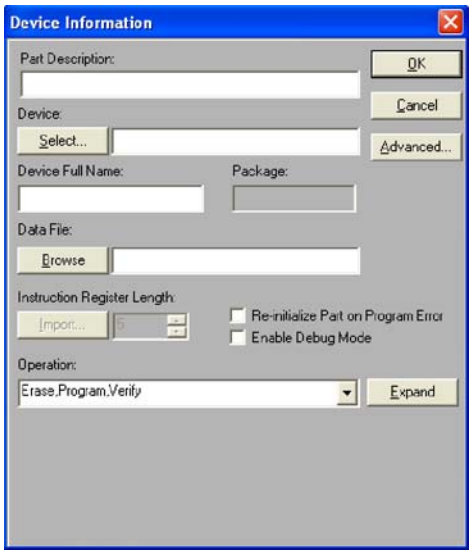
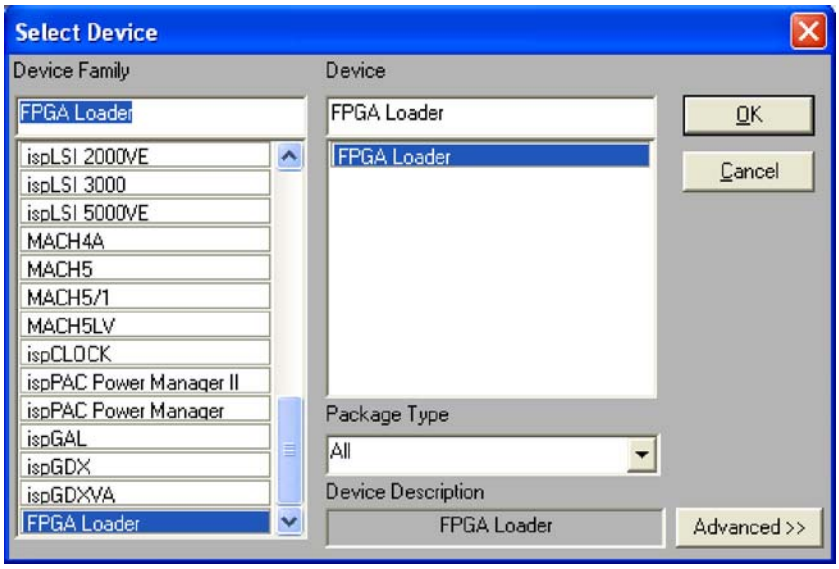


Figure 4. Device Information Window



9. In the Device Information window, click **Select**. This will open the **Select Device** window (Figure 5).

Figure 5. Select Device Window



10. Select **FPGA Loader** and click **OK**. This will open the FPGA Loader window (Figure 6).
11. Select **CPLD or FPGA Device** in the FPGA Loader window. This will bring up the Device Selection window on the right side (Figure 7).

Figure 6. FPGA Loader Window

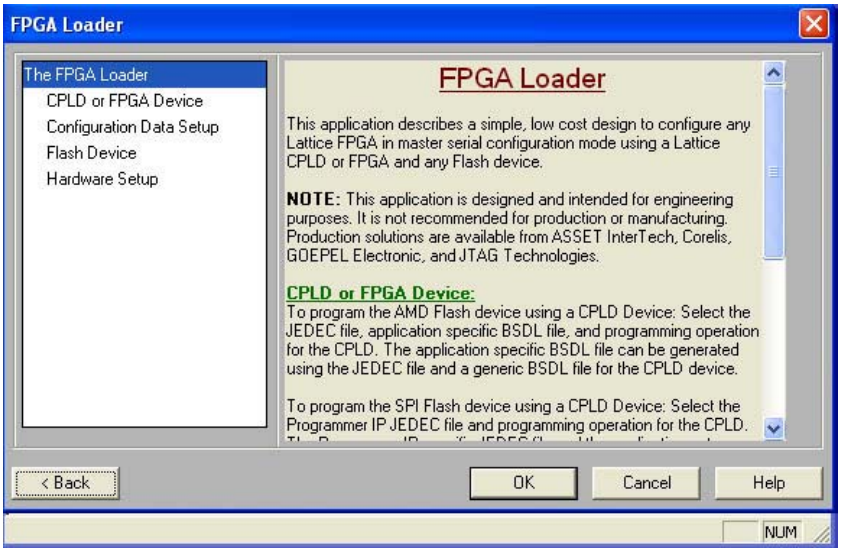
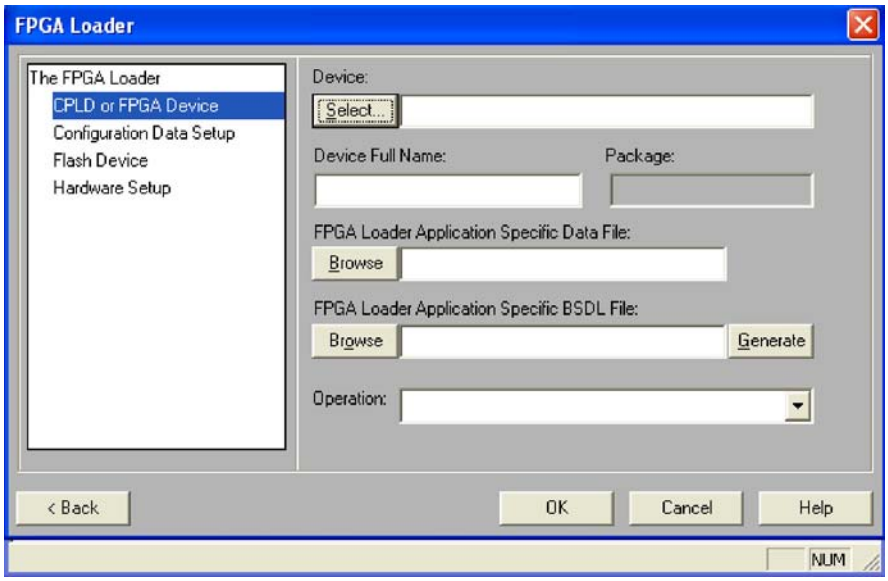
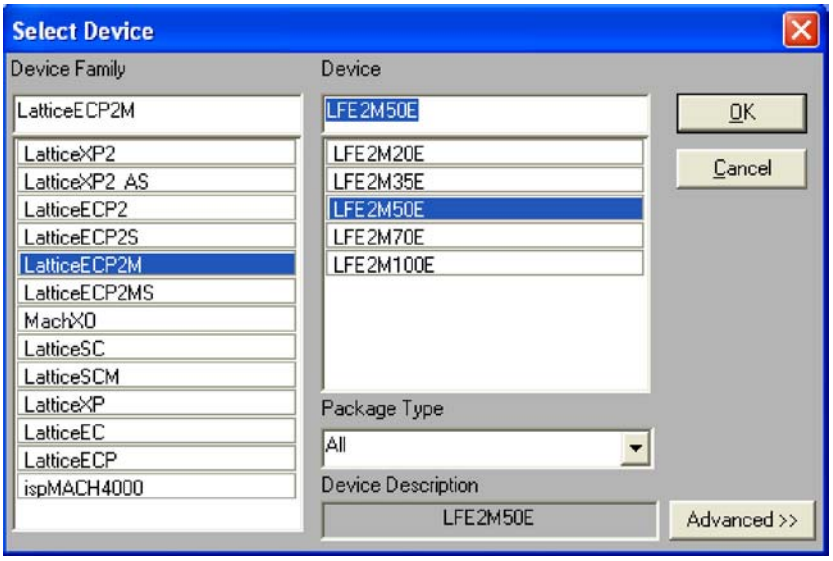


Figure 7. FPGA Loader Window (Click Select for CPLD or FPGA Device Selecion)'



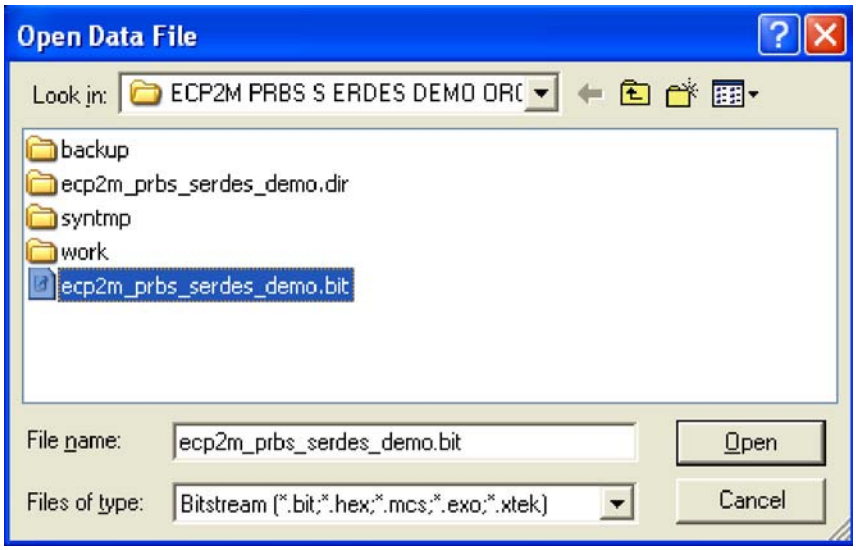
12. Select LatticeECP2M and LFE2M50E, as shown in Figure 8.

Figure 8. Select Device Window



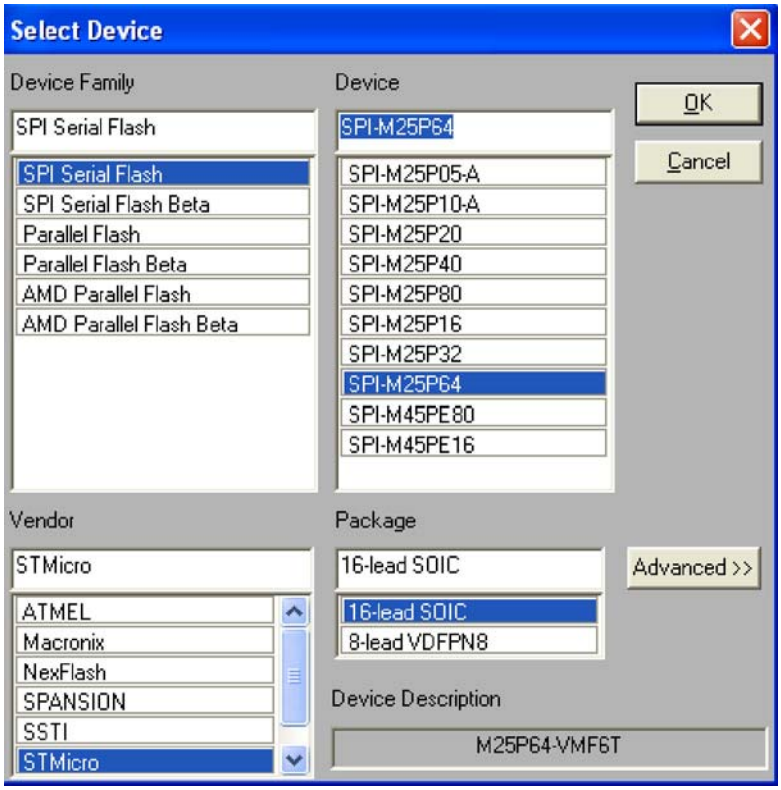
13. Click **OK**. Select **Configuration Data Setup** in the FPGA Loader window. The Open Data File window will open (Figure 9). Select the bit file from the directory and click **Open**.

Figure 9. Open Data File Window



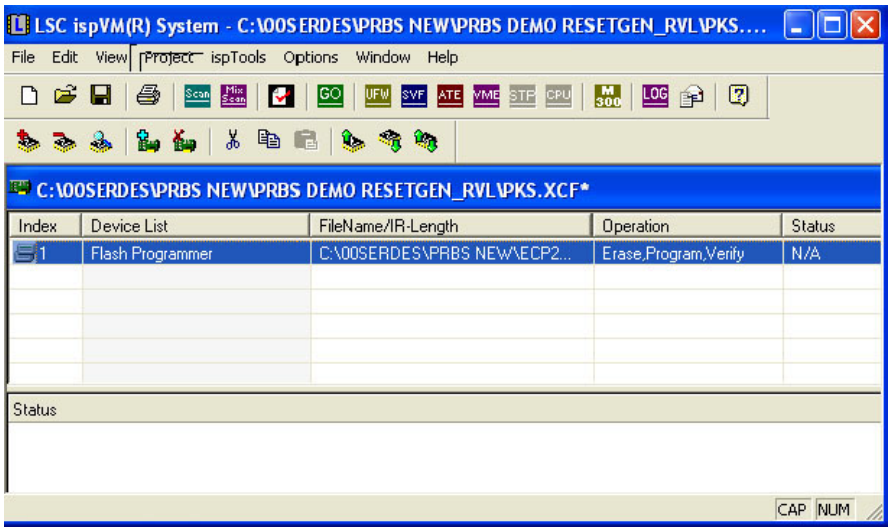
14. Select **Flash Device** in the FPGA Loader window (Figure 10). Select **SPI Serial Flash**, **STMicro** and **SPI-M25P64**, as shown.

Figure 10. Select Device Window



15. Click **OK**. The ispVM System main window will look like Figure 11.

Figure 11. ispVM Main Window



16. Click the green **GO** button and programming begins.

Running the Demo

At power up, it takes about 6 seconds to download the bitstream from on-board Flash memory to configuration memory. Refer to Figure 2 for the discussion below.

LED descriptions:

- **BLU1 (Activity LED)** – This LED will flash at approximately one-second intervals when a receiver link is established successfully.
- **GRN1 (Pass LED)** – This LED stays on when received PRBS data is good.
- **YEL1 (Error Inject LED)** – This LED turns on when SW6D is switched to the on position. SW6D injects error bits in txdata.
- **RED1 (Fail LED)** – This LED turns on when received PRBS data is different than transmitted data.

Switch descriptions:

- **SW6D** – Flipping this switch to the on position (the opposite of what is shown in Figure 2) will inject error bits in the transmit data.
- **SW5D** – Flipping this switch to the on position will clear the error counter register.

Steps:

1. At power up, after about 6 seconds, the BLU1 LED will flash and the GRN1 LED will stay on.
2. Flip SW6D to the on position. This will turn on the YEL1 LED, indicating an error has been injected. Also, the RED1 LED will turn on, indicating that the received data includes error bits.
3. Flip SW6D to the off position. This will turn off the YEL1 LED, indicating error injection has stopped. The RED1 LED will stay on.
4. Flip SW5D to the on position. This will turn the RED1 LED off, indicating that the error counter register has been cleared and will stay cleared.

5. Flip SW5D to the off position. This will not change any LED status but returns the error counter to normal operation.

6. Users may disconnect/connect the external loopback cable to emulate the error injection.

   Note: In general, disconnecting one cable may not be enough to generate an error. The differential link is robust enough to work with a single cable most of the time. When the link is broken, the BLU1 LED stops flashing. Use RESET SW to re-start the demo.

References

- EB25 - LatticeECP2M SERDES Evaluation Board User's Guide
- LatticeECP2M SERDES Evaluation Board web page, Lattice Semiconductor Corporation, www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2mserdesevaluationboar.cfm
- DS1006 - LatticeECP2M Family Data Sheet
- TN1124 - LatticeECP2M/SERDES PCS Usage Guide

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
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e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
May 2007	01.0	Initial release.
May 2008	01.1	Target device changed to LFE2M-50E. Simulation example added. Code changed for continuous PRBS stream.
August 2008	01.2	Reset Sequence module added.
		ORCAstra interface information added.
December 2008	01.3	Simulation Considerations text section added.
		Design package updated to ispLEVER 7.2.
August 2009	01.4	Added Running the Demo text section.
June 2010	01.5	Removed LatticeECP2M ORCAstra text section.
		Added Appendix A.

Appendix A. Lattice Diamond Usage Overview

This appendix discusses the use of the Lattice Diamond design software with the LatticeEPC2M PRBS SERDES demo.

The example code, available at:

www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2mserdesevaluationboar.cfm

includes both an ispLEVER project and a Lattice Diamond project. The bit files of both projects are essentially same.

You can begin with the ispLEVER project and follow the processes below to create a Lattice Diamond project.

1. Importing an ispLEVER design project to Lattice Diamond
2. Adjusting the PCS Module
3. Re-generating the PCS Module
4. Using IPexpress with Lattice Diamond
5. Creating a New Simulation Project using the Simulation Wizard

All of these processes are done in the Lattice Diamond project included.

For detailed information on the processes listed above, see the Lattice Diamond Help System or Appendix E of TN1124, LatticeECP2M SERDES/PCS Usage Guide.