

Introduction

The memory in the LatticeXP2™ FPGAs is built using Flash cells, along with SRAM cells, so that configuration memory can be loaded automatically at power-up, or at any time the user wishes to update the device. In addition to “instant-on” capability, on-chip Flash memory greatly increases design security by getting rid of the external configuration bitstream; while maintaining the ease of use and reprogrammability of an SRAM-based FPGA.

The LatticeXP2 supports the use of an encryption key to protect the contents of the Flash memory for additional security. The LatticeXP2 also supports the use of a One-Time-Programmable (OTP) feature to protect the Flash memory from being erased or re-programmed.

While an external device is not required, the LatticeXP2 does support several external configuration modes. The available external configuration modes are:

- Slave SPI
- Master SPI
- ispJTAG™ (1149.1 interface)

This guide will cover all the configuration options available for the LatticeXP2.

Programming Overview

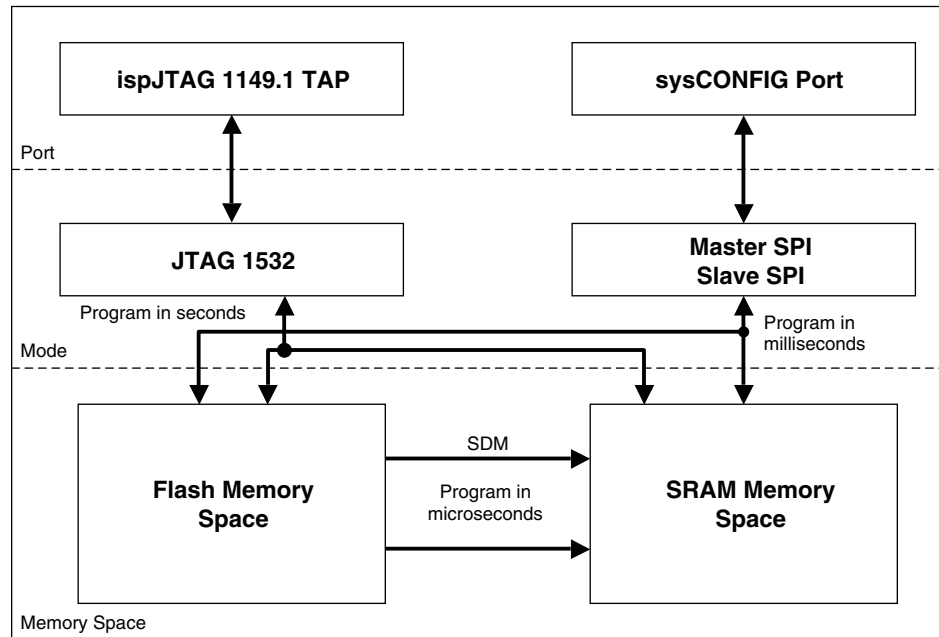
The LatticeXP2 contains two types of memory, SRAM and Flash (refer to Figure 14-1). SRAM contains the FPGA configuration, essentially the “fuses” that define the circuit connections; Flash provides an internal storage space for the configuration data.

The LatticeXP2 also contains additional Flash memory area and that is designated for Tag memory and User Flash memory. The Tag memory is a scratch pad memory that is available to the user for storage of mission critical data, board serialization, revision information, programmed pattern identification, or other information. The User Flash memory is available to provide a back up the contents of the EBR RAM modules if the user desires. These functions will be discussed in more detail in later sections of this document.

The SRAM can be configured using JTAG, the external Master SPI port, or by using the data stored in on-chip Flash. The configuration process consists of SRAM initialization (clear the RAM and the address pointers), loading the SRAM with the configuration data, and setting the FPGA into user mode (waking up the FPGA).

On-chip Flash can be programmed by using JTAG or by using the external Slave SPI port. JTAG Flash programming can be performed any time the device is powered up. The Slave SPI port uses the sysCONFIG™ pins and can program the Flash directly or in the background. Direct programming takes place during config mode, background programming during user mode. The FPGA enters config mode at power up, when the PROGRAMN pin is pulled low, or when a refresh command is issued via JTAG; it enters user mode when it wakes up, i.e. when the device begins running user code. These two programming modes, direct and background, will be referred to in this document as Flash Direct and Flash Background.

Figure 14-1. Programming Block Diagram



Configuration Pins

The LatticeXP2 has one dedicated and nine dual-purpose sysCONFIG pins. The dual-purpose pins are available as extra I/O pins if they are not used for configuration.

The configuration mode pins, along with a programmable option, controls how the LatticeXP2 will be configured. The configuration mode pins (CFG[1:0]) are generally hard wired on the PCB and determine which configuration mode will be used; the programmable option is accessed via preferences in Lattice ispLEVER® design software, or as HDL source file attributes, and allows the user to protect the configuration pins from accidental use by the user or the place-and-route software. The LatticeXP2 devices also support ispJTAG for configuration, including transparent readback, and for JTAG testing. The following sections describe the functionality of the sysCONFIG and JTAG pins. Note that JTAG and ispJTAG will be used interchangeably in this document. Table 14-1 is provided for reference.

Table 14-1. Configuration Pins for the LatticeXP2 Device ¹

Pin Name	I/O Type	Pin Type	Mode Used
CFG0	Input, weak pull-up	Dedicated	All
CFG1	Input, weak pull-up	Dual-Purpose ²	MSPI, SSPI
PROGRAMN	Input, weak pull-up	Dual-Purpose ²	MSPI, SSPI
INITN	Bi-Directional Open Drain, weak pull-up	Dual-Purpose ²	MSPI, SSPI
DONE	Bi-Directional Open Drain with weak pull-up or Active Drive	Dual-Purpose ²	MSPI, SSPI
CCLK	Input or Output	Dual-Purpose	MSPI, SSPI
SISPI	Input or Output	Dual-Purpose	MSPI, SSPI
SOSPI	Input or Output	Dual-Purpose	MSPI, SSPI
CSSPISN	Input, weak pull-up	Dual-Purpose	Slave SPI
CSSPIN	Output, tri-state, weak pull-up	Dual-Purpose	Master SPI
TDI	Input, weak pull-up	JTAG	
TDO	Output	JTAG	
TCK	Input with Hysteresis	JTAG	

Table 14-1. Configuration Pins for the LatticeXP2 Device (Continued)¹

Pin Name	I/O Type	Pin Type	Mode Used
TMS	Input, weak pull-up	JTAG	

1. Weak pull-ups consist of a current source of 30uA to 150uA. The pull-up for CFG0 tracks V_{CC} (core). This means that any voltage level above V_{CC} is considered a “high.” The pull-ups for TDI and TMS track V_{CCJ} ; all other pull-ups track the V_{CCIO} for that pin.

2. This pin becomes a dedicated programming pin when the CFG0 pin is low.

sysCONFIG Pins

Following is a description of the sysCONFIG pins for the LatticeXP2 device. These pins are used to control or monitor the configuration process. These pins are used for non-JTAG programming sequences only. The JTAG pins will be explained later in the ispJTAG Pins section of this document.

CFG[1:0]

The Configuration Mode pin CFG0 is a dedicated input with a weak pull-up. The CFG1 pin is a dual-purpose input pin with a weak pull-up. The CFG pins are used to select the configuration mode for the LatticeXP2, i.e. what type of device the LatticeXP2 will configure from. At Power-On-Reset (POR), or when the PROGRAMN pin is driven low, the device will enter the configuration mode selected by the CFG[1:0] pins. Note that PROGRAMN must not be asserted until after all power rails have reached stable operation.

Table 14-2. LatticeXP2 Configuration Modes

Configuration Mode	CFG[1]	CFG[0]	Mode Description
Dual-Boot Mode 1	0	0	Will attempt to boot from the external SPI Flash first. If unsuccessful, then it tries to boot from internal Flash.
Dual-Boot Mode 2	1	0	Will attempt to boot from the internal Flash first. If unsuccessful, then it tries to boot from external SPI Flash.
Self Download Mode (SDM)	X ¹	1	Single boot mode. The device will only try to boot from internal Flash.

1. Don't care.

When the CFG0 pin is high, the device will configure itself by reading the data stored in on-chip Flash; this is referred to as SDM, or Self Download Mode. See the Self-Download section of this document for more information regarding SDM. If the CFG0 pin is low then the device will read the CFG1 pin to determine which mode to enter. When CFG1 is low the device will first attempt to configure the SRAM using Master SPI mode with the external SPI Flash port. If this fails then the device will configure itself from the on-chip Flash if a configuration file is stored there. When CFG1 is high the device will first attempt to configure the SRAM using on-chip Flash. If a configuration file is not stored there then the device will configure itself using Master SPI mode with the external SPI Flash port.

Dual-Purpose sysCONFIG Pins

The following is a list of the dual-purpose sysCONFIG pins. These pins are available as general purpose I/O after configuration. If a dual-purpose pin is to be used both for configuration and as a general purpose I/O the user must adhere to the following:

- The I/O type must remain the same. In other words, if the pin is a 3.3V CMOS pin (LVCMOS33) during configuration it must remain a 3.3V CMOS pin as a GPIO.
- The Persistent option must be set to OFF. The Persistent option will be set to OFF by the software unless the user sets the SLAVE_SPI_PORT to ENABLE using the Design Planner in ispLEVER. This option is shown in the Global tab of the Design Planner Spreadsheet view.
- The user is responsible for insuring that no internal or external logic will interfere with device configuration.

After configuration these pins, if not used as GPIO, are tri-stated and weakly pulled up.

CFG1

The CFG1 pin is a dual-purpose input with a weak pull-up. Its function is described in the section above. When the CFG0 pin is high, the CFG1 pin is not used for configuration and becomes a general purpose I/O pin available to the user.

PROGRAMN

The PROGRAMN pin is a dual-purpose input with a weak pull-up. This pin is used to initiate a non-JTAG SRAM configuration sequence. A high to low signal applied to PROGRAMN sets the device into configuration mode. The PROGRAMN pin can be used to trigger configuration at any time. If the device is using JTAG then PROGRAMN will be ignored until the device is released from JTAG mode.

The PROGRAMN pin is only available if the CFG0 pin is set to 0 (not in SDM mode). When the CFG0 pin is set to 1 then PROGRAMN becomes a general purpose I/O pin available to the user.

When the CFG0 pin is set to 0, the PROGRAMN pin becomes a dedicated programming pin.

INITN

The INITN pin is a dual-purpose bi-directional open drain pin with a weak pull-up. INITN is capable of driving a low pulse out as well as detecting a low pulse driven in.

When using either the SPI Flash boot or Embedded Flash Boot mode to configure the SRAM, INITN going low indicates that the SRAM is being initialized; INITN going high indicates that the FPGA is ready to accept configuration data. To delay configuration the INITN pin can be held low externally. The device will not enter configuration mode as long as the INITN pin is held low. After configuration has started INITN is used to indicate a bitstream error. The INITN pin will be driven low if the calculated CRC and the configuration data CRC do not match; DONE will then remain low and the LatticeXP2 will not wake up.

When using SDM, configuration from on-chip Flash INITN is not used or monitored.

When programming on-chip Flash the INITN pin is not used. During Flash Direct programming an error will prevent the FPGA from configuring from the Flash, during Flash Background programming an error will not affect the configuration already running in SRAM.

The INITN pin is only available if the CFG0 pin is set to 0 (not in SDM mode). When the CFG0 pin is set to 1 then INITN becomes a general purpose I/O pin available to the user.

When the CFG0 pin is set to 0, the INITN pin becomes a dedicated programming pin.

DONE

The DONE pin is a dual-purpose bi-directional open drain with a weak pull-up (default), or an actively driven pin. DONE will be driven low when the device is in configuration mode and the internal DONE bit is not programmed. When the INITN and PROGRAMN pins go high, and the internal DONE bit is programmed, the DONE pin will be released (or driven high, if it is an actively driven pin). The DONE pin can be held low externally and, depending on the wake-up sequence selected, the device will not become functional until the DONE pin is externally brought high.

Reading the DONE bit is a good way for an external device to tell if the FPGA is configured.

When using JTAG to configure SRAM the DONE pin is driven by the boundary scan cell, so the state of the DONE pin has no meaning until configuration is completed.

The DONE pin is only available if the CFG0 pin is set to 0 (not in SDM mode). When the CFG0 pin is set to 1 then DONE becomes a general purpose I/O pin available to the user.

When the CFG0 pin is set to 0, the DONE pin becomes a dedicated programming pin.

CCLK

CCLK is a dual-purpose bi-directional pin; direction depends on whether a Master or Slave mode is selected. If a Master mode is selected, the CCLK pin will become an output pin; otherwise CCLK is an input pin.

If the CCLK pin becomes an output, the internal programmable oscillator is connected to the CCLK and is driven out to slave devices. When stopped, CCLK becomes an input (tri-stated output). CCLK will restart (become an output) on the next configuration initialization sequence.

CSSPIN

The CSSPIN pin is a dual-purpose output pin with a weak pull-up. The CSSPIN is an active low chip select to an external SPI flash when used with the Master SPI mode. The CSSPIN pin becomes a dedicated pin if the CFG0 pin is set to 0 (not in SDM mode). When the CFG0 pin is set to 1 then CSSPIN becomes a general purpose I/O pin available to the user.

If the CFG0 is set to 0 then this pin should be driven high unless the Master SPI mode is selected to avoid contention between the Master and Slave SPI modes.

CSSPISN

The CSSPISN pin is a dual-purpose input pin with a weak pull-up. The CSSPISN is an active low chip select to the internal SPI interface and is used with the Slave SPI mode.

If the CSSPISN is driven low while in the middle of Master SPI port activity the Master SPI shall be disabled and the Slave SPI interface activated.

The PERSISTENT preference must be set to ON in order to preserve this pin as CSSPISN and allow access to the Slave SPI interface. The PERSISTENT preference will be set by the software automatically when the user sets the SLAVE_SPI_PORT option in the Design Planner.

SISPI

The SISPI pin is a dual-purpose bi-directional pin; direction depends upon whether a Master or Slave mode is active. The SISPI is the Input data pin when using the Slave SPI mode and is the Output data pin when using the Master SPI mode.

The PERSISTENT preference must be set to ON in order to preserve this pin as SISPI and allow access to the Slave SPI interface. The PERSISTENT preference will be set by the software automatically when the user sets the SLAVE_SPI_PORT option in the Design Planner.

SOSPI

The SOSPI pin is a dual-purpose bi-directional pin; direction depends upon whether a Master or Slave mode is active. The SOSPI is the Input data pin when using the Master SPI mode and is the Output data pin when using the Slave SPI mode.

The PERSISTENT preference must be set to ON in order to preserve this pin as SOSPI and allow access to the Slave SPI interface. The PERSISTENT preference will be set by the software automatically when the user sets the SLAVE_SPI_PORT option in the Design Planner.

Table 14-3. Flash Programming Mode Pin Usage

Flash Programming Mode	Direct	Background	Direct	Background
Port ⁶	Slave SPI		ispJTAG ¹	
Pins	CCLK, CSSPISN, SISPI, SOSPI		TAP	
User I/O States	Tristate	User	BSCAN	User
PROGRAMN	↓	Keep at High	Keep At High ²	
INITN	Pass/Fail	Pass/Fail	Not Used ³	
DONE	Done	Not Used	Keep at High ⁴	
SLAVE_SPI_PORT preference	Don't Care ⁵	ENABLE ⁵	Don't Care	

- ispJTAG can be used to program the Flash regardless of the state of the CFG pins.
- The state of the PROGRAMN pin is ignored by the device during JTAG Flash programming but the pin should be held high as a low will cause a configuration failure. When the device is in the SDM mode, the PROGRAMN pin is a dedicated I/O pin so it does not affect configuration.
- The state of the INITN pin is ignored by the device during JTAG Flash programming but the pin should be allowed to float high using the internal pull-up. When the device is in the SDM mode, the INITN pin is a dedicated I/O pin so it does not affect configuration.
- The state of the DONE pin is ignored by the device during JTAG Flash programming but the pin should be allowed to float high using the internal pull-up as a low can keep the device from waking up. When the device is in the SDM mode, the DONE pin is a dedicated I/O pin so it does not affect configuration.
- The SLAVE_SPI_PORT preference must be set to ENABLE to use the Slave SPI port after the device has been configured. The Slave SPI port is also available when the device is not configured.
- The Master SPI port can only be used to configure the SRAM in direct mode from an external SPI Flash memory. The CFG pins must be set per Table 14-2 to enable this mode.

Table 14-4. Memory Access Modes

Mode	Flash		SRAM	
	Read	Write	Read	Write
Slave SPI	Yes ²	Yes ¹	Yes	No
Master SPI	No	No	No	Yes ³

- Slave SPI mode can only write to on-chip Flash memory in background mode unless the Flash memory is erased.
- Slave SPI mode can read from on-chip Flash memory in background mode only.
- Master SPI mode can write to SRAM in direct mode only.

External SPI Flash

When the Master SPI mode is used for configuration an external SPI Flash device is required to hold the configuration data. The size of the bitstream and the required external SPI Flash is shown in Table 14-5.

Table 14-5. Maximum Configuration Bits

Density	Bitstream Size (Mb)	SPI Flash (Mb)
XP2-5	1.27	2
XP2-8	1.99	2
XP2-17	3.54	4
XP2-30	5.79	8
XP2-40	8.03	16

Programming Sequence

There are two types of programming, SRAM, and Flash Background. This section goes through the process for each showing how the dedicated pins are used.

SRAM

When not using SDM (Self Download Mode, on-chip Flash) to program the SRAM, the sequence begins when the internal power-on reset (POR) is released or the PROGRAMN pin is driven low (see Figure 14-2). The LatticeXP2 then drives INITN low, tri-states the I/Os, and initializes the internal SRAM and control logic. When this is complete, if PROGRAMN is high, INITN will be released. If INITN is held low externally the LatticeXP2 will wait until it goes high. When INITN goes high the LatticeXP2 begins looking for the configuration data using the internal Flash memory or the Master SPI port, as determined by the CFG pins.

If the CFG1 pin is high and the Flash Done bit is set (indicating that the on-chip Flash memory is programmed) then the LatticeXP2 will boot from the on-chip Flash memory. If the Flash Done bit is not set then the LatticeXP2 will boot from the external SPI Flash memory using the Master SPI mode.

If the CFG1 pin is low then the LatticeXP2 will boot from the external SPI Flash memory using the Master SPI mode. In the event of an error the LatticeXP2 will boot from the on-chip Flash memory if the Flash Done bit is set.

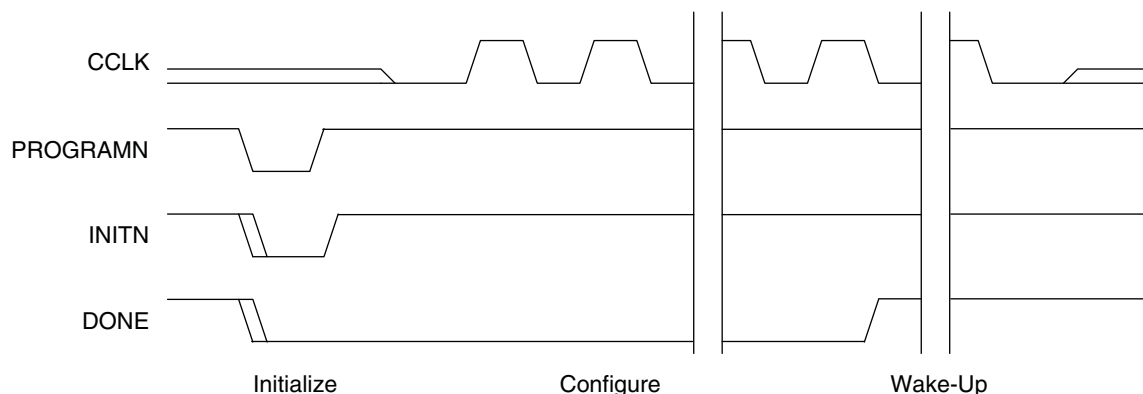
Once configuration is complete the internal DONE bit is set, the DONE pin goes high, and the FPGA wakes up (enters user mode). If a CRC error is detected when reading the bitstream INITN will go low, the internal DONE bit will not be set, the DONE pin will stay low, and the LatticeXP2 will not wake up.

When using SDM to program SRAM the sequence is similar but INITN is not used or monitored. The sequence begins when the internal power-on reset (POR) is released. The LatticeXP2 then tri-states the I/Os and initializes the internal SRAM and control logic. When initialization is complete the LatticeXP2 begins loading configuration data from on-chip Flash.

When using SDM, if the Flash has been programmed, then the configuration sequence will proceed using the data in on-chip Flash. If the Flash has not been programmed, the configuration sequence will stop. Once the Flash has been programmed, a POR or JTAG Refresh instruction must occur to restart the configuration sequence.

When using SDM, once configuration is complete, the internal DONE bit is set and the FPGA wakes up (enters user mode). The external Done pin is not available when using SDM configuration.

Figure 14-2. SRAM Configuration Timing Diagram



Flash Background

Flash Background programming is possible using the Slave SPI port when it is enabled. The Slave SPI port can be enabled in the SDM mode as well as the SPI mode. Flash Background will not disturb the FPGA's present configuration in SRAM.

Flash Background programming may be used in both config mode and user mode (Done bit = 0 or 1). To support Flash Background programming in user mode the SLAVE_SPI_PORT preference must be set to ENABLE.

When the CSSPISN pin goes low, the FPGA will wait for the preamble and then look for the proper commands. A low on INITN indicates an error during a Flash erase or program. Data is written and read on the SISPI and SOSPI pins.

After programming the Flash the user may toggle the PROGRAMN pin to transfer the Flash data to SRAM if the SPI mode is being used. If the SDM mode is being used then the SRAM will be updated on the next power up sequence of when a refresh instruction is issued.

If the CSSPISN pin is driven low, the CSSPIN should be driven high and CCLK maintained as an input to prevent activating the Master SPI interface. This will avoid contention between the Master and Slave SPI interfaces.

ispJTAG Pins

The ispJTAG pins are standard IEEE 1149.1 TAP (Test Access Port) pins. The ispJTAG pins are dedicated pins and are always accessible when the LatticeXP2 device is powered up. When programming the SRAM via ispJTAG the dedicated programming pins, such as DONE, cannot be used to determine programming progress. This is because the state of the boundary scan cell will drive the pin, per JTAG 1149.1, rather than normal internal logic.

TDO

The Test Data Output pin is used to shift out serial test instructions and data. When TDO is not being driven by the internal circuitry, the pin will be in a high impedance state.

TDI

The Test Data Input pin is used to shift in serial test instructions and data. An internal pull-up resistor on the TDI pin is provided. The internal resistor is pulled up to V_{CCJ} .

TMS

The Test Mode Select pin controls test operations on the TAP controller. On the falling edge of TCK, depending on the state of TMS, a transition will be made in the TAP controller state machine. An internal pull-up resistor on the TMS pin is provided. The internal resistor is pulled up to V_{CCJ} .

TCK

The test clock pin, TCK, provides the clock to run the TAP controller, which loads and unloads the data and instruction registers. TCK can be stopped in either the high or low state and can be clocked at frequencies up to the frequency indicated in the device data sheet. The TCK pin supports the value is shown in the DC parameter table of the data sheet. The TCK pin does not have a pull-up. A pull-down on the PCB of 4.7 K is recommended to avoid inadvertent clocking of the TAP controller as V_{CC} ramps up.

VCCJ

JTAG V_{CC} (V_{CCJ}) supplies independent power to the JTAG port to allow chaining with other JTAG devices at a common voltage. V_{CCJ} must be connected even if JTAG is not used. This voltage may also power the JTAG download cable. Valid voltage levels are 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V.

Please see [In-System Programming Design Guidelines for ispJTAG Devices](#) for further information.

Configuration and JTAG Voltage Levels

All of the control pins and programming pins default to LVCMOS. The CFG0 pin is linked to V_{CC} (core); TCK, TDI, TDO, and TMS track V_{CCJ} ; all other pins track the V_{CCIO} for that pin.

Configuration Modes and Options

The LatticeXP2 device supports two configuration modes, utilizing the SPI port or self-configuration. On power up, or upon driving the PROGRAMN pin low depending upon the current mode, the CFG[1:0] pins are sampled to determine the mode that will be used to configure the LatticeXP2 device. The CFG pins are generally hard wired on the PCB and determine how the device will retrieve its configuration data. The SLAVE_SPI_PORT preference is a programmable option which can be set using the Design Planner in Lattice ispLEVER design software, or as HDL source file attributes, and allow the user to protect the configuration pins from accidental use by the user or the place-and-route software.

Configuration Options

Several configuration options are available for each configuration mode.

- When using a master clock, the master clock frequency can be set.
- A security bit is provided to prevent SRAM or Flash readback.

By setting the proper parameters in the Lattice ispLEVER design software the selected configuration options are set in the generated bitstream. As the bitstream is loaded into the device the selected configuration options take effect. These options are described in the following sections.

Master Clock

If the LatticeXP2 is a Master device the CCLK pin will become an output with the frequency set by the user. The default Master Clock Frequency is 2.5 MHz. The software default adjusts the MCLK frequency to 3.1 MHz in the programming bitstream.

The user can determine the Master Clock frequency by setting the MCCLK_FREQ. One of the first things loaded during configuration is the MCCLK_FREQ parameter; once this parameter is loaded the frequency changes to the selected value using a glitchless switch. Care should be exercised not to exceed the frequency specification of the slave devices or the signal integrity capabilities of the PCB layout.

The MCCLK frequency selections made by the user are only valid if the LatticeXP2 device is booted from external SPI Flash. The internal Flash will not control the MCCLK frequency setting in the JEDEC file. In the case of device boot from internal Flash the MCCLK frequency is always 3.1 MHz. In the case of booting the device from external SPI Flash, the user can use UFW program inside the ispVM tool suite to convert the JEDEC file to bitstream format. The UFW program supports MCCLK_FREQ selections. In this case the user can select MCCLK_FREQ during bitstream conversion. MCCLK_FREQ selections from UFW range 2.5 MHz to 130 MHz.

Security Bit

Setting the security bit prevents readback of the SRAM and Flash from JTAG or the sysCONFIG pins. When the security bit is set the only operations available are erase and write. The security bit is updated as the last operation of SRAM configuration or Flash programming. By using on-chip Flash, and setting the security bit, the user can create a very secure device.

The security bit is accessed via the Design Planner in ispLEVER design software.

More information on device security can be found in the document [FPGA Design Security Issues: Using the ispXPGA Family of FPGAs to Achieve High Design Security](#).

Slave SPI Mode

In the Slave SPI mode the CCLK pin becomes an input and commands will be read into the LatticeXP2 on the SISPI pin at the rising edge of CCLK. Data will be written out of the LatticeXP2 on the SOSPI pin at the falling edge of CCLK.

Care must be exercised during read back of EBR or PFU memory. It is up to the user to ensure that reading these RAMs will not cause data corruption, i.e. these RAMs may not be read while being accessed by user code.

The CSSPISN enables and disables the SPI interface operation. When CSSPISN is high the SPI interface is deselected and the SOSPI pin is at high impedance. When CSSPISN is brought low the SPI interface is selected, commands can be written into and data read from the LatticeXP2. After power up the CSSPISN must transition from high to low before a new command can be accepted.

The Slave SPI mode can also be used to access on-chip Flash. The CSSPISN pin must be held low to write to on-chip Flash; data is input from SISPI. The Slave SPI mode can also be used for readback of both Flash and SRAM. By driving the CSSPISN low, the device will input the readback instructions on the SISPI pin and the data will be written out on the SOSPI pin; a bit in the read command will determine if the read is directed to Flash or SRAM. In order to support readback while the device is in user mode (the DONE pin is high), the SLAVE_SPI_PORT preference must be set to ENABLE using the Design Planner.

Master SPI Mode

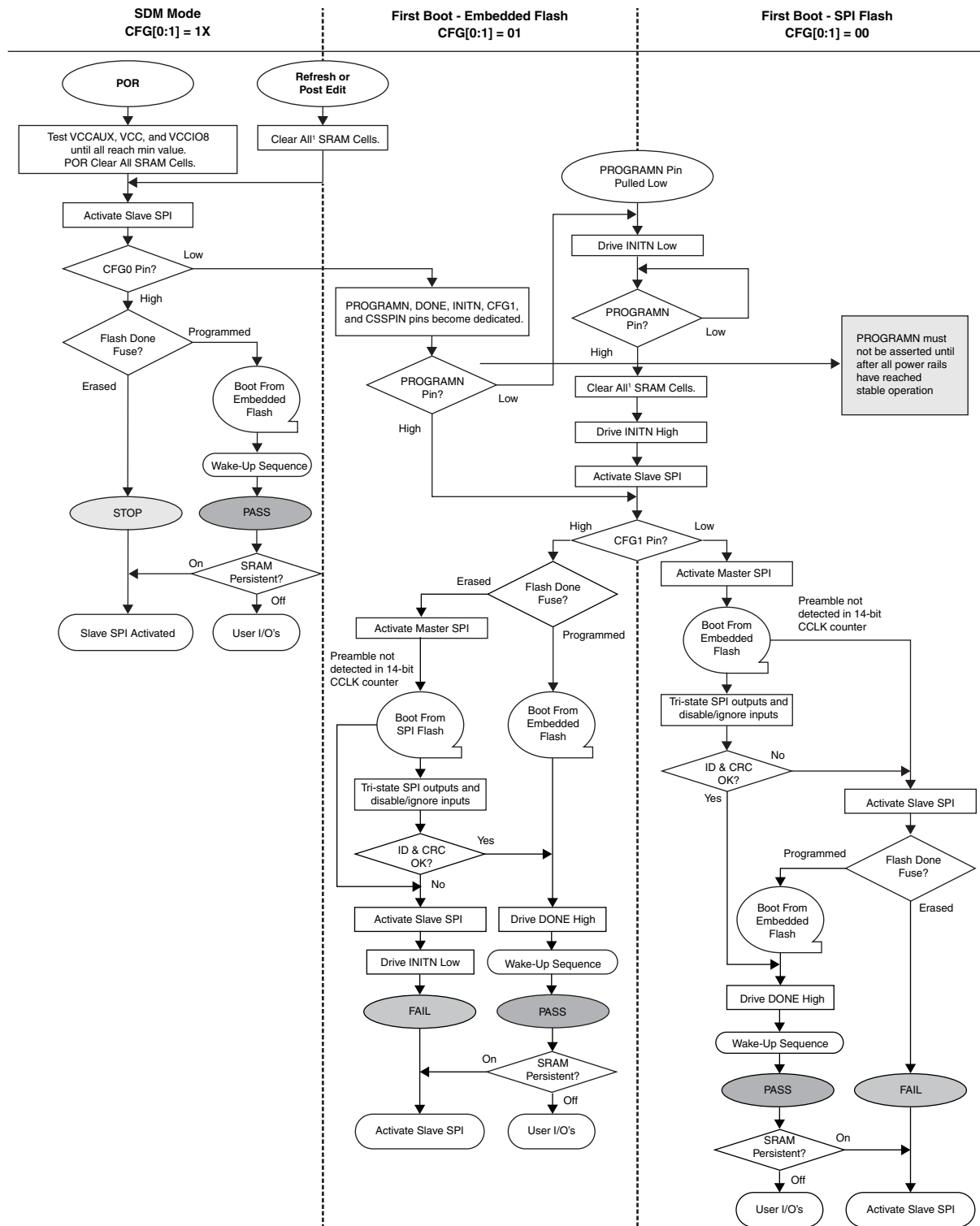
In Master SPI mode the LatticeXP2 will drive CCLK out to the Slave SPI Flash device that will provide the bitstream. The Master device will write commands out on SISPI at the falling edge of CCLK and will accept data on SOSPI at the rising edge of CCLK. The Master Serial device starts driving CCLK at the beginning of the configuration and continues to drive CCLK until the external DONE pin is driven high. The CCLK frequency on power up defaults to 2.5 MHz. The master clock frequency default remains unless a new clock frequency is loaded from the bitstream.

Self Download Mode

Self Download Mode (SDM) allows the FPGA to configure itself without using any external devices, and because the bitstream is not exposed this is also a very secure configuration mode. The user may access on-chip Flash using ispJTAG or the slave SPI port pins.

JTAG may access the on-chip Flash any time the device is powered up, without disturbing device operation. JTAG may also read and write the configuration SRAM. If access to the on-chip Flash and SRAM is limited to JTAG then SLAVE_SPI_PORT can be set to DISABLE, freeing the dual-purpose pins for use as general purpose I/O.

Figure 14-3. Configuration Flow Diagram



ispJTAG Mode

The LatticeXP2 device can be configured through the ispJTAG port. The ispJTAG port is always on and available, regardless of the configuration mode selected. The SLAVE_SPI_PORT can be set to DISABLE in the Lattice isp-LEVER design software to tell the place and route tools that the JTAG port will be used exclusively, i.e. the SPI port will not be used. Setting the SLAVE_SPI_PORT to DISABLE allows software to use all of the dual-purpose pins as general purpose I/Os.

ISC 1532

Configuration through the ispJTAG port conforms to the IEEE 1532 Standard. The Boundary Scan cells take control of the I/Os during any 1532 mode instruction. The Boundary Scan cells can be set to a pre-determined value whenever using the JTAG 1532 mode. Because of this the dedicated pins, such as DONE, cannot be relied upon for valid configuration status.

Transparent Readback

The ispJTAG Transparent Readback mode allows the user to read the content of the device SRAM or Flash while the device remains in a functional state. Care must be exercised when reading EBR and distributed RAM, as it is possible to cause conflicts with accesses from the user design (causing possible data corruption).

The I/O and non-JTAG configuration pins remain active during a Transparent Readback. The device enters the Transparent Readback mode through a JTAG instruction.

Boundary Scan and BSDL Files

BSDL files for this device can be found on the Lattice website at www.latticesemi.com. The boundary scan ring covers all of the I/O pins, as well as the dedicated and dual-purpose sysCONFIG pins.

Wake Up Options

When configuration is complete (the SRAM has been loaded), the device should wake up in a predictable fashion. The following selections determine how the device will wake up. Two synchronous wake up processes are available. One automatically wakes the device up when the internal Done bit is set regardless of whether the DONE pin is held low externally or not, the other waits for the DONE pin to be driven high before starting the wake up process. The DONE_EX preference determines whether the external DONE pin will control the synchronous wake up. When the device is in the SDM mode the DONE pin is not used and therefore the DONE_EX preference has no effect.

Wake Up Sequence

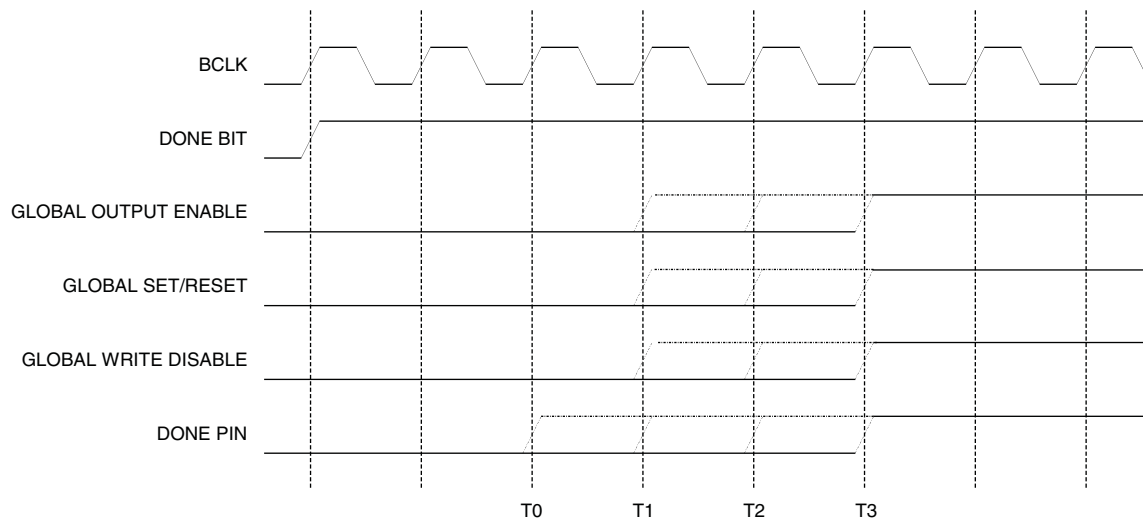
Table 14-6 provides a list of the wake up sequences supported by the LatticeXP2.

Table 14-6. Wake Up Sequences Supported by LatticeXP2

Sequence	Phase T0	Phase T1	Phase T2	Phase T3
1	DONE	GOE, GWDIS, GSR		
2	DONE		GOE, GWDIS, GSR	
3	DONE			GOE, GWDIS, GSR
4	DONE	GOE	GWDIS, GSR	
5	DONE	GOE		GWDIS, GSR
6	DONE	GOE	GWDIS	GSR
7	DONE	GOE	GSR	GWDIS
8		DONE	GOE, GWDIS, GSR	
9		DONE		GOE, GWDIS, GSR
10		DONE	GWDIS, GSR	GOE
11		DONE	GOE	GWDIS, GSR
12			DONE	GOE, GWDIS, GSR
13		GOE, GWDIS, GSR	DONE	

Table 14-6. Wake Up Sequences Supported by LatticeXP2 (Continued)

Sequence	Phase T0	Phase T1	Phase T2	Phase T3
14		GOE	DONE	GWDIS, GSR
15		GOE, GWDIS	DONE	GSR
16		GWDIS	DONE	GOE, GSR
17		GWDIS, GSR	DONE	GOE
18		GOE, GSR	DONE	GWDIS
19			GOE, GWDIS, GSR	DONE
20		GOE, GWDIS, GSR		DONE
21 (Default)		GOE	GWDIS, GSR	DONE
22		GOE, GWDIS	GSR	DONE
23		GWDIS	GOE, GSR	DONE
24		GWDIS, GSR	GOE	DONE
25		GOE, GSR	GWDIS	DONE

Figure 14-4. Wake Up Sequence to Internal Clock


Synchronous to Internal Done Bit

If the LatticeXP2 device is the only device in the chain, or the last device in a chain, the wake up process should be initiated by the completion of the configuration. Once the configuration is complete, the internal Done bit will be set and then the wake up process will begin.

Synchronous to External DONE Signal

The DONE pin can be selected to delay wake up. If DONE_EX is true then the wake up sequence will be delayed until the DONE pin is high. The device will then follow the WAKE_UP sequence selected. When the device is in the SDM mode the DONE pin is not used and therefore the DONE_EX preference has no effect.

Software Selectable Options

In order to control the configuration of the LatticeXP2 device beyond the default settings, software preferences are used. Table 14-7 is a list of the preferences with their default settings.

Table 14-7. Software Preference List for the LatticeXP2

Preference Name	Default Setting [List of All Settings]
SLAVE_SPI_PORT	DISABLE [disable, enable]
MASTER_SPI_PORT	DISABLE [disable, enable]
DONE_OD	ON [off, on]
DONE_EX	OFF [off, on]
CONFIG_SECURE	OFF [off, on]
WAKE_UP	21 (DONE_EX = off) 4 (DONE_EX = on)
WAKE_ON_LOCK	OFF [off, on]
INBUF	ON [off, on]

Slave SPI Port

In order to use the Slave SPI port while in user mode to read SRAM or Flash memory, the SLAVE_SPI_PORT preference must be set to ENABLE. Setting this preference preserves the Slave SPI port pins so the FPGA can be accessed by an external device while in user mode. This also lets the software know that the Slave SPI port pins are reserved and NOT available for use by the fitter or the user.

Master SPI Port

In order to use the Master SPI Port for configuration, the MASTER_SPI_PORT preference should be set to ENABLE.

Configuration Mode

The device knows which physical sysCONFIG port will be used by reading the state of the CFG[1:0] pins, but the fitter software also needs to know which port will be used. The fitter will determine the configuration mode based upon the setting of the SLAVE_SPI_PORT and the MASTER_SPI_PORT preferences. The user may set these preferences, and the ones listed below, using the Design Planner tool.

There are several additional configuration options, such as overflow, that are set by software. These options are selected by clicking Properties under Generate Bitstream Data in ispLEVER. If either overflow option is selected, then the DONE_EX and WAKE_UP selections will be set to correspond (see Table 14-8). Refer to the Configuration Modes and Options section of this document for more details.

Table 14-8. Overflow Option Defaults

Overflow Option	DONE_EX Preference	WAKE_UP Preference
Off	Off (Default)	Default 21 (user selectable 1 through 25)
Off	On	Default 21 (user selectable 1 through 25)
On (either)	On (automatically set by software)	Default 4 (User selectable 1 through 7)

DONE Open Drain

The “DONE_OD” preference allows the user to configure the DONE pin as an open drain pin. The “DONE_OD” preference is only used for the DONE pin. When the DONE pin is driven low, internally or externally, this indicates that configuration is not complete and the device is not ready for the wake up sequence. Once configuration is complete, with no errors, and the device is ready for wake up, the DONE pin must be driven high. For other devices to be able to control the wake up process an open drain configuration is needed to avoid contention on the DONE pin. The “DONE_OD” preference for the DONE pin defaults to ON. The DONE_OD preference is automatically set to ON if the DONE_EX preference is set to ON. See Table 14-9 for more information on the relationship between DONE_OD and DONE_EX. When the device is in the SDM mode the DONE pin is not used and therefore the DONE_OD and DONE_EX preferences have no effect.

DONE External

The LatticeXP2 device can wake up on its own after the Done bit is set or wait for the DONE pin to be driven high externally. Set DONE_EX = ON to delay wake up until the DONE pin is driven high by an external signal synchronous to the clock; select OFF to synchronously wake up when the internal Done bit is set and ignore any external driving of the DONE pin. The default is DONE_EX = OFF. If DONE_EX is set to ON, DONE_OD will be set to ON. If an external signal is driving the DONE pin it should be open drain as well (an external pull-up resistor may need to be added). See Table 14-9 for more information on the relationship between DONE_OD and DONE_EX.

Table 14-9. Summary of DONE Pin Preferences

DONE_EX ¹	Wake Up Process	DONE_OD ¹
OFF	External DONE ignored	User selected
ON	External DONE low delays	Set to Default (ON)

1. When the device is in the SDM mode the DONE pin is not used and therefore the DONE_OD and DONE_EX preferences have no effect.

Master Clock Selection

When the user has determined that the LatticeXP2 will be a master configuration device (by properly setting the CFG[1:0] pins), and therefore provide the source clocking for configuration, the CCLK pin becomes an output with the frequency set by the value in MCCLK_FREQ. At the start of configuration the device operates at the default Master Clock Frequency of 2.5 MHz. Some of the first bits in the configuration bitstream are MCCLK_FREQ, once these are read the clock immediately starts operating at the user-defined frequency. The clock frequency is changed using a glitchless switch. The default MCCLK frequency set in the bitstream is 3.1 MHz.

Security

When CONFIG_SECURE is set to ON, NO read back operation will be supported through the sysCONFIG or ispJTAG port of the general contents. The ispJTAG DeviceID area is readable and not considered securable. Default is OFF.

Wake Up Sequence

The WAKE_UP sequence controls three internal signals and the DONE pin. The DONE pin will be driven after configuration and prior to user mode. See the Wake Up Sequence section of this document for an example of the phase controls and information on the wake up selections. The default setting for the WAKE_UP preference is determined by the DONE_EX setting.

Wake Up with DONE_EX = Off (Default Setting)

The WAKE_UP preference for DONE_EX = OFF (default) supports the user selectable options 1 through 25, as shown in Table 14-6. If the user does not select a wake-up sequence, the default, for DONE_EX = OFF, will be wake-up sequence 21.

Wake Up with DONE_EX = On

The WAKE_UP preference for DONE_EX = ON supports the user selectable options 1 through 7, as shown in Table 14-6. If the user does not select a wake-up sequence, the default will be wake-up sequence 4.

Wake On Lock Selection

The Wake On Lock preference determines whether the device will wait for the PLL to lock before beginning the wake-up process.

ON – The device will not wake up until the PLL lock signal for the given PLL is active.

OFF (default) – The device will wake up regardless of the state of the PLL lock signal.

Power Save

An I/O Power Save mode option, called INBUF, is used for the LatticeXP2 device and will deactivate unused input buffers to save power. This only affects comparator type inputs pins (pins that use VREF), like HSTL, SSTL, etc.

The Power Save mode limits some of the functionality of Boundary Scan. For Boundary Scan testing it is recommended that the INBUF global preference be turned ON to activate all unused input buffers.

One Time Programmable Fuse

The LatticeXP2 has a One Time Programmable (OTP) fuse that can be used to prevent the on chip Flash configuration memory from being erased or programmed. This does not prevent the Flash Tag Memory or Flash User memory from being programmed, so these features are still available. The OTP fuse can be set using the Global Configuration options in the ispLEVER Design Planner or it can be set directly using the ispVM[®] System software at the time of download.

User GOE

The LatticeXP2 has a User GOE (Global Output Enable) feature. This allows the I/Os to be held in Boundary scan control after the standard wake-up sequence has completed. User logic determines when the outputs get turned over from Boundary Scan to User Logic control. This user logic input will be through a CIB and is valid for JTAG “wake up” instructions only.

This feature is instantiated by the user as a macro called IOWAKEUP. This macro only has one signal and can only be controlled immediately after the wakeup sequence (not anytime after).

Tag Memory

The TAG Memory is a block of Flash memory which is always available for read or write (programming in Flash terms) through the Slave SPI port. The LatticeXP2 can be in user mode or an un-programmed state (blank device), independent of the CFG[1:0] pin setting. The only exceptions would be when the LatticeXP2 is in BSCAN test or in direct programming mode. During these modes the SPI interface is unavailable because the I/O is under BSCAN control.

The TAG memory is also available through the JTAG port.

Table 14-10 shows the amount of Tag memory available in each LatticeXP2 device. Each LatticeXP2 device has one dedicated row of TAG memory.

Table 14-10. LatticeXP2 Family TAG Memory

Device Density	Tag Memory (Bits)	Tag Memory (Bytes)
XP2-5	632	79
XP2-8	768	96
XP2-17	2184	273
XP2-30	2640	330
XP2-40	3384	423

Note: The Initial Power on Value (INITVAL) for all Flash cells is all 1's.

The TAG memory has the following features and limitations.

- Each row of TAG memory is limited to sequential access only. Once the read command is specified, the entire TAG memory contents are read sequentially in a first-in-first-out manner.
- Data access speed is limited by the speed of the TAG memory which is Flash based.
- The TAG memory comes from the factory erased. It will retain the user assigned value after programming even during power off periods.

- The TAG memory can be read or written using the hardwired JTAG and SPI interface pins.
- The TAG memory is ready to use upon power-up of the LatticeXP2. It does not need any software IP or design loaded into the device to access the TAG memory via the hardwired interface.
- The TAG memory can also be read and modified from the FPGA core logic using the slave-SPI CIB interface pins to emulate an I²C port.
- The TAG memory is always accessible regardless of the security setting of the device.
- The TAG memory should be disabled before toggling the PROGRAMN pin.
- The TAG memory should be disabled before rebooting the device (power-off-on).

The TAG memory is designed for storing typically “static” data - data that is not likely to change. This TAG memory can take the place of an EEPROM or simple Flash memory on the PCB which might be used for the following system management and manufacturing control information (listed as examples only):

- Saving Electronic ID codes
- Version management
- Date stamping
- Manufacturing version control
- Asset management and tracking
- System calibration settings
- Device serialization and/or inventory control.

Slave SPI Mode Operation

The Slave SPI Mode interface to the TAG memory supports both SPI Bus Mode 0 and Mode 3 operations. In SPI Bus Mode 0 the CLK pin is normally low when the SPI master is in standby and data is not being transmitted. In SPI Bus Mode 3 the CLK pin is normally high during this condition. In both cases the data at the SISPI pin is sampled on the rising edge of CCLK and the data output on the SOSPI pin is clocked on the falling edge of CCLK.

For more information on using the TAG memory please see TN1137, [LatticeXP2 Memory Usage Guide](#).

User Flash

The User Flash is designed as a non-volatile memory location to back up the data stored in the EBR RAM blocks. This gives the user a reliable method to save the contents of the RAM memory for later use.

The amount of User Flash for LatticeXP2 devices is directly tied to the number of EBR blocks in the device and it scales with density. The User Flash is organized physically as either 1- or 2- separate User Flash Modules. However, all User Flash Modules are logically treated as one unified block.

Table 14-11. User Flash Organization

Block Type	XP2-5K	XP2-8K	XP2-17K	XP2-30K	XP2-40K
Physical UFM blocks	1	1	2	2	2
Logical UFM blocks	1	1	1	1	1

The EBR blocks act as the primary interface for the User Flash. Users do not have direct access to the User Flash.

The contents of the EBR can be saved into the User Flash via a store-to-flash control signal. The EBR contents must be saved into the User Flash when required. Two signals, UFMFAIL and UFMBUSYN are provided for keeping track of the status of the store-to-flash command. If the UFMFAIL signal is low and the UFMBUSYN signal is high then the EBR contents were successfully stored in the Flash memory.

The User Flash memory has the following constraints upon its usage.

- The Store-to-Flash operation has impact only on the EBR RAM (Single-Port, True Dual-Port, Pseudo Dual-Port) configurations.
- During the Store-to-Flash operation, the EBR blocks are unavailable for user operation and the Flash is unavailable for configuration operation.
- No selective EBR storing is supported. A Store-to-Flash operation will store the contents of all EBR blocks.
- Due to silicon limitations the user cannot use Store-to-Flash operation if the SED is operating in an Always mode.
- UFM mode cannot concurrently be used with Transparent/Background mode (Flash or SRAM). The SSPI configuration and verify operations (which are essentially Transparent Mode operations) are initiated by the user and the user needs to ensure that the UFM operation is not requested at the same time.

Table 14-12. Differences Between User Flash and Shadow Flash (EBR) Behavior

Parameter	User Flash	Shadow Flash (EBR)
Read/write access speed	Slow	Fast
Access nature	Sequential	Random
Data access	Limited (refer to Sec13.3)	Infinite or unlimited
Data organization	Sequential, one bit at a time	Flexible, variable data width
Data granularity	Whole UFM block	One EBR block

For more information, please see TN1137, [LatticeXP2 Memory Usage Guide](#).

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2007	01.0	Initial release.
May 2007	01.1	Updated sysCONFIG Pin descriptions
		Added footnote to Summary of DONE Pin Preferences table.
January 2008	01.2	Updated Slave SPI Port information and PROGRAMN pin usage.
		Removed PERSISTENT and CONFIG_MODE preferences.
		Added SLAVE_SPI_PORT and MASTER_SPI_PORT preferences.
February 2008	01.3	Corrected SLAVE_SPI_PORT settings in ispJTAG mode section.
		Corrected INITN pin description.
		Corrected SDM configuration description in SRAM section.
November 2008	01.4	Updated Dual-Purpose sysCONFIG Pins text section.
April 2009	01.5	Updated LatticeXP2 Configuration Modes table.
June 2009	01.6	Added clarification to MCCLK frequency selection.
July 2011	01.7	Updated LatticeXP2 Configuration Modes table.
July 2013	01.8	Updated CFG[1:0] description in sysCONFIG Pins section.
		Added Configuration Flow Diagram.
		Updated Technical Support Assistance information.
		Updated document with new corporate logo.
September 2013	01.9	Updated footnote in Configuration Pins for the LatticeXP2 Device table.
January 2014	02.0	Updated description of CCLK pin in the sysCONFIG Pins section.
		Updated description on driving CCLK in the Master SPI Mode section.
		Added items to the list of features and limitations in the Tag Memory section.