The Challenges of Automotive Vision Systems Design

A Lattice Semiconductor White Paper

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Automotive Vision Systems Design Challenges

Automotive electronics are now beginning to radically change the automobile in ways that would have seemed impossible just a few years ago. Engine control and ABS systems based on electronic sub-systems are now standard features of most automobiles. Among the many new and emerging applications undergoing significant change, one primary example is automotive vision systems. Indeed, video and vision processing have become the fastest growing technologies being deployed in automobiles

To fuel this expansion in vision applications, the automotive electronics market continues to increase its need for Complex Programmable Logic Devices (CPLDs) and Field Programmable Gate Arrays (FPGAs). Higher integration of electronic components, along with declining electronics prices, is the primary enabler of this trend. Lane keeping, driver monitoring, night vision and occupant classification are just a few of the applications driving the need for additional vehicle imagers. Many of the new applications using video imagers are in the area of advanced safety systems, which are used to assist the driver in vehicle management, or to autonomously control occupant safety systems. Along with imager video data, new video sources also need processing, including video games and video stored on high-speed Serial ATA disk drives.

There are several considerations that a system architect must think through when designing automobile video systems. The first is the functionality of the system. For instance, will it be a system that handles vision information for safety systems, streaming video data for entertainment, or a combination of the two? What are the interconnection types and speed among the video system components? Additional considerations include:

- How many video source devices are there?
- How many display outputs?
- How far apart are the different devices in the system?
- Which wiring scheme will be used?

All the while, the system architect must be keenly aware of the overall system cost.

Interconnect

Interconnection of the various sources is one of the most critical areas for consideration, and this white paper will focus primarily on the different topologies that may be utilized in an automobile.

Figure 1 graphically shows three topologies that may be utilized: Star, Bus and Ring. The Star topology is a “one to one” connection system. One external component connects to one of the video controller ports, and the communication channel can be either uni-directional or bi-directional. This is the most common low-cost connection option. All the interaction between the devices is known and pre-set. A system constructed in this way is difficult to expand once it is deployed, unless all the necessary connection options were considered in the initial design specification. A DVD player sending composite video to the system video controller for display on an LCD panel is an example of this type of connection.

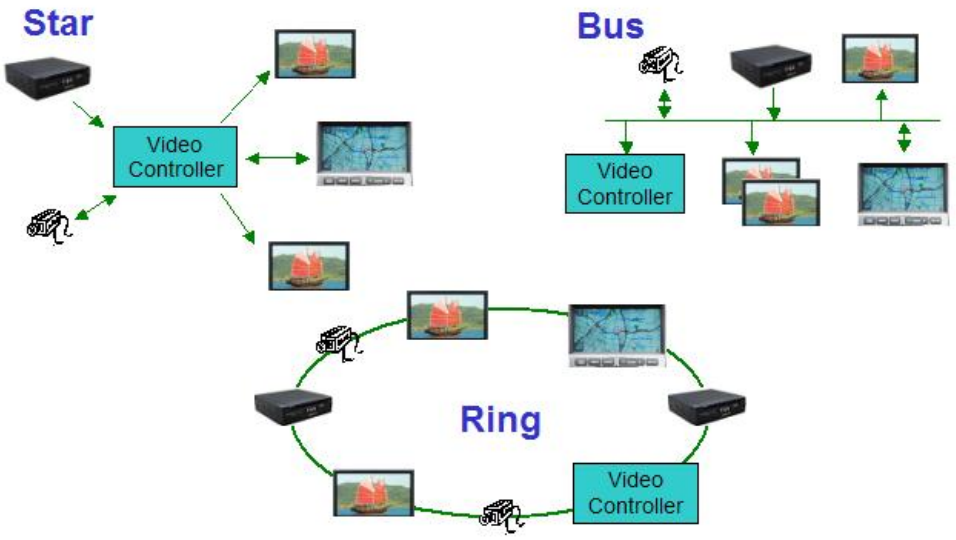

Figure 1 – Star, Bus and Ring Topologies

The Bus topology is a “one to many” connection, in which a single device connects to the bus, which may have several different devices attached to it. Each device on the bus must have a local controller that knows how and when to communicate with the other devices on the bus. The local controller places the video data into packets, which are then transmitted across the bus. Each device has a unique address that is used by the communications protocol for sending and receiving video packet data. When receiving data, each local controller listens to the bus for any packets that are addressed to it. The local controller then will pass the packet information on to the device for processing. This type of system is easily expandable because each device has a unique address. One drawback, however, is that there may not be enough bus bandwidth to share among multiple video devices. USB and CAN are examples of implementations using Bus topologies.

Ring is the third topology. Once again, each device on the ring has a unique address, a local data controller and media transceiver for connection to the

ring. The transceiver has an incoming and outgoing connection. For a display device such as an LCD display, the transceiver receives information from the previous device on the ring, looking for its own address in the data packet; if there is a match, it processes the data or command. If the address doesn't match, then it transmits the data packet to the next device on the ring.

Automotive Ring Buses for entertainment applications are designed with very high bandwidth in order to support many different devices transmitting audio and video packets in a way that makes them appear real-time to a viewer. Ring buses are typically based on Twisted Pair wiring or Optical cabling. These systems are very expandable, but each device needs a local controller and transceiver for the appropriate wiring medium, which adds to the overall system cost.

Signalling

The next step in the process is to consider what types of signalling will be used to transmit data over the bus system. There are many protocols that could be utilized.

Table 1 lists the different signalling protocols that are prevalent in automotive video designs, and compares their attributes. The first column provides the signalling name, and the second, third and fourth columns list the physical cable type, the relative cost and the ease of field expansion. There are then two columns for typical video image sensors. The first column tells if this is a native interface to the image sensor and then the relative price to connect to this protocol. In the case of RGB, which is the first row, it is not a native output for an automotive image sensor and the cost to convert the image sensor data to RGB for transmission is high.

The next two columns for the FPGA are similar to columns for the imager. First is whether the interface is a standard I/O for the FPGA, and the associated relative cost. Some of the protocols are listed twice, and the second occurrence is noted in a grey color: this is to note that there are

FPGAs that contain a Serialize / Deserialize (SERDES) as part of its I/O structure.

The next two columns provide the same information for LCD panels. Some of the LCD interfaces are not a standard that is available in most panel sizes. The final column is an overall relative rating for using the interface system from imager to FPGA to LCD panel. It factors in the cabling costs along with the expandability and the native connection cost for each device and gives a rating. It does not use any distance data, which is why LVTTL gets a Best rating, even though it is suitable only for short distances. The MOST system also gets a Best rating because it is very expandable and offers high speed, even though it has a relatively high implementation cost.

System Interconnect Schemes

Signal	Cable Type	Cable Cost per foot	Ease of field expansion	Standard Camera Output	Cost to implement at Camera	Standard I/O for FPGA	Cost to implement for FPGA	Standard LCD Panel	Cost to implement at LCD	Relative Overall Score
RGB	Copper	Medium	Poor	No	High	No	High	No	High	Poor
S Video	Copper	Medium	Poor	No	High	No	High	No	High	Poor
NTSC/PAL	Coax	Low	Poor	Yes	Low	No	High	Yes[2]	Low	Best
LVTTL	Copper	Low	Poor	No	Medium	Yes	Low	Yes	Low	Best
LVDS 1 pair 8b/10b	LVDS TP	High	Poor	Yes	Low	No	Medium	No	Medium	Better
LVDS 1 pair 8b/10b	LVDS TP	High	Poor	Yes	Low	Yes[1]	Low	No	Medium	Better
LVDS 1 pair 10b/12b	LVDS TP	High	Poor	Yes	Low	No	Medium	No	Medium	Better
LVDS 1 pair 10b/12b	LVDS TP	High	Poor	Yes	Low	Yes[1]	Low	No	Medium	Better
LVDS 18-bit	LVDS TP	High	Poor	No	Low	Yes	Low	Yes[2]	Low	Better
LVDS 7:1	LVDS TP	High	Poor	No	Medium	Yes	Low	Yes[2]	Low	Better
Ethernet	Copper TP	Low	Good	No	High	No	Medium	No	High	Better
Ethernet	Copper TP	Low	Good	No	High	Yes[1]	Low	No	High	Best
Ethernet	Fiber Optic	Low	Good	No	High	No	Medium	No	High	Better
Ethernet	Fiber Optic	Low	Good	No	High	Yes[1]	Low	No	High	Best
D2B	Copper TP	Low	Very Good	No	High	No	Medium	No	High	Best
D2B	Fiber Optic	Low	Very Good	No	High	No	Medium	No	High	Best
Most	Copper TP	Low	Very Good	No	High	No	Medium	No	High	Best
Most	Fiber Optic	Low	Very Good	No	High	No	Medium	No	High	Best
1394b	Copper TP	Medium	Good	No	High	No	Medium	No	High	Better

Notes:

1. FPGA Contains SERDES for Clock Recovery
2. Not typical interface for LCD panels

Table 1

There is no “one size fits all” for automotive interconnect schemes. A typical automobile will have several communication systems that co-exist, each for different applications. Automotive video systems may use multiple types of

these interconnect systems to optimize performance. The important consideration is to convey the video information as efficiently and as cost effectively as possible from the source to either a processor or a display.

Image Capture

It is crucial to ensure that image capture and processing are carried out as efficiently as possible; again, there are several ways this can be accomplished.

Figure 2 shows some examples of what could be termed “intelligent “ image capture systems. These systems perform some level of local image processing; this could be lens fisheye correction or full object recognition. The information is transmitted over a vehicle multi-media bus to the video controller. This would typically be a Ring- or Bus-based topology using a protocol such as MOST or D2B.
In all three examples, the image sensors shown are from Micron Technology, which manufacture such devices for automotive applications. The first example shows a typical microprocessor-based system performing the control and video data processing functions prior to the data being sent over a physical interface to the display sub-system. The second example has a low-cost FLASH-based CPLD processing the video and the third example uses an SRAM-based FPGA device. In all three examples, the processing element conditions the data for the media over which the information must be sent. In the latter two examples, the use of programmable logic extends the flexibility of reconfigurable hardware. In the last example, a microcontroller such as the LatticeMICO8™ from Lattice Semiconductor can be instantiated within the FPGA for even greater flexibility.

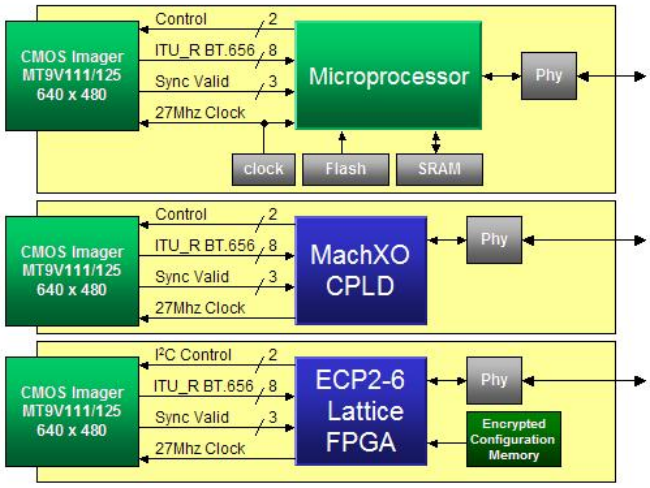

Figure 2 – "Intelligent" Image Capture Systems

One method of sending the captured image is to convert the parallel video data to a serial stream, encoding it in 8b/10b for transmission over a single-pair twisted wire LVDS interface. This interface embeds the clock into the data stream and reduces the number of wires needed to transmit the signal to the video controller. At the receiving end, the system needs to process the data back into its original form. Figure 3 shows four examples of LCD displays. The first three are examples using SERDES circuitry to convert the signals. The third shows an example using an SRAM-based FPGA with integrated SERDES functionality. The use of programmable logic, in this case a Lattice ECP2/2M™ FPGA, already has all the critical timing parameters embedded, so the design engineer will not have to dedicate crucial resources to an onerous and time-consuming task.

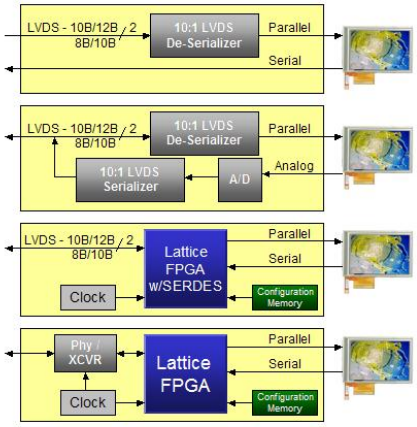

Figure 3 – LCD Displays

Many additional features besides just logic elements are incorporated into the FPGA fabric. One such feature-rich device is the Lattice ECP2M FPGA; its architecture is intended for low-cost applications. The device has embedded SERDES as well as source synchronous I/O capability, embedded memory and DDR interfaces among its features. When coupled with the LatticeMico32™ open core soft processor, the LatticeECP2M device can perform a complete video controller function, as shown in Figure 4. The LatticeMico32 is a 32-bit RISC processor that communicates with internal system peripherals on dual WISHBONE buses. Timers, DMA, Memory Controllers, General Purpose IO, Serial Peripheral Interface and UARTs round out the list of included peripheral devices.

Also shown is an NTSC input (this could also be PAL) from a DVD along with inputs from several image sensors on single-pair LVDS. To drive the LCD panels, there is a direct parallel connection for a local display, in conjunction with the Rear Entertainment display that is connected using the single-pair LVDS. The feedback channel from the rear touch screen is a serial link back to the FPGA. This system also has connections to the CAN automotive control and MOST multimedia buses.

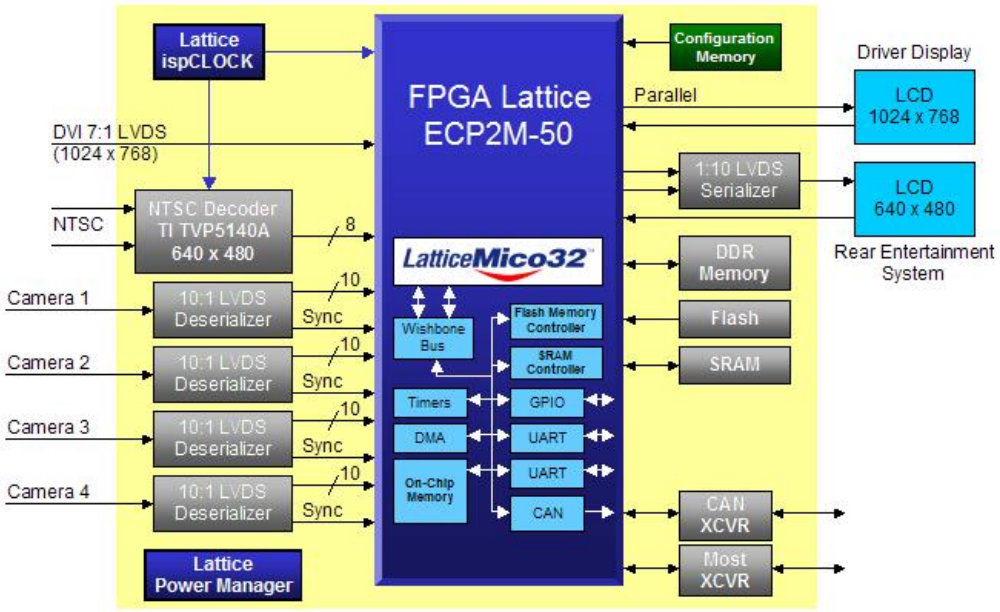

Figure 4 – A Complete Video Controller Function

Summary

No single wiring or protocol will work for all applications. Even when working with automotive video bus systems like MOST and D2B, the need remains to convert to and from the native interfaces on the imager and LCD devices.

This is the strength of reprogrammable FPGAs, and why many designers are using them for the three applications reviewed. Because they are reprogrammable, FPGAs allow designers to easily accommodate changing and emerging standards. In addition, FPGAs are very cost effective and have a very long life cycle, which is in alignment with long life automotive designs and applications.

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