

Introduction

The LatticeECP3™ and LatticeECP2M™ families are low-cost FPGA product lines offering high-end features such as high-speed, embedded SERDES (SERializer/DESerializer) interfaces. These devices feature up to 16 SERDES channels with data rates of up to 3.125 Gbps.

This technical note outlines two experiments that measure the SERDES backplane transmission performance thresholds of the LatticeECP3 and LatticeECP2M devices. These experiments include:

- **Eye Diagram Experiment:** Uses eye diagrams to explore FPGA performance over a standard reference backplane.
- **Data Rate Experiment:** Uses bit error rate measurement techniques to verify FPGA backplane data rate limits at varying speeds and trace lengths.

Both experiments use a bit error rate tester (BERT) for pattern generation, a Tyco HM-Zd as the backplane and a LatticeECP3 or LatticeECP2M FPGA as the device under test. Both experiments collect data at 2.5 Gbps and 3.125 Gbps and use pre-emphasis adjustments to optimize transmitter performance.

Eye Diagram Experiment

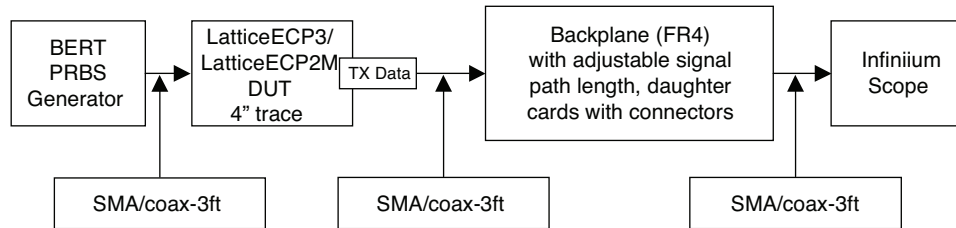
The eye diagram experiment checks the ability of the LatticeECP3 or LatticeECP2M FPGA to drive SERDES signals through a backplane at different pre-emphasis levels and data rates. It provides a visual, qualitative measurement of link performance by persistently sampling the signal at the receive end of the backplane.

In this configuration, a pseudo-random bit sequence (PRBS) pattern is generated and then sent into the LatticeECP3 or LatticeECP2M DUT. The PRBS is looped back and transmitted by the DUT into the backplane. The signal is routed out of the backplane, where it is sampled on an oscilloscope and eye diagrams are assembled. This experiment was performed at 2.5 Gbps and 3.125 Gbps with different levels of pre-emphasis. See Figure 19-1 for an illustration.

The equipment used in this test includes:

- Tyco HM-Zd Quad Route Test backplane with two daughter cards
- Agilent Infiniium DSO81304B 13 GHz oscilloscope
- High-quality coaxial cabling (rated for >3.125 Gbps) with SMA connectors
- Agilent 81250 3.7 GHz Parallel Bit Error Tester (ParBERT)
- Agilent 81130A function/pulse generator
- Agilent E3610A power supply
- Thermonics Thermostream for temperature control
- Internal LatticeECP3 and LatticeECP2M evaluation boards

Figure 19-1. Eye Diagram Experiment Setup



Backplane Specifications

- Tyco Electronics HM-Zd Quad Route Test backplane with daughter cards
- Backplane – 200 mils thick with 14 layers, made from Nalco 4000-FR4 material
- Signal layers 10 mil wide (1/2 copper thickness) designed for 100-ohm differential impedance traces
- Daughter cards – 93 mil thick with 14 layers
- Daughter cards – 6 mil wide, 100-ohm differential impedance traces
- Backplane trace length 40 inches

Test Setup Parameters

- DUT (LatticeECP3 or LatticeECP2M fpBGA)
- SERDES VCC supply values: 1.2V -5%
- Ambient temperature: 125°C
- Data pattern = PRBS (7-bit polynomial)
- Socketed, nominal device

Eye Diagram Measurements

Receiver end eye diagrams are an excellent measurement of expected link performance. This experiment tested a 40-inch length trace path, whereas most applications will have a 12 to 24 inch path. Eye diagrams were taken at 2.5 Gbps and 3.125 Gbps at varied pre-emphasis levels.

Pre-emphasis compensates for signal losses that occur with higher speeds and longer trace lengths. In general, increasing pre-emphasis will increase the signal quality for an improved eye diagram. The FPGA provides eight programmable pre-emphasis levels, available on a per-channel basis. To illustrate the progressive advantages of increased pre-emphasis, Tables 19-1 and 19-2 show eye diagrams taken at six of these pre-emphasis settings, each sampled at both 2.5 Gbps and 3.125 Gbps. Eye opening widths (measured in pS) and peak-to-peak voltage swings (in mV) are listed with each sample. For each of these measurements, larger is better.

Table 19-1. LatticeECP3 Eye Diagram Measurements

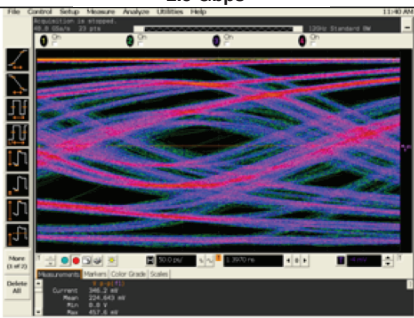
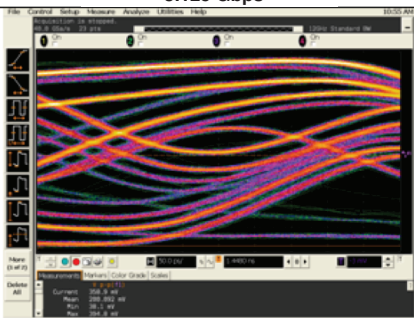
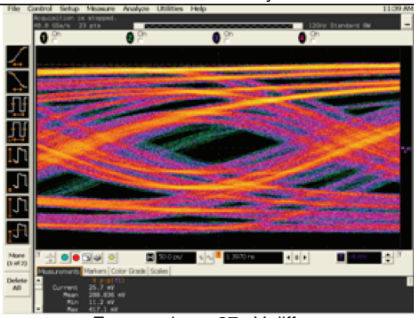
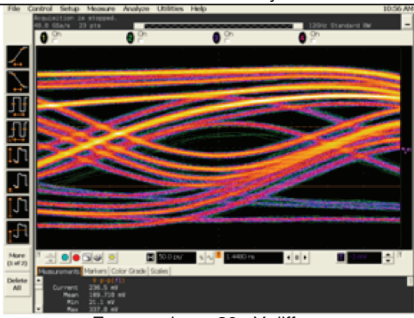
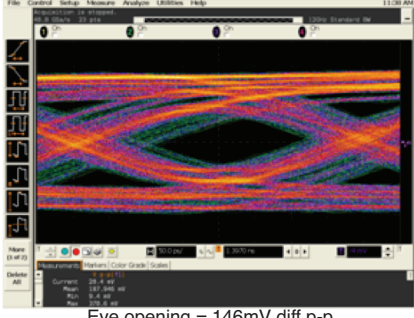
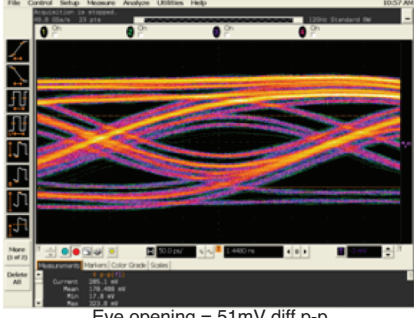
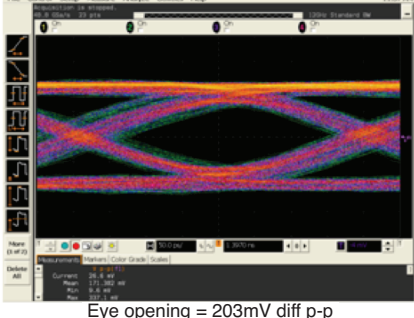
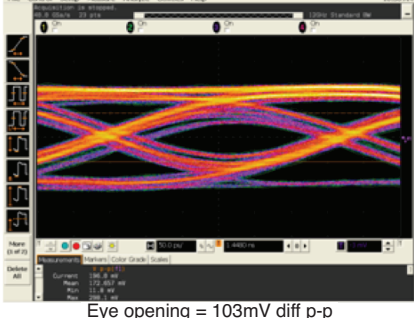
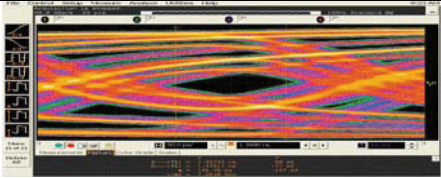
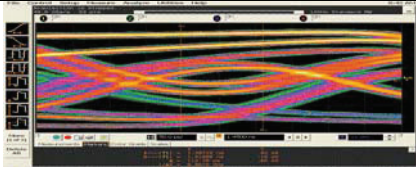
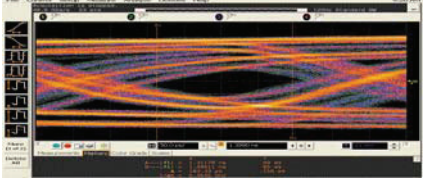
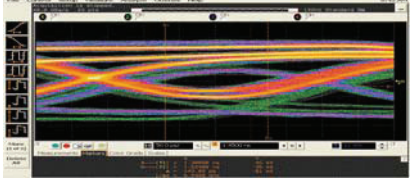
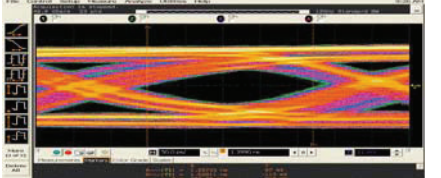
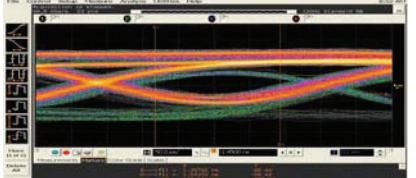
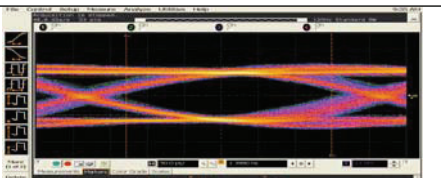
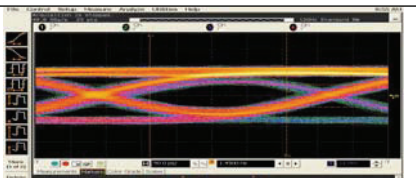
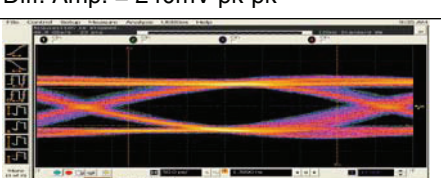
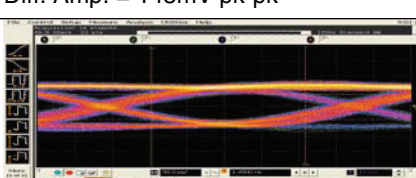
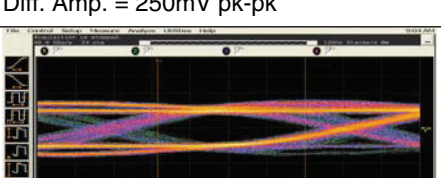
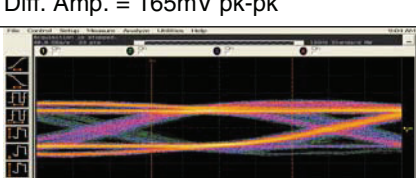
Pre-emphasis	2.5 Gbps	3.125 Gbps
Disabled 0%	 No detectable eye	 No detectable eye
1 (5%)	 Eye opening = 87mV diff p-p	 Eye opening = 30mV diff p-p
2 (12%)	 Eye opening = 146mV diff p-p	 Eye opening = 51mV diff p-p
3 (18%)	 Eye opening = 203mV diff p-p	 Eye opening = 103mV diff p-p

Table 19-2. LatticeECP2M Eye Diagram Measurements

Pre-Emphasis Setting	2.5 Gbps	3.125 Gbps
Pre-Emphasis Disabled	 Eye opening= 140pS, Diff. Amp. = 130mV pk-pk	 Eye opening= 110pS, Diff. Amp. = 45mV pk-pk
1 (16%)	 Eye opening= 180pS, Diff. Amp. = 155mV pk-pk	 Eye opening= 140pS, Diff. Amp. = 80mV pk-pk
2 (36%)	 Eye opening= 220pS, Diff. Amp. = 210mV pk-pk	 Eye opening= 176pS, Diff. Amp. = 123mV pk-pk
4 (44%)	 Eye opening= 265pS, Diff. Amp. = 240mV pk-pk	 Eye opening= 194pS, Diff. Amp. = 145mV pk-pk
5 (56%)	 Eye opening= 270pS, Diff. Amp. = 250mV pk-pk	 Eye opening= 210pS, Diff. Amp. = 165mV pk-pk
6 (80%)	 Eye opening= 270pS, Diff. Amp. = 210mV pk-pk	 Eye opening= 195pS, Diff. Amp. = 160mV pk-pk

Results and Conclusion

Tables 19-1 and 19-2 show that for both data rates the eye opening width and the pk-pk height were maximized at a pre-emphasis of 5. However, if the receiver sensitivity requirements are met, the user might choose a lower pre-emphasis setting in the interest of power savings and lower EM radiation. For example, the LatticeECP3 and LatticeECP2M SERDES receive ports have a minimum input differential sensitivity of 100 mV, so even with pre-emphasis disabled, this requirement would be met at 2.5 Gps (130 mV pk-pk).

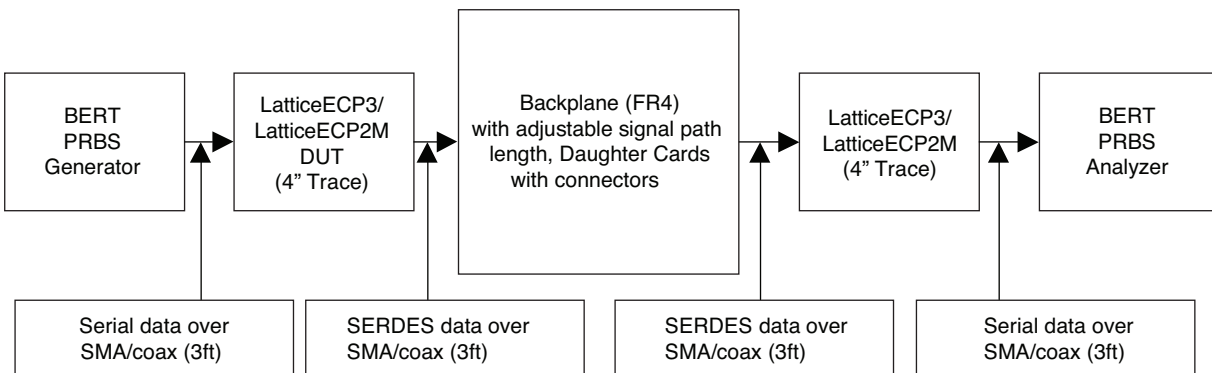
The eye diagrams in this experiment demonstrate that the LatticeECP3 and LatticeECP2M effectively provide high-quality signaling in a long trace, backplane design. These diagrams also show that pre-emphasis settings can be used to optimize SERDES performance.

Data Rate Experiment

The data rate experiment checks the FPGA SERDES transmission performance using a Bit Error Rate Tester (BERT) for expected/received data comparisons in a pass/fail context. The configuration begins by generating a PRBS sequence at a BERT, then sending the pattern into a LatticeECP3 or LatticeECP2M DUT. The FPGA loops the data back to the backplane as a SERDES bitstream. The SERDES data then exits the backplane and is received by the LatticeECP3 or LatticeECP2M (not necessarily the same device as the earlier DUT), which loops the data back to a BERT analyzer. Finally, the BERT compares the incoming bitstream to an expected data pattern and keeps track of how many mismatches are found. A typical expected bit error rate (BER) is less than 1×10^{-12} errors per second. See Figure 19-2 for an illustration.

The equipment used for this test was the same as used for the eye diagram experiment.

Figure 19-2. Data Rate Experiment



Backplane Specifications

- Backplane specifications are the same as for the eye diagram experiment
- Total trace length: 60 inches for 2.5 Gbps testing and 40 inches for 3.125 Gbps testing

Test Setup Parameters

- DUT (LatticeECP3 or LatticeECP2M fpBGA)
- Ambient temperature: 125°C
- SERDES VCC supply values: 1.2V -5%
- Socketed device
- All process variations
- Pre-emphasis setting: 4
- Equalization: 8 db

Data Rate Measurements

The data rate experiment was performed against samples from five process variations. Each sample was tested at 2.5 Gbps and 3.125 Gbps. The pass criterion was BER of less than 1×10^{-12} errors per second.

Results and Conclusions

For all process splits, the FPGA samples achieved a BER of better than 1×10^{-12} at 3.125 Gbps and 2.5 Gbps. This indicates that with a pre-emphasis setting of 4, the LatticeECP3 and LatticeECP2M can drive SERDES data error-free up to 40 inches of backplane at 3.125 Gbps and 40 inches of backplane with margin at 2.5 Gbps.

Conclusions and Design Guidelines

The experiments detailed in this technical note measured the ability of the LatticeECP3 and LatticeECP2M to reliably transmit SERDES data streams in a typical backplane design. The data-rate experiment used a statistical pass/fail scenario, whereas the eye-diagram experiment provided a visual, qualitative measurement. Both experiments concluded that the LatticeECP3 and LatticeECP2M deliver high-quality SERDES transmission over long backplane distances and over a broad range of data rates.

In both experiments, pre-emphasis was used to optimize LatticeECP3 and LatticeECP2M backplane performance. The eye diagram experiment went further to demonstrate that increased pre-emphasis provides a larger eye opening. Pre-emphasis settings are available on a per-channel basis.

Both experiments proved LatticeECP3 and LatticeECP2M performance at 2.5 Gbps and 3.125 Gbps. The data-rate experiment went further to show that devices from all process variations meet these performance goals.

Due to the number of factors in a high-speed PCB design, it is difficult to predict system performance in all scenarios. The data rate experiment illustrated robust performance at 3.125 Gbps over 40 inches in typical conditions, even for the slowest speed grades of the devices. The maximum trace length that can be implemented for an individual system environment may vary and should be evaluated by the individual designer.

The following suggestions will help designers optimize their high-speed LatticeECP3 and LatticeECP2M applications:

1. It is critical that all SERDES path cables and connectors be carefully selected. Cabling should be high-quality coaxial and connectors should be SMA. Both should be characterized for the intended frequency range. The designer should pay close attention to the parasitic performance of these devices.
2. Backplane and port cards should be implemented with good high-speed design practices in mind. For more details see TN1033, [High-Speed PCB Design Considerations](#).
3. To improve the performance of receivers, use the LatticeECP3 or LatticeECP2M programmable equalization settings. For example, 8 db was used in the data rate experiment in this technical note.
4. Use analog circuit simulation tools to assess backplane performance signal integrity issues prior to building models. Contact Lattice for information about obtaining LatticeECP3 or LatticeECP2M SERDES HSPICE models for your simulations.
5. Early lab experimentation of long paths are recommended prior to full system model design in order to reduce technical risk. Eye diagram and bit error rate experiments are recommended.

References

- TN1118, [LatticeSC High-Speed Backplane Measurements](#)
- TN1176, [LatticeECP3 SERDES/PCS Usage Guide](#)
- TN1124, [LatticeECP2M SERDES/PCS Usage Guide](#)
- TN1033, [High-Speed PCB Design Considerations](#)
- TN1114, [Electrical Recommendations for Lattice SERDES](#)

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2007	01.0	Initial release.
March 2007	01.1	Updated LatticeECP2M Eye-Diagram Measurements table.
April 2007	01.2	Updated Eye-Diagram Measurements section.
May 2010	01.3	Added LatticeECP3 FPGA data.
February 2012	01.4	Updated document with new corporate logo.
June 2013	01.5	Updated Technical Support Assistance information.