LatticeSC MACO Core LSCDR1X18 Low-Speed Clock and Data Recovery User's Guide

January 2008 Technical Note TN1122

Introduction

The LatticeSC™ LSCDR (low-speed clock and data recovery) MACO™ core is a fully integrated low-power clock and data recovery (CDR) block designed for low-speed serial communication systems. The clock and data recovery circuit (CDR) is a digital base band circuit that post-processes a binary signal to produce an optimally sampled data bit stream and clock signal that is synchronized with the incoming data (bitclk). The LSCDR1X18 core extracts timing information and data from serial input data rates between 100 to 500Mbps. The LatticeSC design eliminates sensitive noise entry points of clock forwarded schemes, thus making it less susceptible to board-level interaction and helping to ensure optimal jitter performance. It is meant to compliment the high-speed (600Mbps to 3.8Gbps) SERDES available on LatticeSCM40, LatticeSCM80, and LatticeSCM115 devices.

Lattice's MACO cores assists FPGA designer efforts by providing pre-tested, reusable functions that can be easily plugged in, freeing the designer to focus on their unique system architecture. These proven cores are optimized utilizing the LatticeSCM™ architecture, resulting in fast and small cores.

Table 1. Application Specific Speeds for Low-Speed Clock and Data Recovery

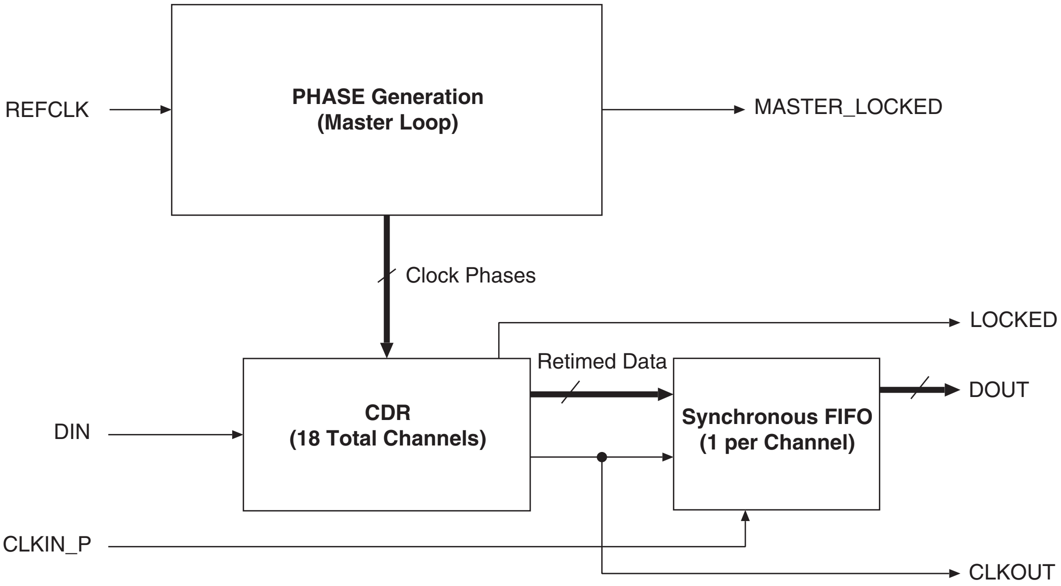
Standard	Speed (Mbps)
OC-3	155
100 Mb Ethernet	125
SMPTE 259M (SD-SDI)	270 (typical)
Generic Operation	100-500

The LSCDR receives clock and data from up to 18 data channels, reproducing the same data re-timed with an appropriate clock phase. The main objective of the circuit is to phase align the recovered clock with the data stream as quickly as possible.

In addition, the LSCDR supports data streams for applications that employ PURESPEED™ I/O interfaces as well as use with the LatticeSC 3.8Gb/s high-speed SERDES CML high-speed interface. Common pin interfaces to the SERDES CML support both SMPTE-259M, SMPTE-292M, and SMPTE-424M (Society of Motion Picture and Television Engineers) digital video standards also known respectively as SD-SDI and HD-SDI. The high-speed SERDES/low-speed SERDES combination also allow OC-3, OC-12, OC-48 SONET applications using the same pin interface.

Point-to-point and backplane applications including OC-3 standards, Fast-Ethernet, regenerators and repeaters, as well as broadband routers and cross-connects are solved using PURESPEED LVDS interfaces to the LSCDR1X18 module.

Figure 1. LSCDR Block Diagram



Functional Overview

The LSCDR1X18 MACO module consists of a phase generator, up to 18 slave CDRs as desired, and a synchronous FIFO. The phase generation stage creates clock phases equally spaced within one reference clock period. It indicates that all phases are properly spaced by generating a LOCK output. The slave CDRs utilize the clock phases and the LOCK signals to determine which clock phase is most closely aligned with the data transition. The CDR then uses the opposite phase to re-time the data. The retimed data and clock are resynchronized to each other through a synchronous FIFO which allows all the slave CDRs operating at the same frequency to be sent on the same clock phase. The entire LSCDR includes a LOCK detect circuit indicating that the clock and data recovery is functioning correctly.

The 18 CDR channels are partitioned into six groupings (A, B, C, D, E, F). These groupings allow three channels to be slaved to each other, using the same read output clock. The serial to parallel conversion is user programmed from 1 to 4 (full-rate, half-rate, or quarter-rate) DOUT outputs. The serial data is shifted to the parallel data bus starting with serial bit0 = parallel bit0.

The module can be connected to any PURESPEED I/O pin or CML SERDES pin via the PCS block. One slave is the minimum channel usage. The design is very flexible and not bounded as the CDR functionality assists in re-timing of any internal delays easing the pinout placement of FPGA designs.

Core Details

The Phase Generator produces either 16 or 8 clock phases depending upon the clock frequency and is set by the software. These clock phases are equally spaced across one clock period. The Phase Generator also produces a lock signal indicating these clock phases are properly aligned. The CDR Lock Detect Circuit uses several different criteria to determine lock due to the difficulty in determining if the output Data matches the input. The CDR lock detect does this using four different criteria.

1. Is the Master Loop locked?
2. If the Master Loop is locked, have 128 positive data transitions happened?
3. Has the data transitioned more than one time in 128 clock cycles (Asynchronous Mode)?
4. Has the clock phase stepped outside the limits to maintain a valid output?

The LOCK mode can be synchronous or asynchronous to the REFCLK. In systems where the reference clock and incoming data rate have 0ppm offset, the synchronous LOCK mode is useful. In this synchronous mode, the reference clock can be stopped and restarted without affecting operation and there is no maximum amount of time between data transitions. The asynchronous LOCK is used where clock and data are slightly offset. A sample retiming diagram for the CDR is shown below. This idealized waveform shows the CDR choosing the clock phase opposite the phase aligned with the positive data edge.

The module has active low resets for the entire block as well as individual channels. The master reset (RSTN) powers down the entire LSCDR core and resets all CDRs, all FIFOs, and re-times the data when RSTN is de-asserted. In synchronous applications it is used to reset all the channels and resynchronize the entire block. The channel resets (RSTN_[A:E][0:3] works well in asynchronous situations to independently resynchronize channel DLLs. These signals reset the FIFOs individually, along with the slave-decoders and the CDR lock detect.

Figure 2. LSCDR Operation Waveform

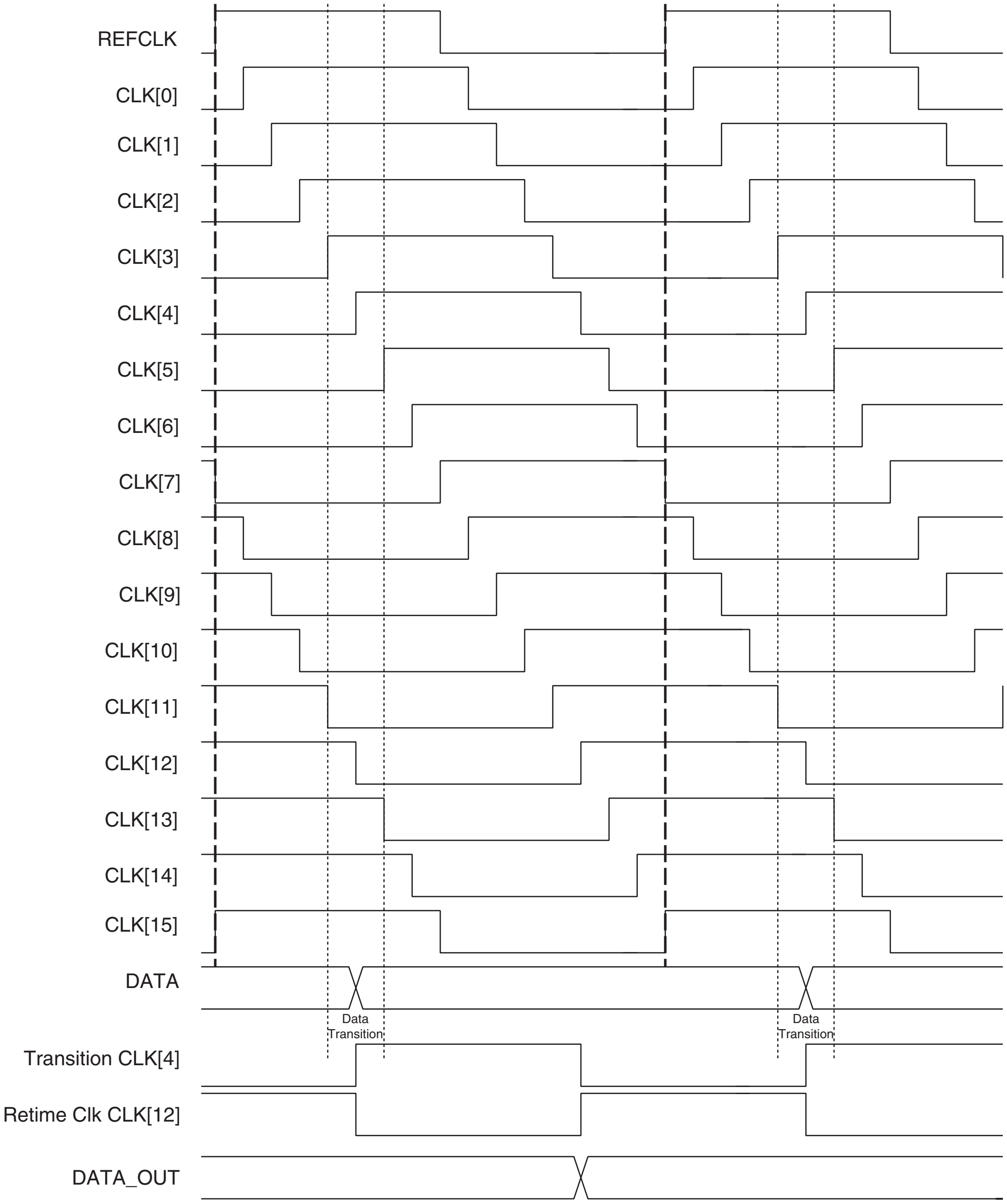
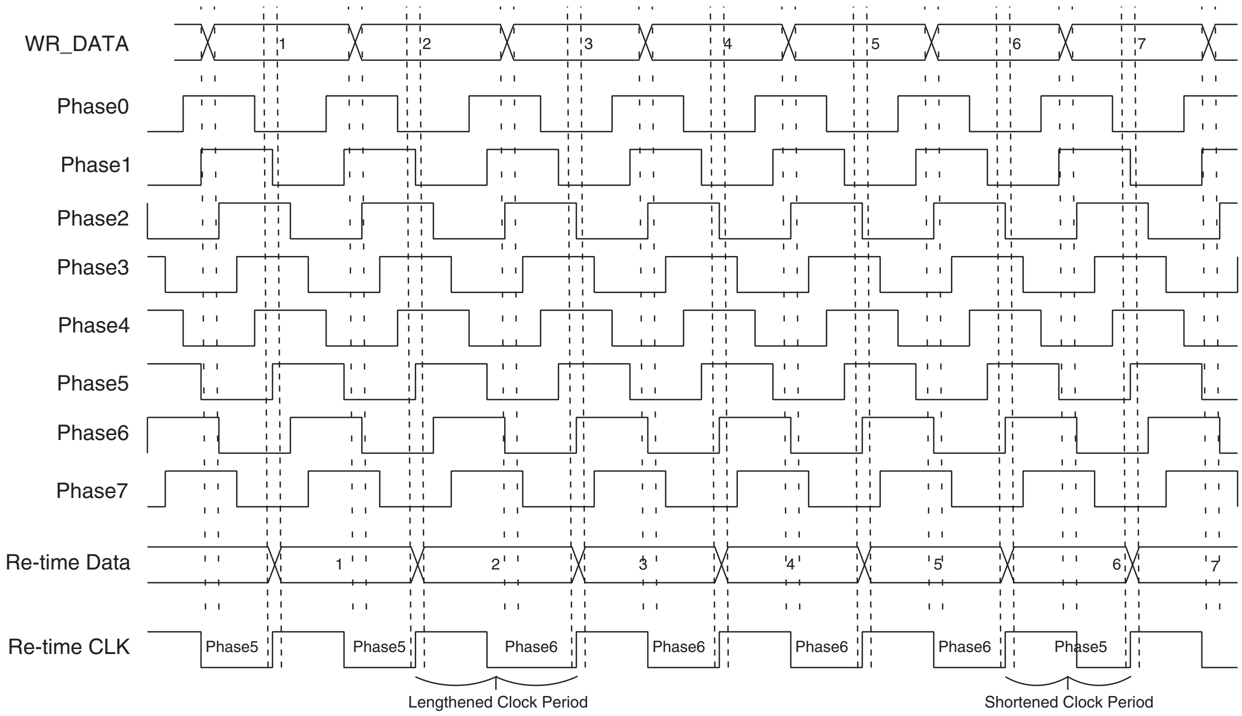


Figure 3 depicts the method the CDR uses to keep synchronized with the data. The module uses a synchronizing method that will either slip or increment the clock phase. The software selection will set either 1/16 or 1/8 of a clock cycle depending upon the mode select of the phase change. This means that as the data moves across the clock phases (due to the ppm offset) the clock phase selected will change.

Figure 3. LSCDR Clock Phase Shifting

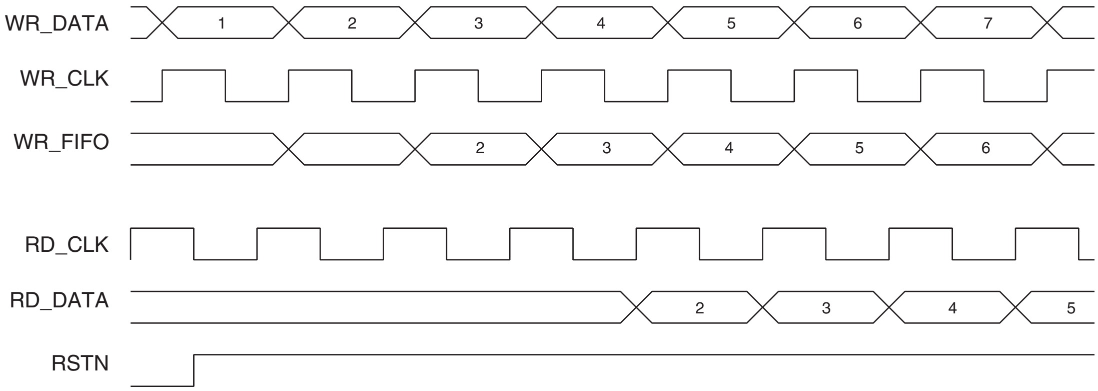


The deep synchronous FIFOs provide resynchronization of the CDR slaves on a per slave basis. The retimed data from the slaves operating within the same frequency range are phase aligned with each other. The FIFOs are synchronous with no bit-stuffing or bit-removal capability. Therefore, the incoming data for the CDR channels within a group must have 0ppm between their respective frequencies.

The data outputs are phase aligned by using the same READ clock to each slave. For example, in a scenario requiring all 18 channels to be phase aligned, the design must supply the same READ clock to all six groups of three channels.

The FIFO is a 4-bit wide/8-word deep FIFO. This allows maximum flexibility in the round trip time of the READ clock. The write FIFO (WR_FIFO) begins immediately after the FIFO begins operation. The read FIFO waits four read clocks before beginning operation. If the read pointer and write pointer overlap, the circuit resets and begins again. The data output can be in a 1-bit (full-rate), 2-bits wide(half-rate), or 4-bits wide(quarter-rate). The output clock from the CDR is output at the appropriate rate based on the chosen FIFO width.

Figure 4. FIFO Startup Waveform



Reference Clock

The LSCDR accepts an external reference clock between 100 and 500MHz. This reference clock can be sourced from either a primary clock or edge clock. This clock source is optionally generated from a PLL in the FPGA or directly from an input pin. When REFCLK is absent the CDR outputs will shut down, however the LOCK will remain high. In asynchronous mode after return of the reference clock, the CDRs will momentarily lose lock and transmit unknown data until they have re-aligned to the data. The DLL will remain synchronized as long as the clock does not fall outside its original frequency. Therefore, when the clock comes back, the CDR will return to normal operation.

Read Clocks

The CDR read clock input available per group CLKIN_ [A:E] _P provides the clock that will read data from the CDR. This is user selected from one of the six groups. The recovered clock comes from the CLKOUT_[A:E][2:0] port of a user-selected master channel. The user optionally connects the master recovered clock back to CLKIN_[A:E] _P primary input clock with FPGA routing. This allows the clock to be routed on FPGA primary or secondary clock routing so that a transfer from the LSCDR to synchronous registers in the FPGA fabric can occur. The CLKOUT_[A:E][2:0] of the master is optionally used to drive the slave CLKIN_[A:E] _P ports. Any group [A:E] can be optionally used as a master.

Pinout Descriptions

The LSCDR1X18 MACO module primitive contains I/O ports along the FPGA interface and is listed in Table 2. The input and output direction is in respect to the LSCDR block. The ports are allocated as needed for a particular number of desired slaves.

Table 2. LSCDR1X18 MACO Core Pinout

Port Name	Direction	Description
REFCLK	Input	Reference clock - User parameterized to route from edge clock or primary clock
RSTN	Input	Active-low reset to entire LSCDR block. User option to connect to GSR if desired using GSR enabled option in GUI.
FORCE_LOCK	Input	Forces the master lock output high. Should be low for normal use.
MASTER_HOLD	Input	1 - Holds the ALU 0 - Normal Operating Mode
MASTER_LOCKED	Output	1 - Master is locked 0 - Master is not locked
CLKIN_[A:E]_P	Input	Clock to read data for one input per Group[A:E]
Per Channel Ports		
DIN_[A:E]0	Input	Serial data input for channel [A:E]0
DIN_[A:E]1	Input	Serial data input for channel [A:E]1

Table 2. LSCDR1X18 MACO Core Pinout (Continued)

Port Name	Direction	Description
DIN_[A:E]2	Input	Serial data input for channel [A:E]2
DOUT_[A:E]0_[3:0]	Output	Output bus for channel [A:E]0
DOUT_[A:E]1_[3:0]	Output	Output bus for channel [A:E]1
DOUT_[A:E]2_[3:0]	Output	Output bus for channel [A:E]2
CLKOUT_[A:E]0	Output	Recovered clock for [A:E]0
CLKOUT_[A:E]1	Output	Recovered clock for [A:E]1
CLKOUT_[A:E]2	Output	Recovered clock for [A:E]2
LOCKED_[A:E]0	Output	1 - Channel [A:E]0 is locked 0 - Channel [A:E]0 is not locked
LOCKED_[A:E]1	Output	1 - Channel [A:E]1 is locked 0 - Channel [A:E]1 is not locked
LOCKED_[A:E]2	Output	1 - Channel [A:E]2 is locked 0 - Channel [A:E]2 is not locked
RSTN_[A:E]0	Input	Reset channel [A:E]0
RSTN_[A:E]1	Input	Reset channel [A:E]1
RSTN_[A:E]2	Input	Reset channel [A:E]2

MACO Technology

The LatticeSCM devices that have the MACO blocks enabled provide pre-engineered IP for the LSCDR module. Figures 5, 6 and 7 illustrate the MACO block layout for the LFSCM40, LFSCM80, and LFSCM115 FPGAs and identify the locations of the two available LSCDR1X18 MACO cores.

Figure 5. LFSCM40 Diagram

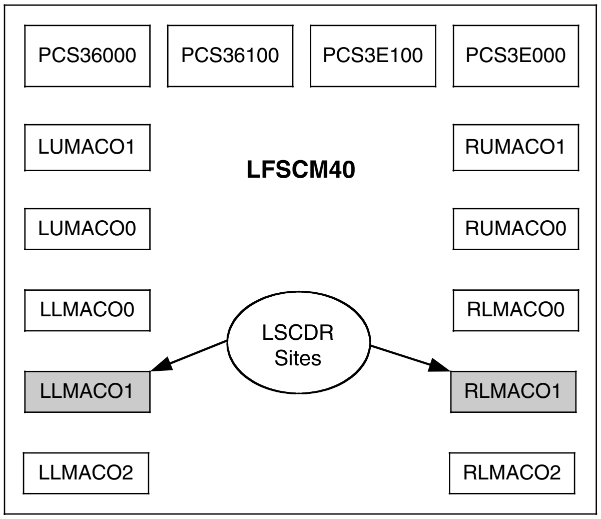


Figure 6. LFSCM80 Diagram

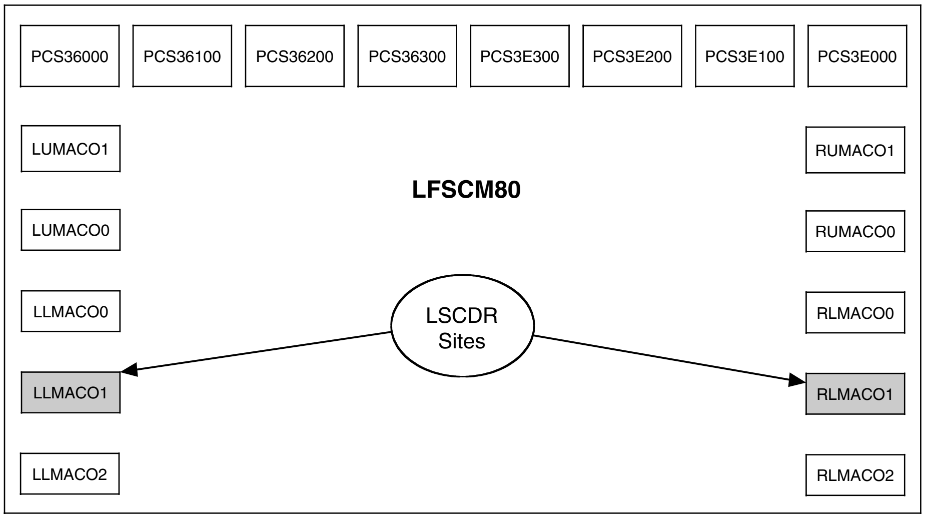
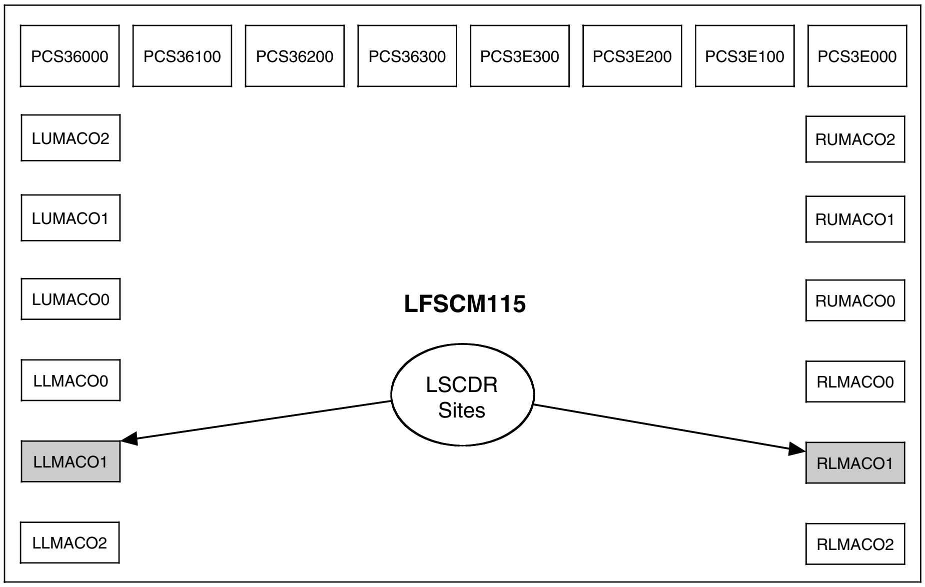


Figure 7. LFSCM115 Diagram

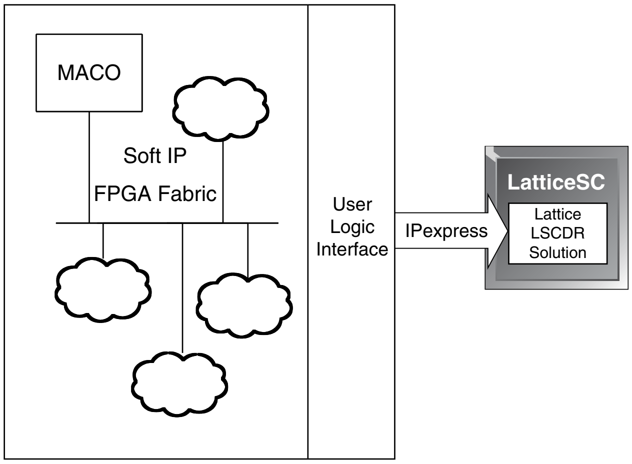


Software Support

Complementing the Lattice ispLEVER® software is the support to generate a number of user-customizable cores with the IPexpress™ utility. This utility will assist the designer to input design information into a parameterized design flow. Designers can use the IPexpress software tool to help generate new configurations of this IP core. Specific information on bus size and clocking are prompted by the GUI and compiled into the FPGA design database. The utility generates templates and HDL specific files needed to synthesize the FPGA design.

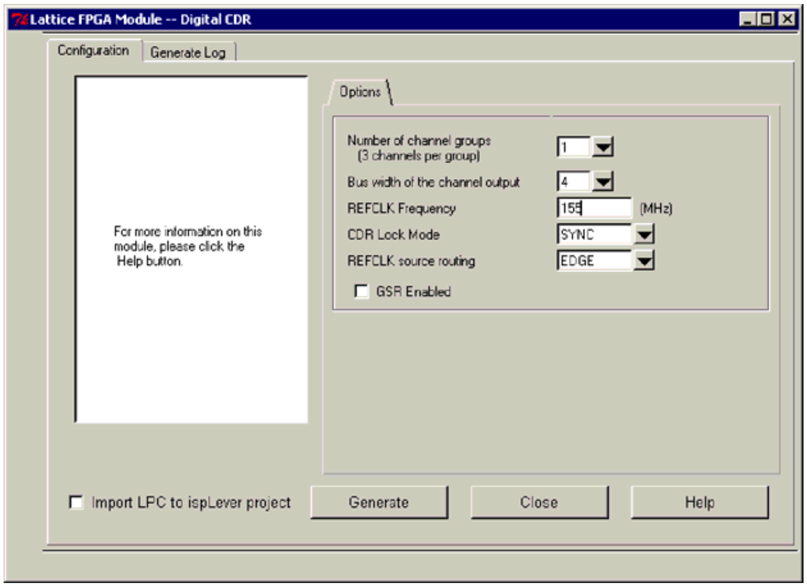
IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help systems. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

Figure 8. LatticeSC Low-speed Clock and Data Recovery MACO Core



The IPexpress GUI permits designers to custom parameterize their application-specific CDR design. The GUI allows selections of clocking, bus widths, and channel provisioning. The user can choose the needed parameters to generate a functional core specific to their needs. This specific information is properly assigned by the software generation to create RTL and ispLEVER-specific files applicable to the FPGA design flow.

Figure 9. LSCDR IPexpress GUI



Lattice FPGA Module -- Digital CDR

For more information on this module, please click the Help button.

Number of channel groups (3 channels per group): 1

Bus width of the channel output: 4

REFCLK Frequency: 155 (MHz)

CDR Lock Mode: SYNC

REFCLK source routing: EDGE

□ GSR Enabled

□ Import LPC to ispLever project

Number of Channels – Creates channels based on a 3-channel per group basis up to 6 groups or 18 channels

Bus Width – This option selects the size of the data output bus from 1 to 4. The output clock will be divided down to match the bus width.

REFCLK Frequency – This information is used to set attributes that will impact the lock time and phase adjustment of the CDR.

CDR Lock Mode – Sync mode is used for systems where there is 0ppm offset between the REFCLK and incoming data rate. Async mode is used for systems where there is an offset between the REFCLK rate and incoming data rate.

REFCLK Source Routing – This option selects either edge or primary clock routing for the connection to the CDR REFCLK.

GSR Enabled – Enables (when selected) or disables (when de-selected) the GSR from re-setting the Digital CDR.

Import LPC to ispLEVER Project – Imports the parameter configuration file (.lpc) into the project currently open in ispLEVER Project Navigator. This option is not available when running IPexpress as a stand-alone tool.

Applications

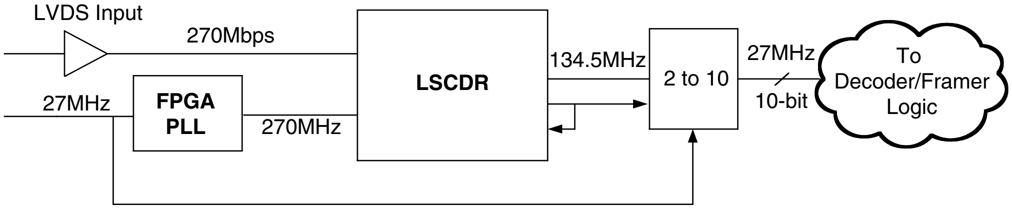
Serial Digital Interface for Video

The SDI standard is defined in the SMPTE standards and is widely used in broadcasting and video production. The SDI standard describes how to carry uncompressed serial, digitized video data between equipment in production facilities over video coax cables including data rate dependant standards for SD-SDI and HD-SDI. The basic electrical specifications of these two standards are the same, but the main difference is that HD-SDI has higher data rate at 1.485 Gbps with the lower speed SD-SDI data rate of 270 Mbps being the most popular rate. The LatticeSC supports SDI in both the SERDES transceiver or PURESPEED FPGA I/O interfaces.

Low-Speed SDI Mode with LVDS Interface

SD-SDI standards are supported using the LVDS capabilities of the PURESPEED I/O. In this solution the 270Mbps serial stream is received directly via the LVDS input. An FPGA PLL multiplies a 27MHz reference clock typically found in video applications. This provides the bit-rate clock and enables jitter-controlled serialization to the LSCDR1X18 MACO module. The input stream is retimed using the LSCDR to create a 134.5Mbps, 2-bit bus. Conversion logic inside the FPGA will convert the 2-bit wide to 10-bit wide word at 27MHz.

Figure 10. SD-SDI Receiver Application



HD-SDI Mode

1.485 Gbps HD-SDI support uses the built-in PCS (Physical Coding Sublayer) capabilities of the flexiPCS™/SERDES of the LatticeSC. It includes the high-speed CML receiver and the CDR capabilities of the built-in PCS block. This application is straightforward and does not require the use of the LSCDR module.

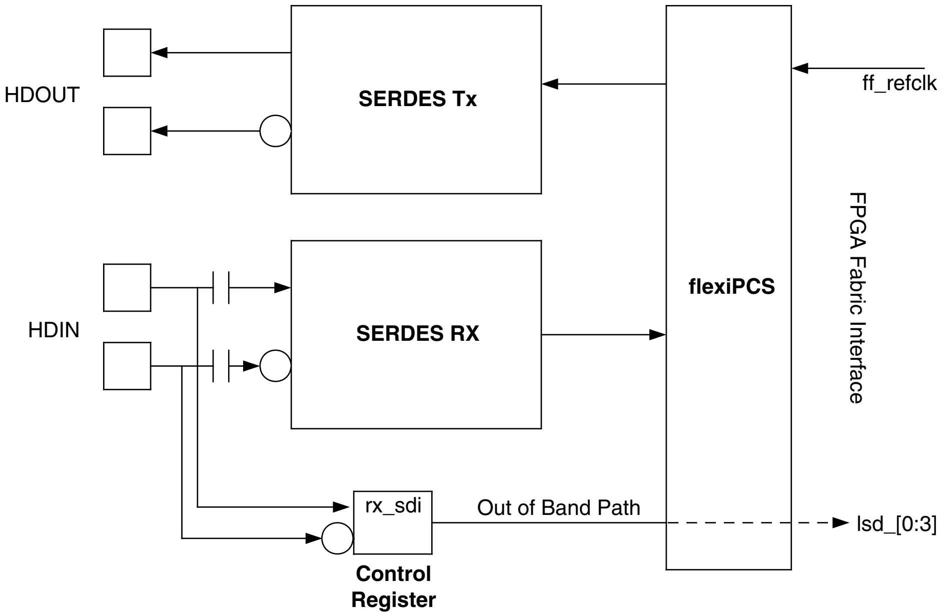
This operation uses the LatticeSC PCS, 10-bit SERDES Only mode. The SERDES Only mode of the flexiPCS block is intended for these applications requiring access to a high-speed I/O interface without the protocol-based manipulation provided in the LatticeSC PCS logic. A single channel can support a fully compliant data link and each quad can support up to four such channels. The mode selection is performed on a per quad basis. Therefore, the selection of a SERDES Only mode for a quad dedicates all four channels in that quad to that SERDES Only mode.

SD/HD-SDI Multi-Mode

The LatticeSC family easily accommodates changing video broadcast and production requirements. The LatticeSC HD/SDI-multi-rate handles bit-rates from 144, 177, 270, 360Mbps and 1.5Gbps for optimum performance. This versatility provides any easy upgrade path from SDI to HDTV technologies while also supporting applications using a wide range of non-standard bit rates.

The LatticeSC can perform both SD-SDI and HD-SDI with the same physical interface. This is possible using the SERDES/PCS data path in conjunction with the LSCDR MACO module for lower SDI data rates. This interface allows a common data path via the SERDES CML I/O and at the same time uses the flexibility of the device when lower speed applications are needed that are outside the range of the SERDES PCS module.

Figure 11. Low Speed Data Path to FPGA Fabric



The above application illustrates the different Rx data path scenarios that can be solved using the same physical connections. The HD-SDI application uses the built-in PCS functionality to complete the de-serialization needed in a typical HD-SDI (1.485Gbps) video application. The operation of the SERDES requires the user to provide a reference clock to each active SERDES quad to provide a synchronization reference for the SERDES PLLs. An FPGA PLL is used to multiply the input clock to the desired reference clock frequency. The reference clock input from FPGA logic is used (ff_refclk) instead of the dedicated input pin reference clock. The ff_refclk inputs for all active quads on a device must be connected to the same clock. The PCS running in half-rate mode will send 20-bit data to the FPGA fabric at 74.25MHz or full-rate sends 10-bit data at 148.5MHz synchronized by the flexiPCS.

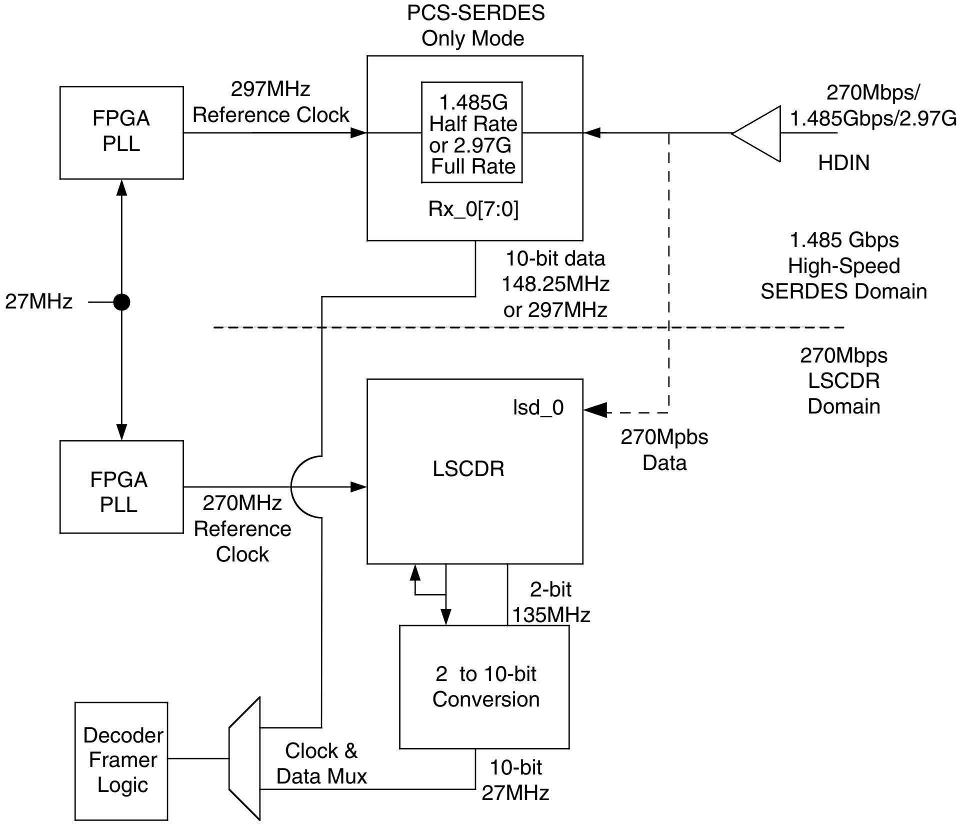
Using the same pins, low-speed (<600Mbps) SDI applications can also be solved. An input path circuit appears in parallel with the high-speed Rx SERDES and can be used to route input data to the LSCDR1X18 MACO. The inputs are passed directly from the SERDES input buffers on HDIN to the FPGA interface and are not locked to the reference clock. The per Quad lsd_[0:3] inputs do not toggle unless enabled via the rx_sdi register selection. They can be enabled on a per channel basis by writing the appropriate Channel Interface Register Offset Address 0x15, bit 2 to a '1'. When driving a SERDES input buffer with a low speed signal, the SERDES input buffer should be set to DC mode, which is done on a per channel basis by writing the appropriate Channel Interface Register Offset Address 0x15, bit 4 to a '1'.

Using this approach, low-speed SDI applications include the use of the LatticeSC LSCDR1X18 MACO core. The data from lsd_[0:3] will supply the input data to the LSCDR core aligned to the reference clock applied directly to the LSCDR. Only two instances of this core are available in any LatticeSC, but each are 18 channels wide. This accommodates the maximum number of high-speed SERDES channels (32) found in any LatticeSC device.

On the output side, the high-speed SERDES is used to transmit either high-speed data, or lower-speed data using decimation. In decimation mode the SERDES continues to run at high speed, but the output data can only change every nth clock where n is the decimation factor.

Figure 12 depicts the multi-mode receiver functionality as previously discussed. It illustrates the use of the same input reference clock. The clocking depicted in Figure 12 will allow a typical video system clock to generate the appropriate clocks for both SDI and HD-SDI interfaces.

Figure 12. SD-SDI and HD-SDI Receiver Physical Implementation Diagram



OC-3

155Mbps SONET applications can utilize the LSCDR MACO module. The 155 Mbps data stream can terminate the SONET data before sending the stream out to a backplane. The LSCDR1X18 MACO module includes the FIFOs required without additional logic. The LSCDR interface provides the input clock and data outputs to protocol dependent IP cores. The LatticeSC PLLs also support the use of 19.4MHz reference clocks found in typical telecom systems. Applications can combine the flexibility to do OC-3 aggregation to OC-48.

Again, a combination of the high-speed SERDES plus the LSCDR allows OC-3, OC-12, and OC-48 on the same pins. This is done in a similar way as shown in Figure 12 with the OC-12 and OC-48 domains done in the high-speed SERDES while OC-3 is done in the LSCDR.

Generic Synchronous Mode

Synchronous mode of the LSCDR MACO can be used to solve the interface challenges of source synchronous interfaces as well as interfaces with CML I/O. This is useful when applied in I/O restricted designs as well as traditional communications interfaces implementing the high speed digital de-skewing and alignment functions used in many protocols.

The LSCDR can select a synchronous LOCK mode allowing input from a source where the data and clock are (0ppm) phase aligned. This mode can be used to implement designs that improve and simplify system level design.

In synchronous LOCK mode, the reference clock or data can be stopped and restarted without affecting the operation for any amount of time. This allows an unlimited run length pattern on data and allows clock switchover on the reference clock from a primary to backup clock. The CDR will also lock without receiving data.

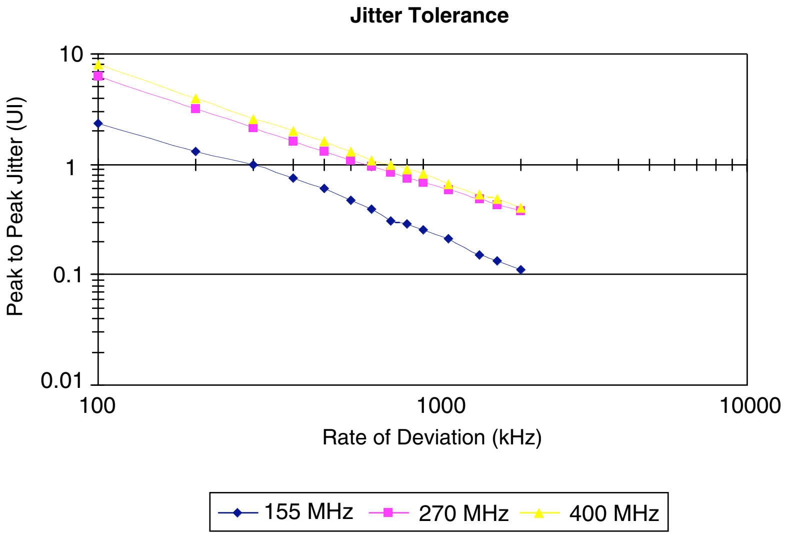
Specifications

Table 3. LSCDR Specifications

LSCDR1X18 Specification[1, 2]	Min.	Typ.	Max.	Units
X16 Mode REFCLK Frequency	100	—	<190	MHz
X8 Mode REFCLK Frequency	190	—	500	MHz
Required REFCLK Duty Cycle	45	50	55	%
Jitter Tolerance[3]	—	—	See Figure 13	UI
Utilized Slave Channels	1	—	18	
Reference Clock/Data Frequency Offset	-500	—	500	ppm
Stream of Non-transitions (Asynchronous Mode Only)	—	—	72	Bits
CDR Lock and Relock Time	—	—	4096	Bits

1. Temperature: -40°C to 105°C.
2. Voltage (VCC Core): 0.95V to 1.26V(typical = 1.0V to 1.2V)
3. Low frequency (<2MHz). Non-transitional run-length: For Async. Mode, see LatticeSC Family Data Sheet, Sync. Mode = NA.

Figure 13. Jitter Tolerance Across Operating Range



Conclusion

LatticeSC offers low-speed CDRs designed to allow easy integration into protocol independent applications automatically locking onto incoming data streams at any rate between 100Mbps and 500Mbps. These MACO based CDRs are area optimized and power efficient and provide flexible connectivity across the entire FPGA. As highlighted in this technical note, the LatticeSC has a balanced mix to handle both low-speed and gigabit systems and also provides multi-mode features combining low and high-speed systems in a single device.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
January 2007	01.0	Initial release.
January 2008	01.1	Global updates to include LatticeSCM115.