LatticeECP2M™ SERDES Evaluation Board

User's Guide

May 2010
Revision: EB25_01.7

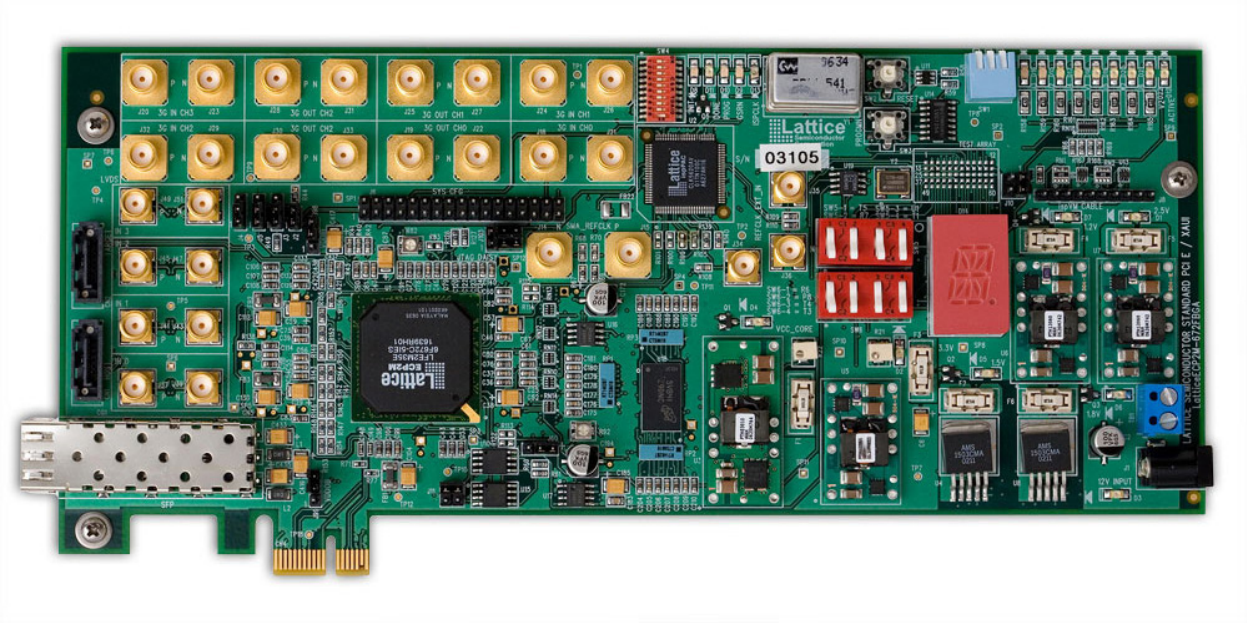
Introduction

This user's guide describes the LatticeECP2M™ SERDES Evaluation Board featuring the LatticeECP2M FPGA. This stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces. The board also includes a PCI Express x1 edge for future expansion. Please note the PCI Express x1 edge is only connected if the board is populated with the LatticeECP2M-50 or larger FPGA.

The evaluation board includes provisioning to connect four high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete customer evaluations of the LatticeECP2M FPGA. The intended use of this guide is to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeECP2M FPGA.

Figure 1. LatticeECP2M SERDES Evaluation Board



Board Features

- LatticeECP2M FPGA in 672-ffBGA package. Default device is LFE2M35E-6FF672C.
- Four SERDES high-speed channels interfaced to SMA test points and clock connections SERDES interface to x1 PCI Express edge fingers (PCI Express x1 edge available with LatticeECP2M-50 or larger FPGA only)
- DDR2 memory device
- SFP Transceiver cage and associated interface (available with LatticeECP2M-50 or larger FPGA only)
- SATA-like connections to SERDES channels (available with LatticeECP2M-50 or larger FPGA only)
- Power connections and power sources
- ispVM® programming support
- On-board and external reference clock sources
  - Interchangeable clock oscillators
  - On-board reference clock management using Lattice ispClock™ devices

- ORCAstra Demonstration Software interface via standard ispVM JTAG connection
- Various high-speed layout structures
- User-defined input and output points
- SMA connectors included (10) for high-speed clock or data interfacing
- Performance monitoring via test headers, LEDs and switches

The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 2 shows the functional partitioning of the board.

Lattice makes its best effort to provide evaluation board designs to help users with evaluation and development. However it remains the user's responsibility to verify proper and reliable operation of Lattice products in their end application by consulting documentation provided by Lattice. Differences in component selection and/or PCB layout in the user's application may significantly affect circuit performance and reliability.

Figure 2. LatticeECP2M SERDES Evaluation Board Block Diagram

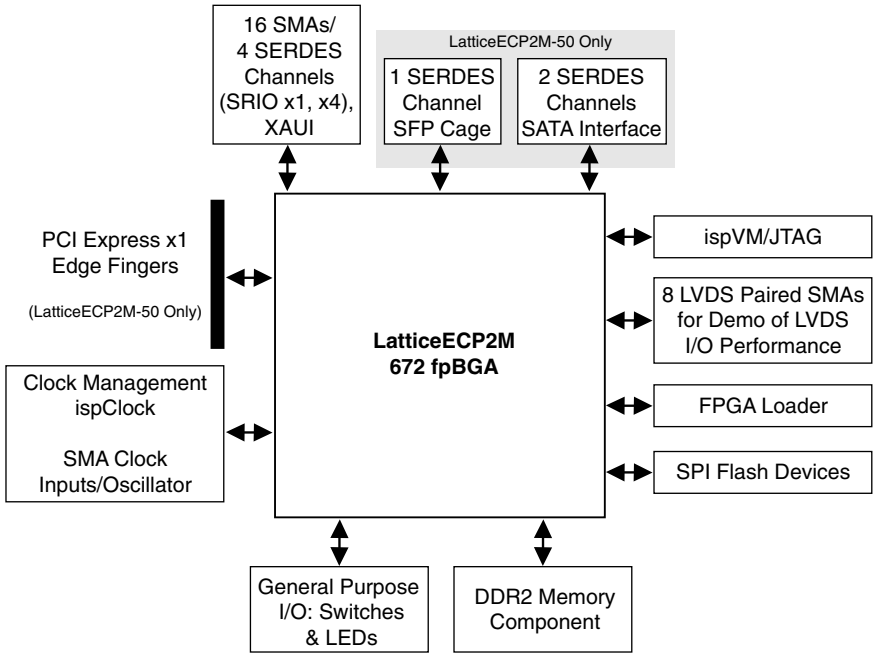
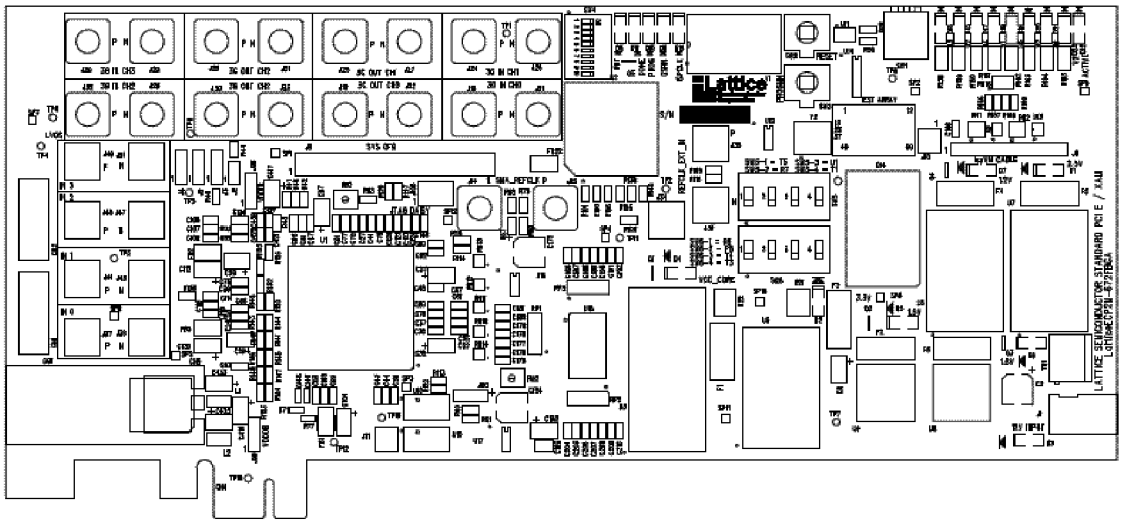


Figure 3. LatticeECP2M SERDES Evaluation Board, Top View



LatticeECP2M Device

This board features a LatticeECP2M FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeECP2M devices in the 672-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeECP2/M Family Data Sheet.

Note: The connections referenced in this document refer to the LFE2M35E-FF672 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family. However, only the LFE2M50E-FF672 device allows full use of the PCI Express x1 edge, SFP and SATA interfaces.

Applying Power to the Board

The LatticeECP2M SERDES Evaluation Board is ready to power on. The board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a bench-top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J1 and plug the wall transformer into an AC wall outlet.

Power Supplies

(see Appendix A, Figure 2)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a bench-top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies use surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses (see Appendix A, Figure 4)

F1	1.2V Core Fuse
F2	1.5V Fuse
F3	3.3V Fuse
F4	1.2V Fuse
F5	2.5V Fuse
F6	1.8V Fuse

Table 2. Board Power Supply Indicators (see Appendix A, Figure 4)

D1	2.5V Source Good Indicator
D2	3.3V Source Good Indicator
D3	12V Input Good Indicator
D4	1.2V VCC Core Source Good Indicator
D5	1.5V Source Good Indicator
D6	1.8V Source Good Indicator
D7	1.2V Source Good Indicator

External power can be supplied via the screw-terminals (TB1) as an alternative.

Table 3. Board Supply Disconnects (see Appendix A, Figure 3)

TB1	Screw terminal for 12 VDC Pin1(square PCB pad) -> +12V DC Pin2 -> Ground

PCI Express Power Interface

Power can be sourced to the board via the PCB edge-finger (CN1). This interface allows the user to provide power from a PCI Express Host board.

Programming/FPGA Configuration

(see Appendix A, Figure 4)

A programming header is provided on the evaluation board, providing access to the LatticeECP2M JTAG port.

Note: An ispDOWNLOAD® Cable is included with each ispLEVER design tool shipment. Cables may also be purchased separately from Lattice.

ispVM Download Interface

J8 is an 10-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device.

Table 4. ispVM JTAG Connector (see Appendix A, Figure 2)

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE
Pin 10	INITN

Programming Daisy Chain

This board includes two Lattice Semiconductor programmable devices that can be programmed in a daisy chain. A jumper setting of J105 controls the chain. Both devices are in the programming chain from the JTAG header J8 with jumpers on J105 across pins {1-2}, pins{3-4} and pins{5-6}. Also a jumper on J10 across pins{1-2} and pins{3-4} are also required for both devices to be in the chain.

If the user desires only to program U1, J105 requires jumpers across pins{1-2} and pins{3-5}. J10 requires only a jumper across pins{1-2}.

Download Procedures

Requirements

- PC with ispVM System v.16.0 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

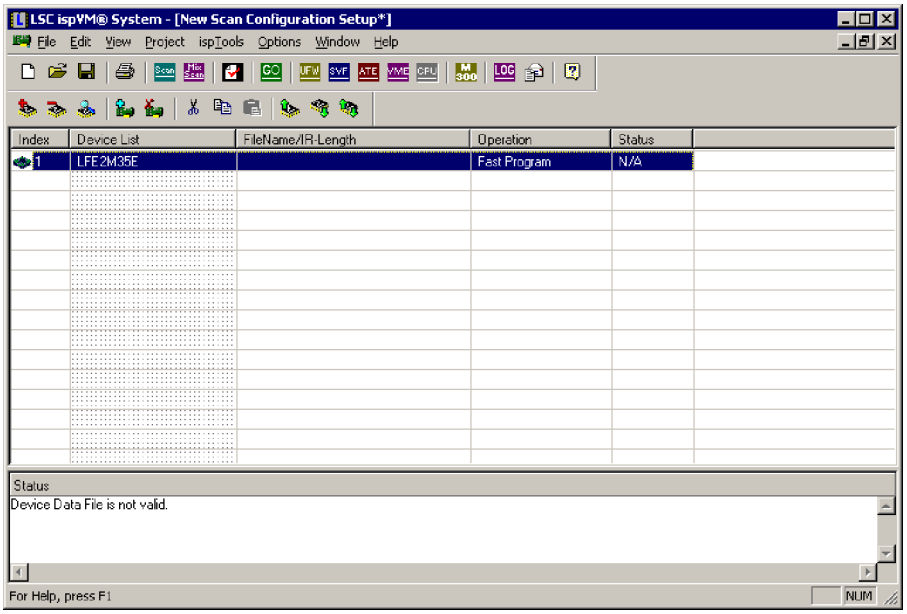
- ispDOWNLOAD Cable (HW-DLN-3C, HW-USBN-2A, etc.)

JTAG Download

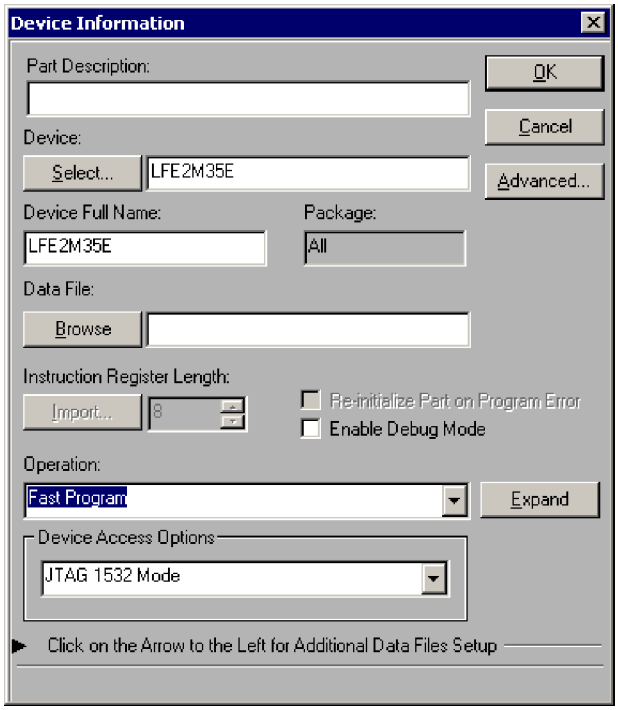
The LatticeECP2M device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2M FPGA device and render the board inoperable.*

1. Press the **SCAN** button located in the toolbar. The LatticeECP2M device will automatically be detected.



2. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.



3. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators

(see Appendix A, Figure 4)

These LEDs indicate the status of configuration to the FPGA.

- D8 (red) illuminated – Indicates that programming was aborted or reinitialized, driving the INITN output low.
- D11 (green) illuminated – Indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D12 (green) flashing – Indicates TDI activity.
- D10 (red) illuminated – Indicates that PROGRAMN is low.
- D9 (red) illuminated – Indicates that GSRN is low.

PROGRAMN and GSRN

(see Appendix A, Figure 4)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and GSRN (SW2). Depressing the button drives a logic level "0" to the device.

CFG [2:0]

(see Appendix A, Figure 4)

The FPGA CFG pins are set on the board for a particular programming mode via the SW1 DIP switch. JTAG programming is independent of the MODE pins and is always available to the user.

On-Board Flash Memory

(see Appendix A, Figure 4)

Two memory devices (U10 and U12) are on-board for non-volatile configuration memory storage.

These two devices occupy the same Flash slot on the board. U10 can be populated with an 8M or smaller 8-pin SOIC device. U12 can be used in place of U10 with a 16-pin TSSOP 64M Flash device.

U15 is supplied as an 8M Flash device.

J11 is used to control the selection of the Flash memory to be accessed.

FPGA Clock Management

(see Appendix A, Figure 8)

The evaluation board includes various features for generating and managing on-board clocks. The clocks are generated from input provided via SMAs (see Table 5) or from crystal oscillators (Y1 and Y2). Y1 is socketed for interchangeability and Y2 is a 100MHz surface-mounted oscillator which is fanned-out around U1 for reference clocks with a fan-out buffer IC.

A 4-pin DIP type oscillator such as the Connor-Winfield XO-400 series can be used in socket Y1.

Both of these input clock sources are routed through the Lattice ispClock5620A programmable clock manager devices (U2). These clock management devices allow for clock synthesis and buffering.

Table 5. SMA Clock Input

SMA	Signal
J35	U2 Reference + Input
J36	U2 Reference - Input

U2 is an ispClock5620A clock generator that allows designers to implement clock distribution networks supporting multiple, synchronized output frequencies using a single device. By integrating a Phase-Locked Loop (PLL) along with multiple output dividers, the ispClock5620A can derive up to five separate output frequencies from a single input reference frequency. PAC-Designer® software (available for download from the Lattice web site at www.latticesemi.com/pac-designer) is used to program the ispClock features.

ispClock supports reference clocks in the range of 10 to 320 MHz. The duty cycle of the clock source does not need to be 50%; the only requirement is that both the HIGH and LOW times of this signal must be 1.25ns or longer. The following standards are supported with either minimal or no external components: LVTTL, LVCMOS, SSTL2, SSTL3, HSTL, LVDS and LVPECL.

When the ispClock5620A is in a LOCKED state, the LOCK output pin goes LOW. The LOCKN pins are connected to amber LED D13 and will illuminate when the LOCKN pin goes low. The lock detector has two operating modes; phase-lock mode and frequency lock mode. In phase-lock mode, the LOCK signal is asserted if the phases of the reference and feedback signals match. In frequency-lock mode the LOCK signal is asserted when the frequencies of the feedback and reference signals match.

U2 is controlled by SW4 or from a predefined connection to U1 (LatticeECP2M). The DIP switch controls the ispClock device. The reference clock selection and device reset is controlled using the switches. The switches that control the ispClock outputs can be synchronously controlled by the SGATE output on a bank-by-bank basis or tri-stated on an output-by-output basis using the OEXb and OEYb inputs. All outputs may be tri-stated by bringing the GOEb input high.

The VCCO voltage is board-connected to 2.5V or 3.3V based on the on-board connection of FB21 or FB22.

The output clocks of U2 are routed to devices to provide system level clocking. These pre-defined board clocks are routed to input LatticeECP2M input clock pins for SERDES reference clocks, primary clocks, PLL inputs and DLL inputs as well as connection to a SMA (J34). This SMA is 50-ohm terminated for off-board interconnection to test equipment.

A clock input to the ispClock device can be provided from the PCI Express edge-fingers. This is accomplished by configuring the on-board resistor jumpers R79 and R80 (see Appendix A, Figure 5).

The board has various component stuffing options to provision specific clock source variations. Table 6 outlines the need to open or short connections on the board as well as required terminations for proper signal quality.

Table 6. Clock Source Connection Variations

Clock Source	R67	R68	R69	R70	R100	R101	R215
Default	short	short	50-ohm	50-ohm	short	short	100-ohm
Y1 or Y2 Clock Source	open	open	open	open	short	short	open
J14/J15 CML or LVDS source	short	short	50-ohm	50-ohm	open	open	open
Core Ref Clock	open	open	don't care	don't care	don't care	don't care	don't care

SERDES

(see Appendix A, Figure 5)

SERDES Reference Clock

The 50-ohm terminated SMA connectors provide supply reference clocks directly to the LatticeECP2M device from the ispClock management device. This device drives clocks to both SERDES quads via 100-ohm LVDS signaling. The on-board clock oscillators mentioned in previous sections of this document can be chosen to drive the same SERDES reference clocks. In addition, the board can be provisioned to source the clock from the PCI Express edge-fingers directly to the SERDES REFCLK pins.

SERDES Channels

Surface Mounted SMA Connections

(see Appendix A, Figure 5)

DC coupled top-mounted SMA connectors connect to the four SERDES Tx and Rx channels. These pins are directly coupled to the designated SMA connector, creating a path for both input and output differential data.

Table 7. SERDES Connectors (see Appendix A, Figure 5)

SMA	Channel Name
J18	U_HDINP0
J21	U_HDINN0
J24	U_HDINP1
J26	U_HDINN1
J29	U_HDINN2
J32	U_HDINP2
J20	U_HDINP3
J23	U_HDINN3

SMA	Channel Name
J19	U_HDOUTP0
J22	U_HDOUTN0
J25	U_HDOUTP1
J27	U_HDOUTN1
J30	U_HDOUTP2
J33	U_HDOUTN2
J28	U_HDOUTP3
J31	U_HDOUTN3

SERDES SFP Transceiver Interface

(see Appendix A, Figure 5)

A small form-factor pluggable (SFP) transceiver cage is included for evaluation of SFP specific protocols. The PCB includes the appropriate power and high-speed circuitry needed for the SFP standard transceiver. *Note: this interface is only available on boards featuring a LatticeECP2M-50 or larger FPGA.*

Table 8. SFP Connections to SERDES Pins (see Appendix A, Figure 5)

SFP Rx	Channel Name
RD+	L_HDINP3
RD-	L_HDINN3

SFP Tx	Channel Name
TD+	L_HDOUTP3
TD-	L_HDOUTN3

Table 9. SFP Control and Status Connections to FPGA

SFP Pin	FPGA BGA
TxFault	M3
TxDis	L8
LOS	N2
RateSel	N3

SFP Pin	FPGA BGA
ModeDef0	N1
ModeDef1	M1
ModeDef3	M6

SERDES SATA Channels

(see Appendix A, Figure 5)

Connections are included to attach SATA type cables to SERDES channels for board-to-board or loopback purposes. The connectors are configured using the 7-pin SATA specifications. *Note: this interface is only available on boards featuring a LatticeECP2M-50 or larger FPGA.*

Table 10. SERDES to SATA Connector

CN1 Pin	FPGA BGA
TxFault	M3
TxDis	L8
LOS	N2
RateSel	N3

CN2 Pin	FPGA BGA
ModeDef0	N1
ModeDef1	M1
ModeDef3	M6

SERDES PCI Express Channels

(see Appendix A, Figure 5)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1) to fit directly into an x1 host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections. *Note: this interface is only available on boards featuring a LatticeECP2M-50 or larger FPGA.*

FPGA Test Pins

(see Appendix A, Figure 10)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to switches and LEDS designated according to the following table.

Table 11. FPGA Test Pins (see Appendix A, Figure 7)

Switch	BGA	Netname
SW6D	T3	Switch1
SW6C	T4	Switch2
SW6B	P8	Switch3
SW6A	R6	Switch4
SW5D	T1	Switch5
SW5C	U1	Switch6
SW5B	R7	Switch7
SW5A	T5	Switch8

LED	BGA	NetName
D16	U3	RED1
D17	U4	YELLOW1
D19	U5	GREEN1
D21	U6	BLUE1
D15	U2	RED2
D18	V1	YELLOW2
D20	W2	GREEN2
D22	V2	BLUE2

Note: LEDs will illuminate if connected to an un-programmed FPGA pin. It is recommended that a pull-down be programmed on FPGA output pins.

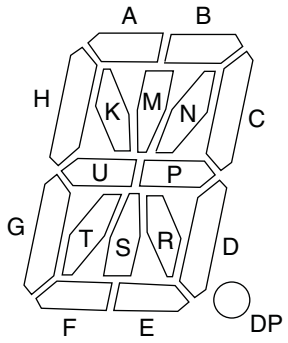
17-Segment LED Display

(see Appendix A, Figure 10)

General-purpose FPGA pins are connected to a 17-segment display according to the following table. These pins can be driven low to illuminate the display segments.

Figure 4. 17-Segment LED Display

Segment	BGA
A	H2
B	J3
C	G1
D	H3
E	J7
F	H5
G	G5
H	G6
K	F3
M	J8
N	E1
P	J9
R	E3
S	F5
T	D3
U	F6
DP	C2



Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit evaluations of several types of FPGA I/O buffers. The use of several termination schemes permits easy interfaces for the type of buffer.

Table 12. FPGA I/O Test SMA Connectors (see Appendix A, Figure 9)

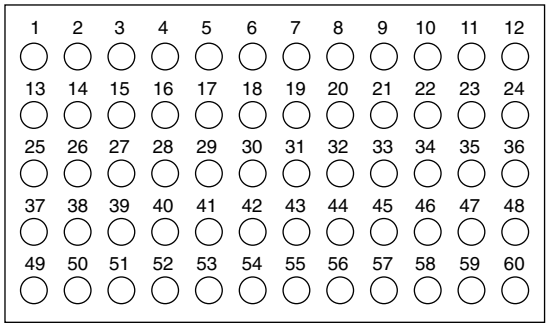
SMA Designation	Name	LFE2M35E Signal	672-BGA	Termination Description	Termination Resistor(s)
J37	LVDS_INP0	PR37A	N23	100-ohm Differential	R130
J39	LVDS_INN0	PR37B	M21		
	LVDS_INP1	PR41A	P24	100-ohm Differential	R132
	LVDS_INN1	PR41B	P23		
J45	LVDS_INP2	PR51A	T24	100-ohm Differential	R134
J47	LVDS_INN2	PR51B	U24		
J49*	LVDS_INP3	PR57A	V24	100-ohm Differential	R136
J51*	LVDS_INN3	PR57B	W24		
J38	LVDS_OUTP0	PR50A	T23	100-ohm Differential	R131
J40	LVDS_OUTN0	PR50B	T22		
J42	LVDS_OUTP1	PR53A	V26	100-ohm Differential	R133
J44	LVDS_OUTN1	PR53B	V25		
J46	LVDS_OUTP2	PR55A	W26	100-ohm Differential	R135
J48	LVDS_OUTN2	PR55B	W25		
J50	LVDS_OUTP3	PR59A	Y26	100-ohm Differential	R137
J52	LVDS_OUTN3	PR59A	AA26		

Test Pad Array

A 5 x 12 array of test pads are provided for the user to utilize for test points. This array provides 48 general I/O contacts and 12 ground points.

Table 13. Test Pad Array BGA Reference

Test Points Array on Component Side



AA20	V17	W20	AC25	AC23	AD26	AB21	AC22	AD12	AF12	W14	AB13
AA13	AE9	AF9	AB6	E23	E24	P26	P25	U21	U19	V21	J2
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
K7	J6	K5	L5	P5	N6	P4	R3	W5	Y4	U8	W6
G7	G8	E6	D5	G12	C8	E13	H17	E14	G17	D17	E17

High Speed Test Point

DP1

(see Appendix A, Figure 9)

General-purpose FPGA pins are available to a differential test pad. These connections allow a high-impedance probe to measure the performance of a coupled- differential output buffer pair.

DDR2 Memory

U18

(see Appendix A, Figure 10)

The LatticeECP2M SERDES Evaluation Board is equipped with an 84-ball BGA DDR2 SDRAM memory device such as the Micron MT47H16M16BG-3 device. The DDR2 memory interface includes a 16-bit wide device. The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeECP2M device.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP2M35 SERDES Evaluation Board (Non-RoHS, Obsolete)	LFE2M35E-S-EV	
LatticeECP2M50 SERDES Evaluation Board (Non-RoHS, Obsolete)	LFE2M50E-S-EV	
LatticeECP2M50 SERDES Evaluation Board (RoHS Compliant)	LFE2M50E-S-EVN	

Known Issues

The current silkscreen markings by J28 and J31 are incorrectly labeled. They should be labeled 3G OUT CH3.

SATA Host interface (CN1) – Receive data must be polarity-inverted in FPGA design for correct connection.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
December 2006	01.0	Initial release.
December 2006	01.1	Includes new SERDES schematic in Appendix A.
March 2007	01.2	Added Ordering Information section.
April 2007	01.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
May 2007	01.4	Updated SW6D switch information in FPGA Test Pins table.
February 2008	01.5	Updated FPGA Clock Management text section and added Clock Source Connection Variations table.
		Updated SERDES Connectors table.
		Added Known Issues section.
		Updated SERDES schematic in Appendix A.
January 2009	01.6	Updated ordering information.
May 2010	01.7	Updated Known Issues section.

Appendix A. Schematic

Figure 5. Cover Page

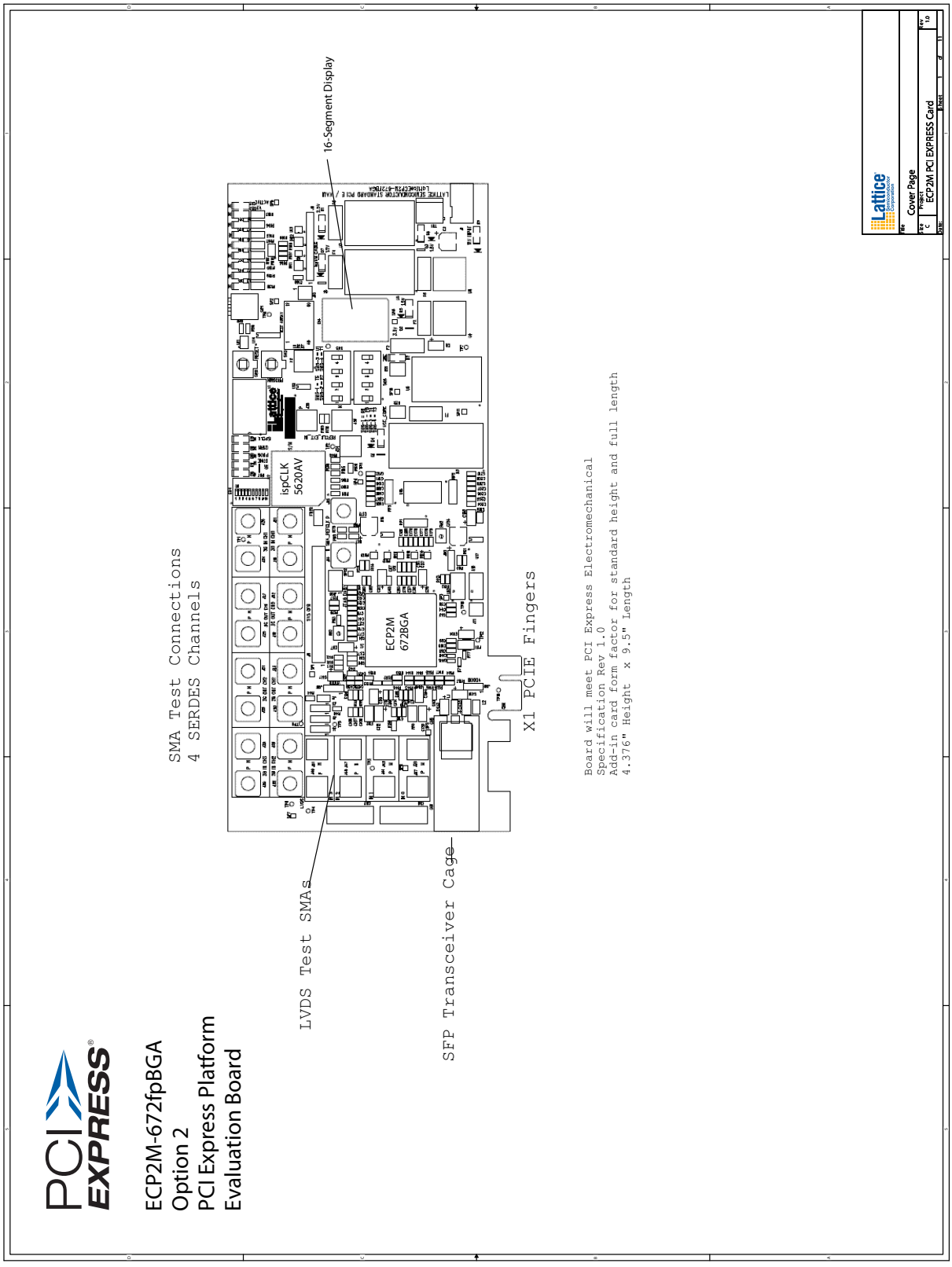


Figure 6. DC/DC Conversion

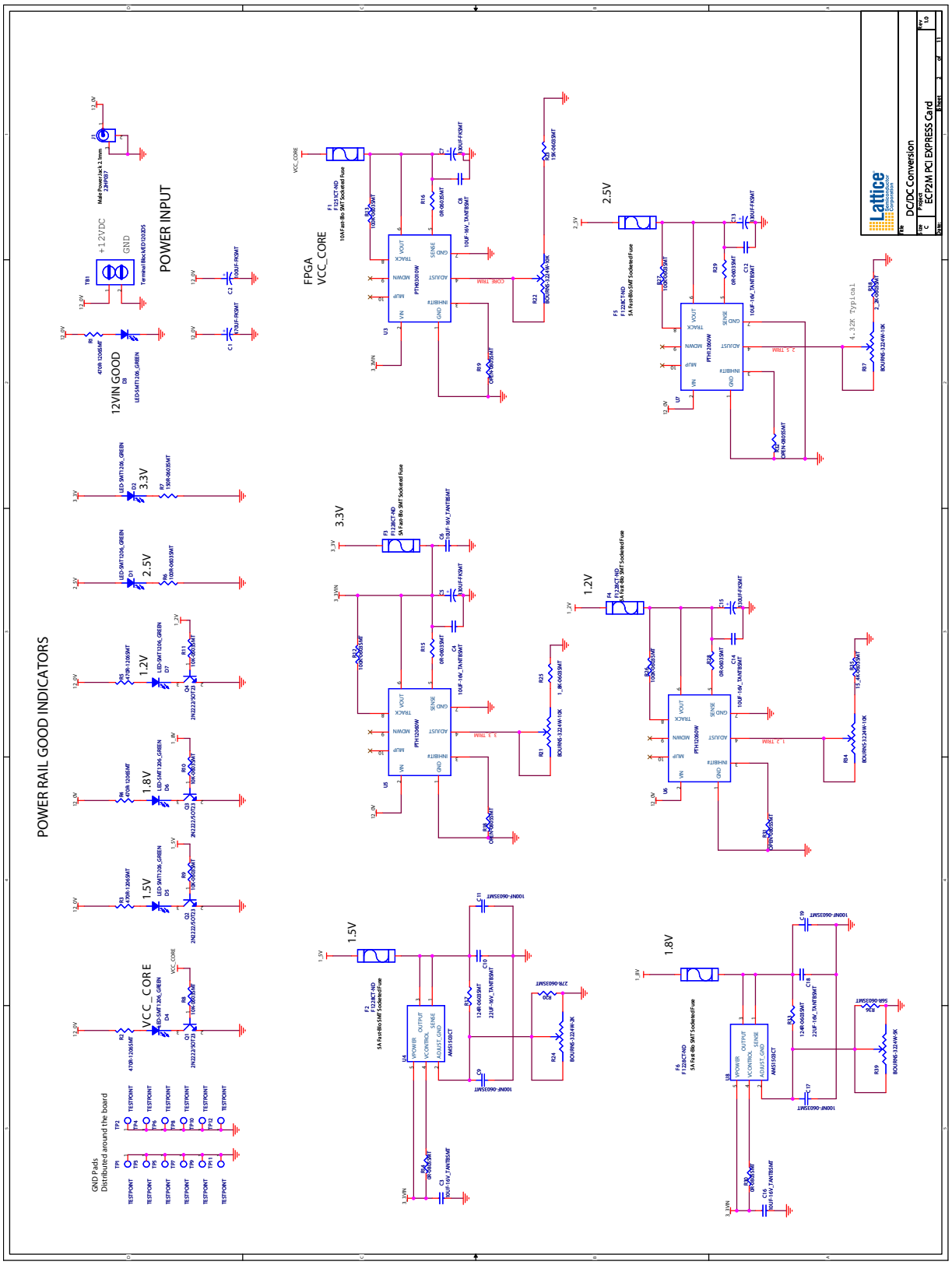


Figure 7. Power Supplies

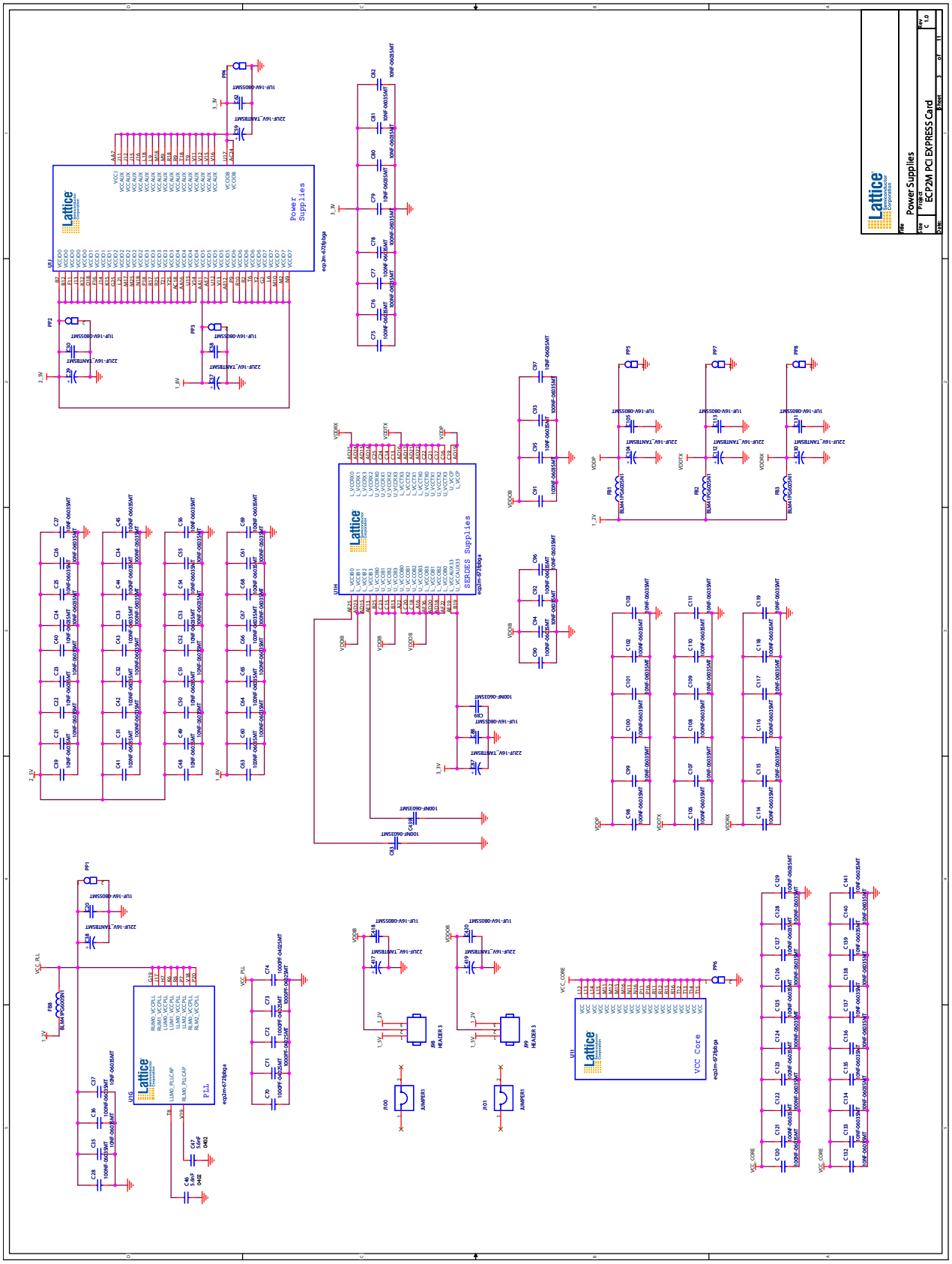


Figure 8. Configuration/Testpoints

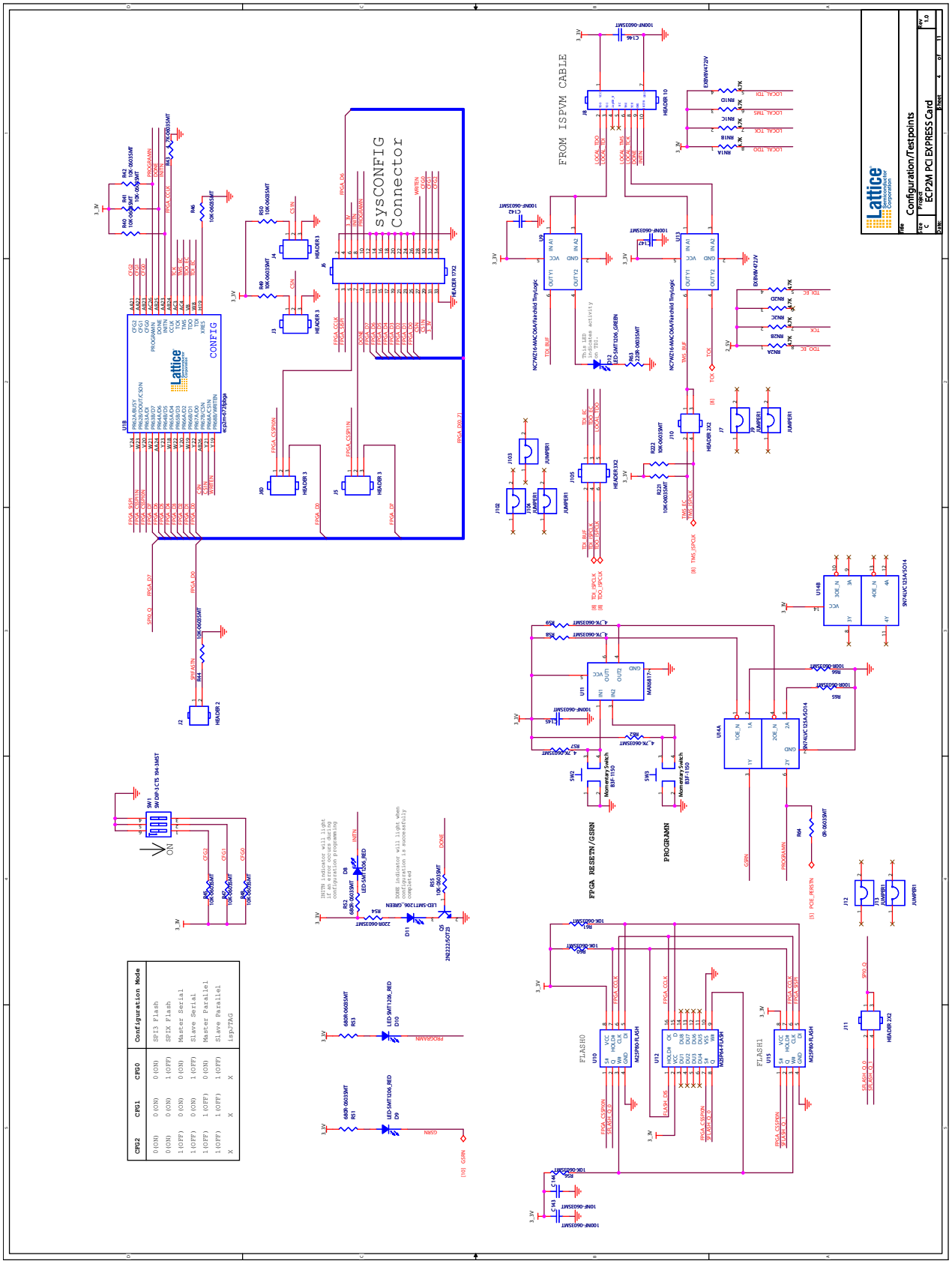


Figure 9. SERDES

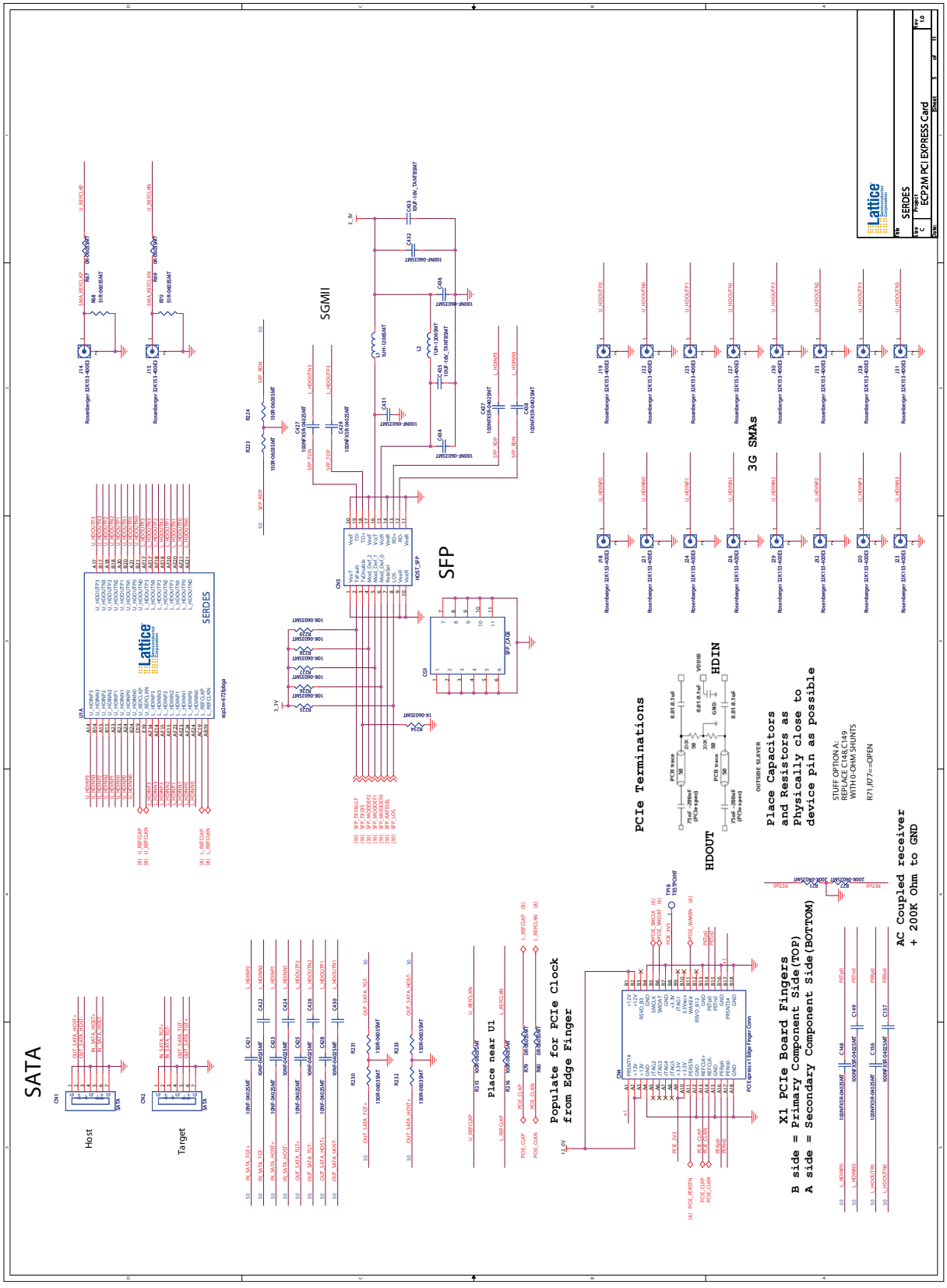


Figure 10. DDR2 FPGA Controller

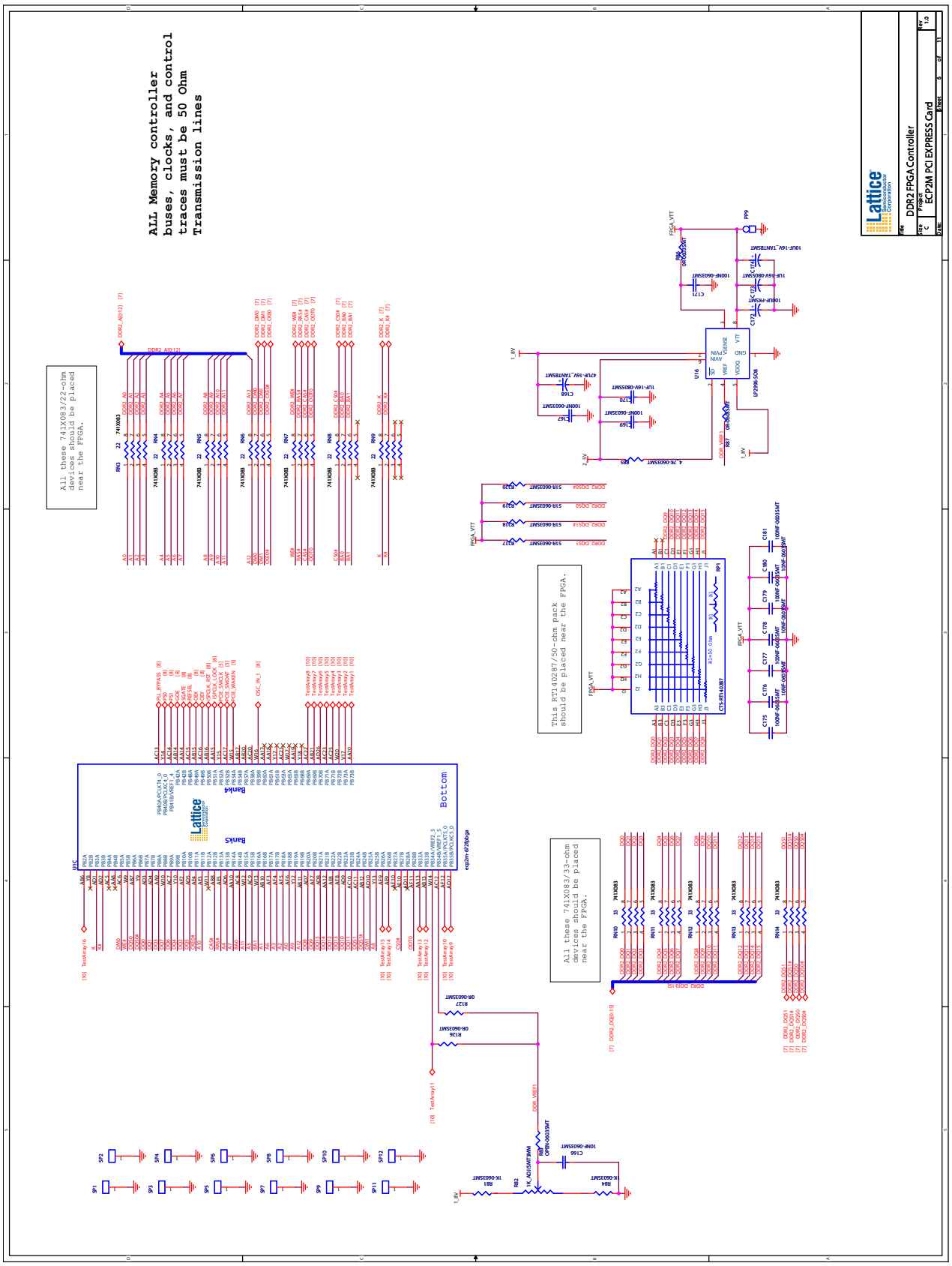


Figure 11. DDR2 Device/Termination

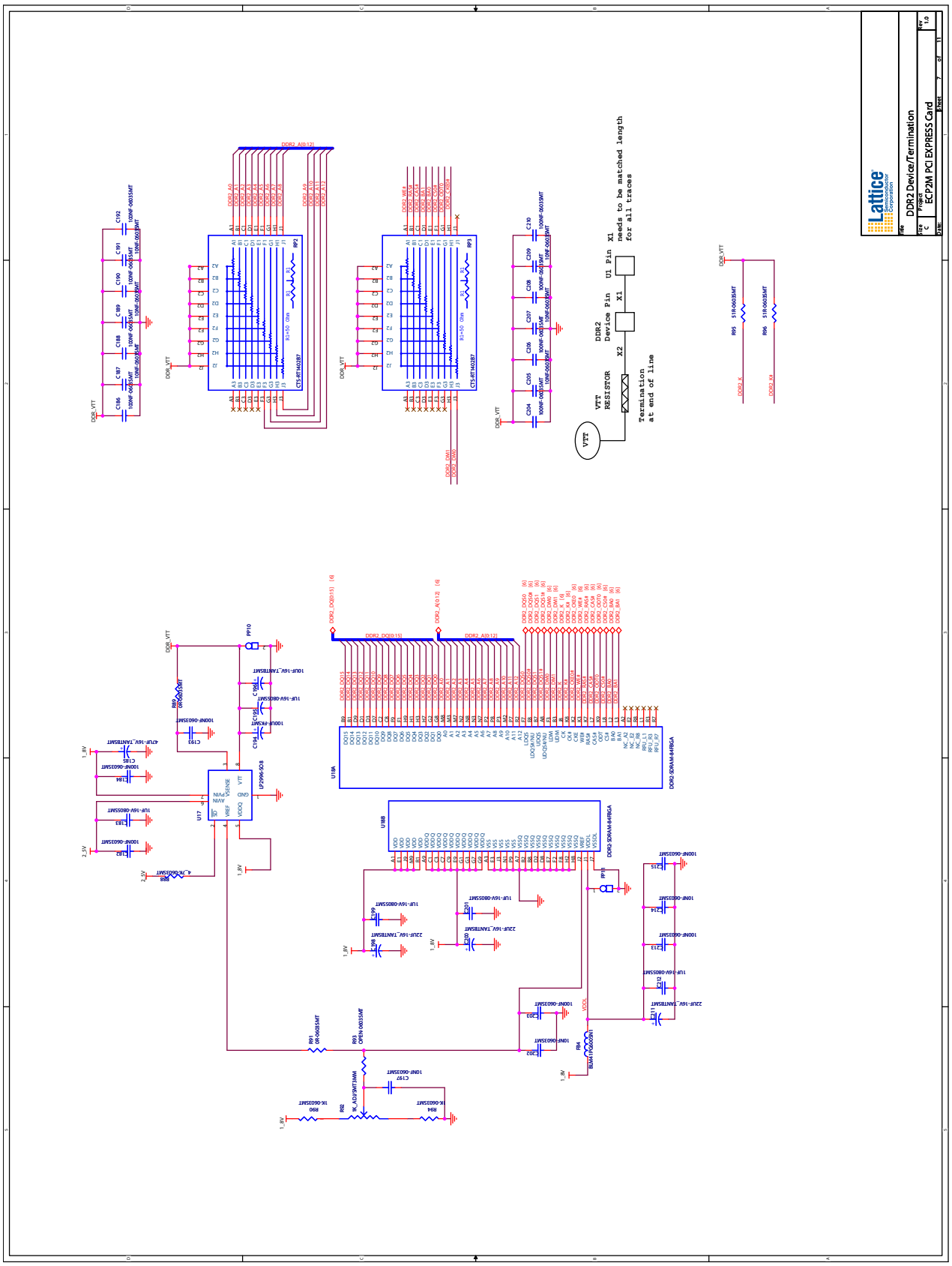


Figure 12. Clocks

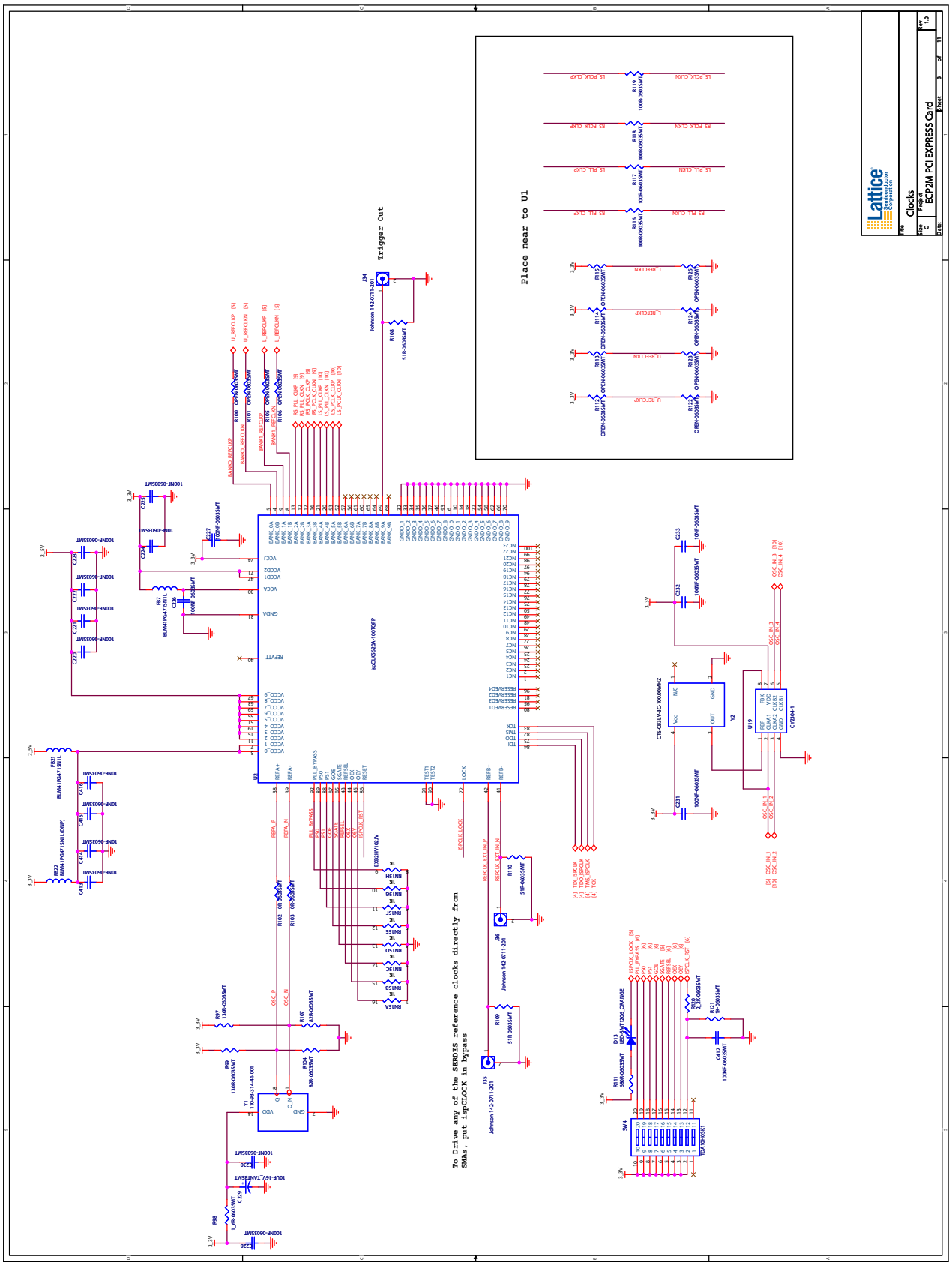


Figure 13. Differential I/O Loops

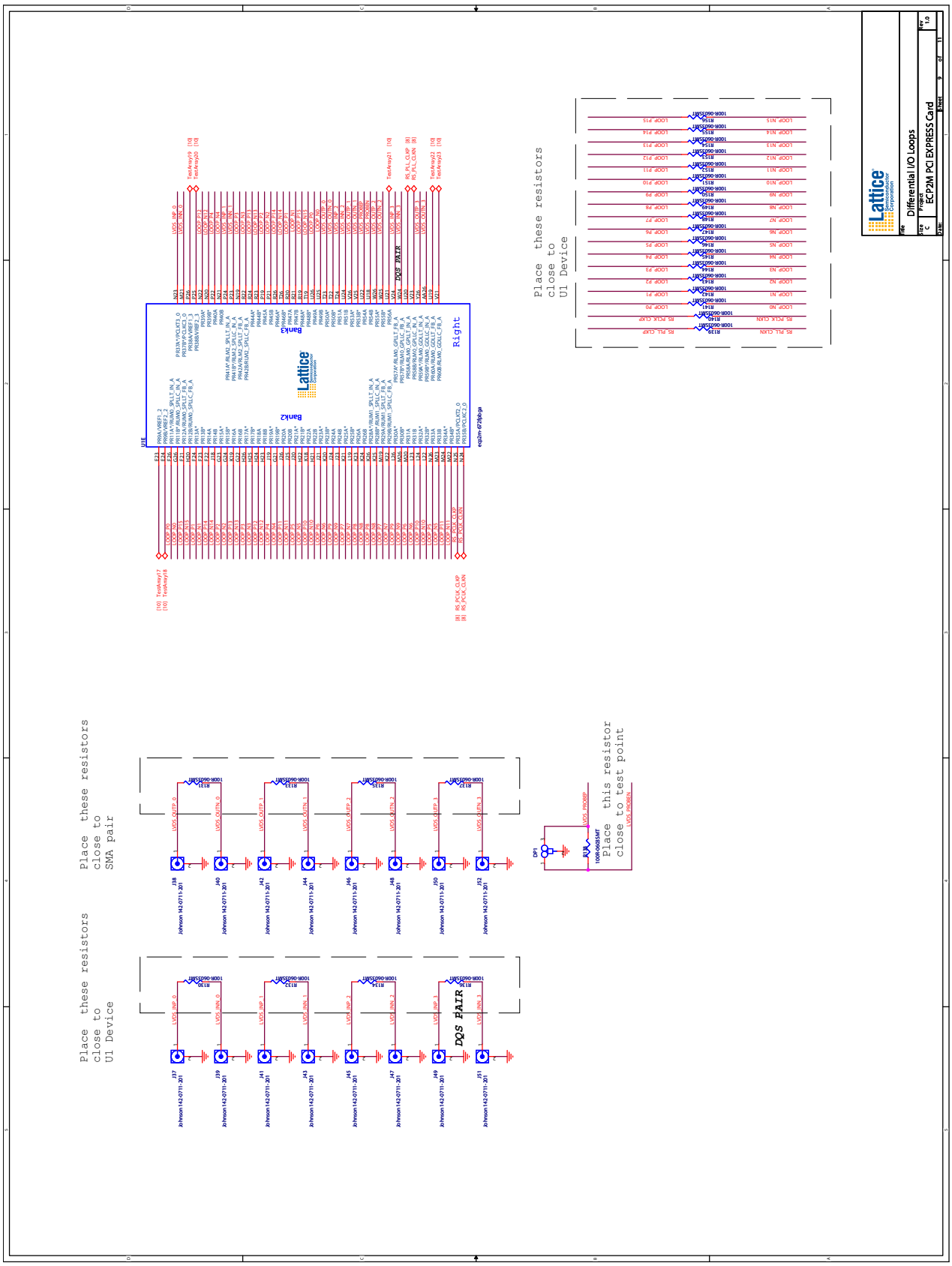


Figure 14. FPGA Test

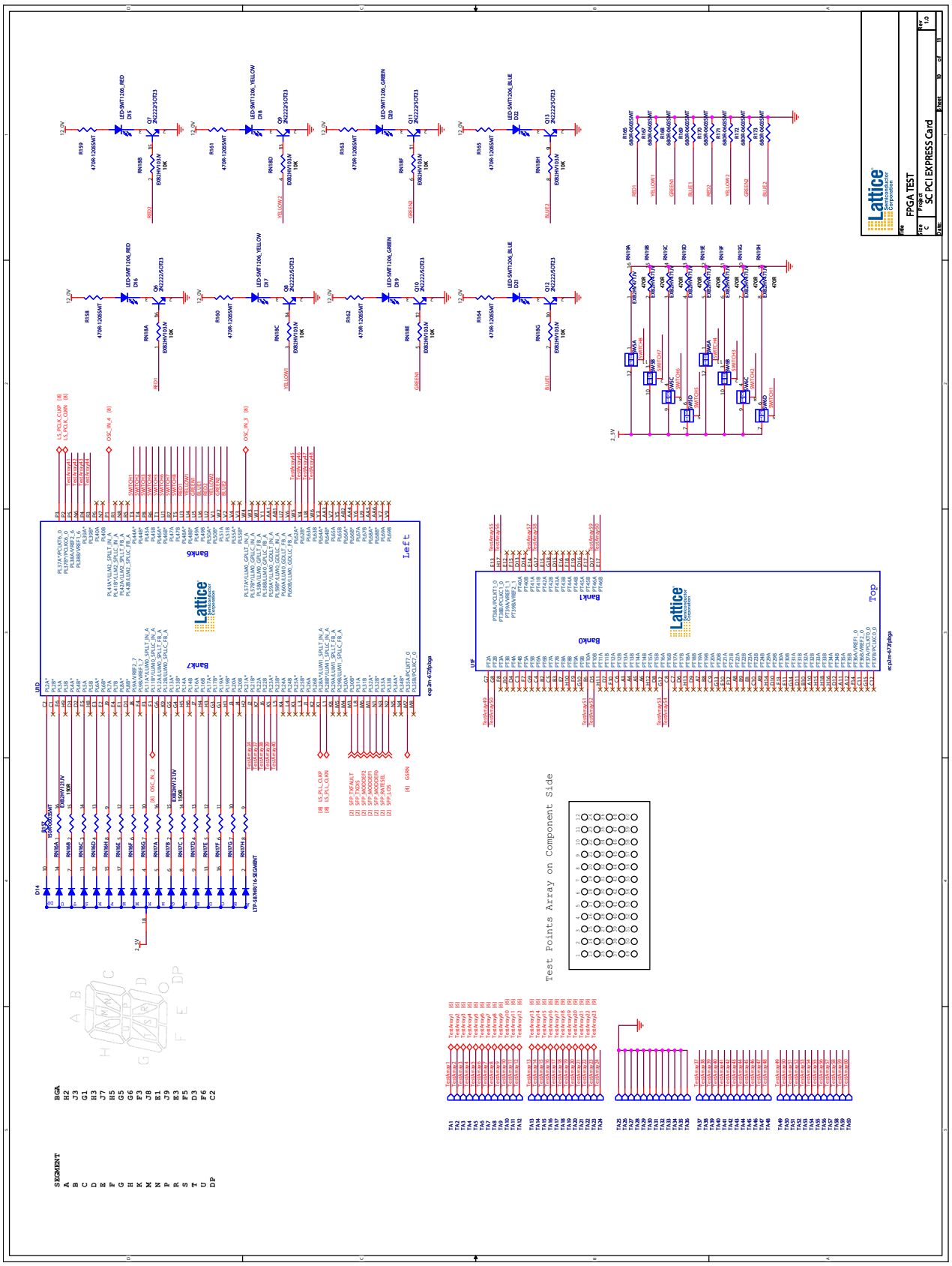


Figure 15. VSS/Decoupling