

Introduction

The System Packet Interface, Level 4, Phase 2 (SPI4.2) is a system level interface, published in 2001 by the Optical Internetworking Forum (OIF), for packet and cell transfer between a physical layer (PHY) device and a link layer device, for aggregate bandwidths of OC-192 ATM, Packet over SONET/SDH (POS), and 10Gbps Ethernet applications. The interface specifies a source-synchronous interface with differential data rates of at least 622 Mbits/sec (Mbps).

Designed for packet transfer between a MAC device and a network processor or switch fabric, the SPI4.2 interface supports the aggregate bandwidths required of ATM and packet-over-SONET/SDH (POS) applications. Moreover, SPI4.2 provides a common interface for 10Gbps wide area network (WAN), local area network (LAN), metro area network (MAN) and storage area network (SAN) technologies, and it is ideal for systems that aggregate low data rate channels into a single 10Gbps uplink for long haul or backbone transmission.

Typically, SPI4.2 has a 16-bit LVDS interface that operates at rates from 622Mbps to 900Mbps. These high data rates coupled with wide data paths make the task of managing skews between data and clocks extremely challenging. Traditionally, designers have used static constraints designed in the PCB to handle these skews. Unfortunately, this solution, though adequate under lower data rates, fails to solve the skew problems in today's leading edge designs. For this reason, SPI4.2 institutes a feature called dynamic alignment. Dynamic alignment utilizes a training sequence from the transmitter to the receiver to correct the clock/data skew within a 1-bit period. LatticeSCM FPGAs support SPI4.2 data rates up to 1Gbps with dynamic phase alignment and up to 700Mbps in static alignment mode.

This document discusses the SPI4.2 interoperability tests performed between a LatticeSCM device and a PMC-Sierra PM-3388 device. Specifically, this technical note discusses the following topics:

- Overview of LatticeSCM SPI4 MACO™ Solution
- Overview of PMC-Sierra PM-3388 Ten Port Gigabit Ethernet Controller (specifically related to the SPI4 interface)
- SPI4.2 Interoperability testing between the LatticeSCM and PMC-Sierra PM-3388 devices.

LatticeSCM SPI4 MACO Solution

Features

The LatticeSCM family, equipped with ASIC-like system level building blocks (referred to as Masked Array for Cost Optimization, or MACO blocks), is designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide, and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUXs that are required in today's high-end system designs.

SPI4.2 Features

LatticeSCM FPGAs contains one or two SPI4.2 cores implemented in Masked Array for Cost Optimization (MACO). The SPI4.2 implementation is fully compliant with OIF-SPI4-02.0 specification, offering up to 256 logical ports, with transmit/receive data paths that are 16-bits wide with in-band port address, SOP, EOP indication, and error control.

SPI4.2 features:

- Up to two full-featured OIF-SPI4-02.0 compliant interfaces
- Dynamic timing receive interface w/bandwidth up to 500MHz DDR (1Gbps)
- Static timing receive interface w/speeds up to 350MHz DDR (700Mbps)
- Transmit interface w/speeds up to 500MHz DDR (1000Mbps)
- 256 logical ports with embedded calendar-based sequence port polling mechanism and bandwidth allocation
- Simple FIFO interface to the FPGA logic enables ease of design and built-in clock domain transfers
- Loopback modes provide system- and chip-level debug
- Full-rate SPI4.2 interface running at 350MHz DDR (700Mbps) consumes 0.85W of power or less

Interoperability simulations completed with Lattice ORSPI4 (a full-featured SPI4.2 compliant device).

PMC PM-3388 Ten-Port Gigabit Ethernet Controller

Features

The PMC-Sierra PM-3388 is an ASIC device that implements a ten-port full duplex 1 Gigabit Ethernet MAC data transport device. The PMC-Sierra PM-3388 provides line interface connectivity provided by an on-chip SERDES function and data transport to the upstream device via the industry standard POS-PHY Level 4 interface.

The features (general and SPI4.2 related) of the PMC-Sierra PM-3388 include:

- Direct connect to optics via ten internal Serializer/Deserializer (SERDES) interfaces. Each SERDES is compatible with the IEEE 802.3-2000 PMA physical layer specification.
- On-chip data recovery and clock synthesis.
- Ten standard IEEE 802.3 Gigabit Ethernet MACs for frame verification.
- Frame filtering on 8 unicast or 64 multicast entries (per Gigabit Ethernet port).
- Internal 64K byte egress and 224K (229,376) byte ingress FIFO buffers to handle system latencies. These buffers can be partitioned during device initialization between the 10 ports.
- Line-side and system-side loopback capability for system level diagnostics.
- SATURN POS-PHY Level 4 16-bit LVDS System Interface (clocked up to 700MHz).
- A standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- A generic 16-bit microprocessor bus interface for configuration, control, and status monitoring. A full 32-bit microprocessor data bus is provided: this is to support the optional reading of the per-channel Ethernet statistics registers as a 32-bit data word.

Test Equipment

Below is the equipment used in the interoperability tests:

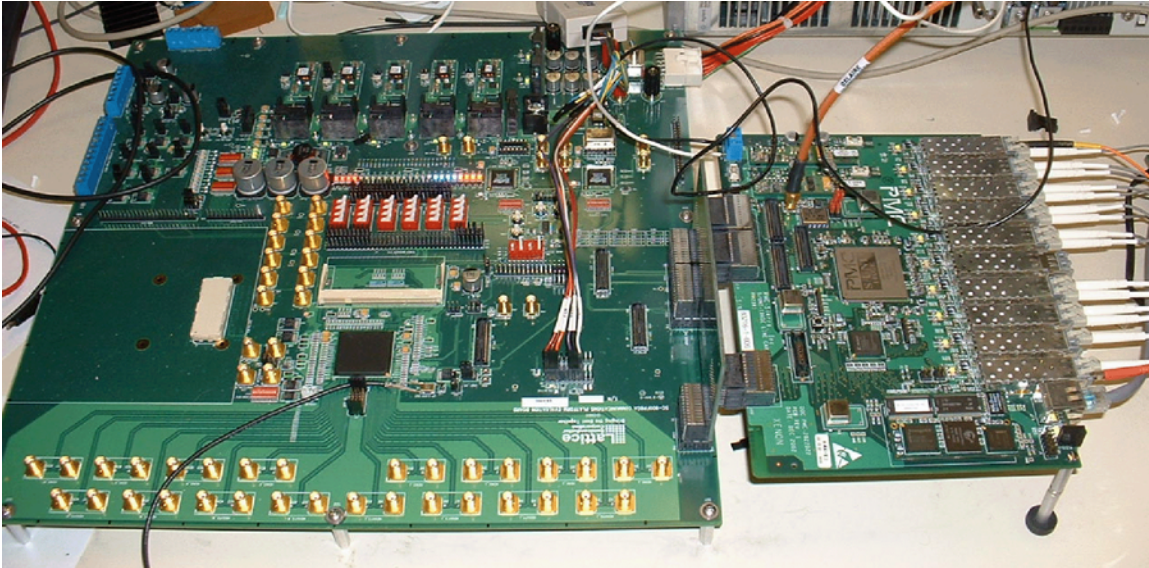
PMC-Sierra PM2381 Development Board

The PMC-Sierra PM2381 evaluation board includes:

- A PMC-Sierra PM-3388 device
 - On-board 175MHz and 125MHz clock source (plus support for external clocks)
 - A microcontroller for the board and PMC-Sierra PM-3388 device
 - 10 x 1 Gbps transponder sockets
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Figure 1 shows the test setup between the LatticeSCM Communications Board and the PMC-Sierra PM2381 board.

Figure 1. Test Setup of the PM2381 and LatticeSCM Communications Board

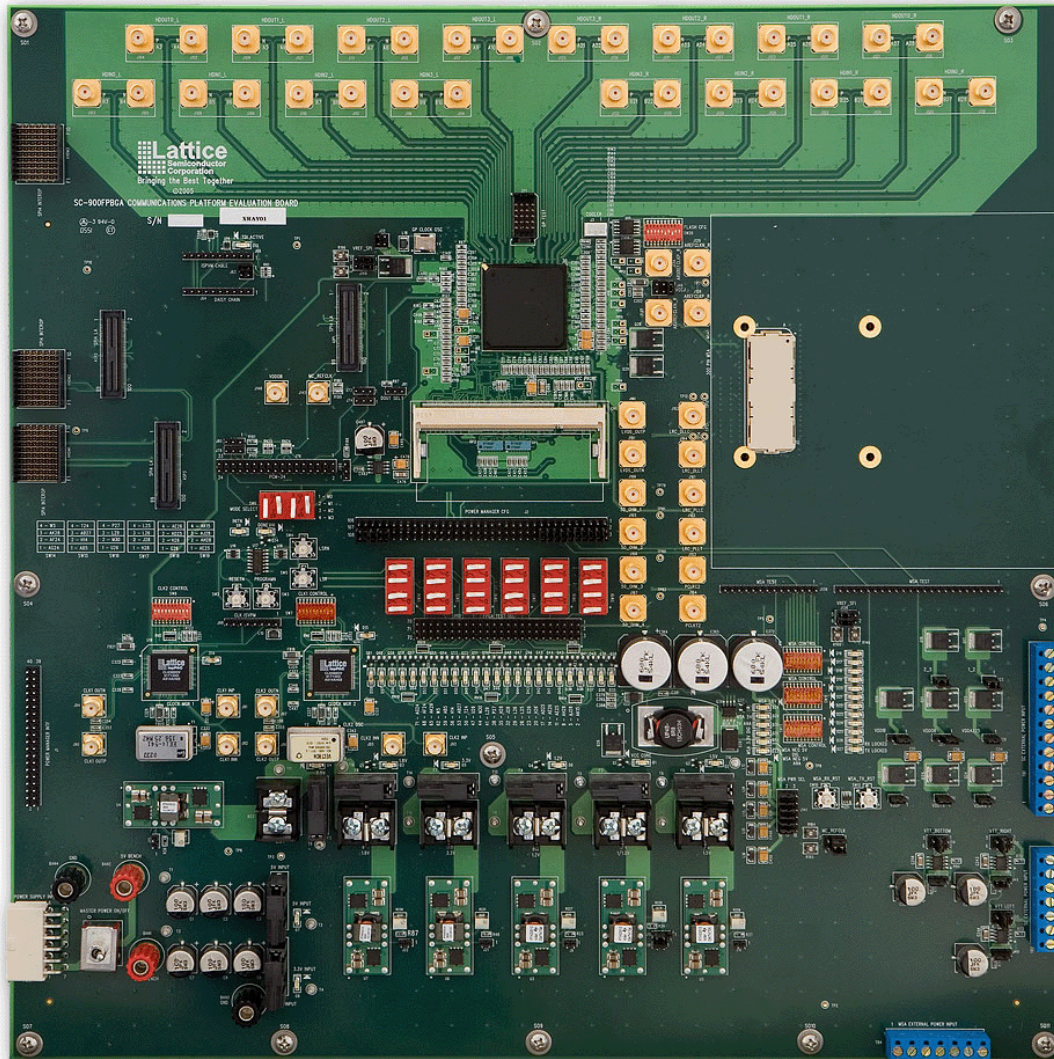


LatticeSCM Evaluation Board

The LatticeSCM Communications Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSCM FPGA or aid in development of custom designs. Each LatticeSCM communications board contains:

- An LFSC3GA25E-6F900C FPGA device
- A 300-pin MSA transponder interconnection to evaluation Single Data Rate (SDR) performance for SFI-4.1/XSBI applications
- A Molex VHDM interconnection to system packet interface level 4-phase 2 (SPI4.2)
- A 200-pin SODIMM socket supporting 64-bit 200-pin DDR-2 SDRAM
- SMA test points for high-speed SERDES and clock I/O
- On-board power connections and power sources
- An on-board interchangeable clock oscillator
- On-board reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- On-board Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 2 shows the LatticeSCM Communications Board.

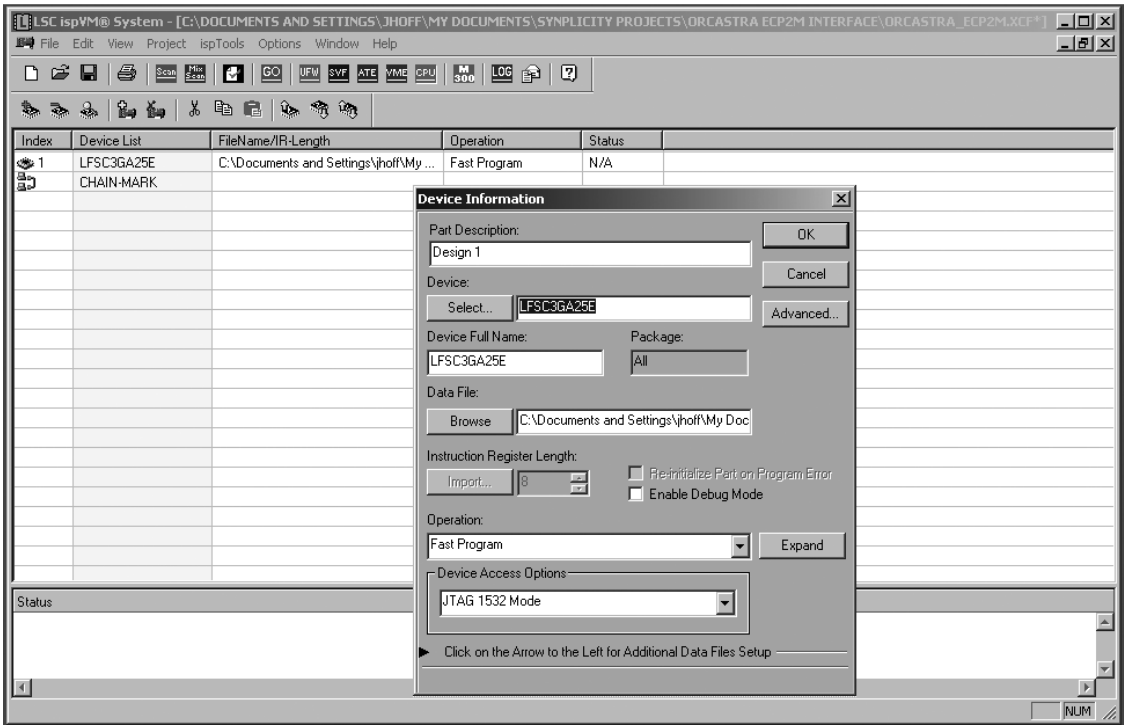
Figure 2. LatticeSCM Communications Board

ispVM® System

The ispVM System is included with the ispLEVER® design tool and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST and ispSVF programming as well as gang-programming with DLxConnect.

Figure 3 shows a screen shot of the ispVM System software.

Figure 3. ispVM System

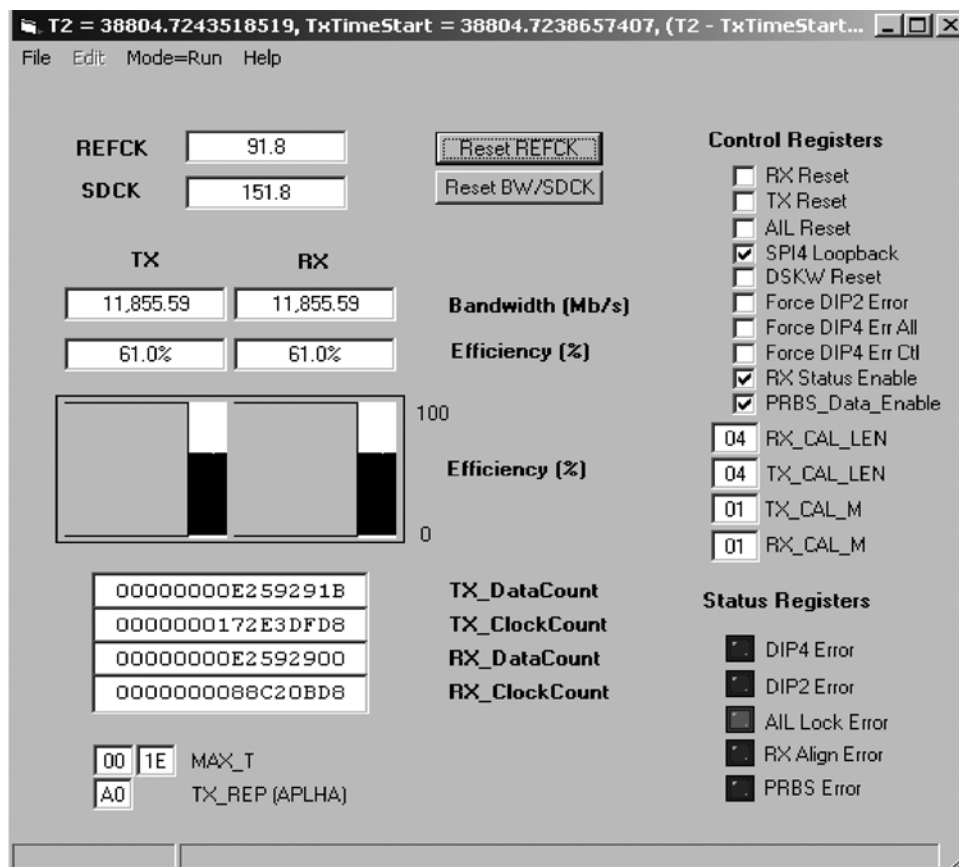


ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of a FPGA or FPSC by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to the board. Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the FPSC.

Figure 4 is a screen shot of ORCAstra system

Figure 4. ORCAstra System



Interoperability Testing

This section provides details on the interoperability tests between a LatticeSCM SPI4.2 MACO and a PMC-Sierra PM-3388 SPI4.2 interface. The purpose of these tests is to confirm the correct processing of SPI4.2 protocol between the two devices. Particularly, the tests verify:

- The ability to handle fixed length packets.
- The ability to handle packets ranging from 64 to 1024 bytes with Gaussian distribution.

Test Description

The set-up includes a LatticeSCM Communications board connected to a PMC-Sierra PM-3388 (PM2381) evaluation board through a Mezzanine board specially designed for the interoperability tests. The Mezzanine board maps the SPI4.2 signals from the connector on the LatticeSCM Communications board to the SPI4.2 signals on the connector on the PM2381 board. The data is sourced from a Spirent AX-4000 machine using a 1Gbps Ethernet card and is looped back to it to check for errors and statistics. The loopback is performed inside the LatticeSCM FPGA which means that the data traverses the complete path from the Spirent 1Gbps optical module to the SPI4 MACO and back to the Spirent 1Gbps Module. In all of the tests, the data flow is monitored with AX-4000 proprietary software.

Figure 5 shows the Mezzanine board interfacing the Lattice SC Communication board to the PMC-Sierra PM2381 Evaluation board.

Figure 6 shows a block diagram of the tests performed.

Figure 5. Mezzanine Board

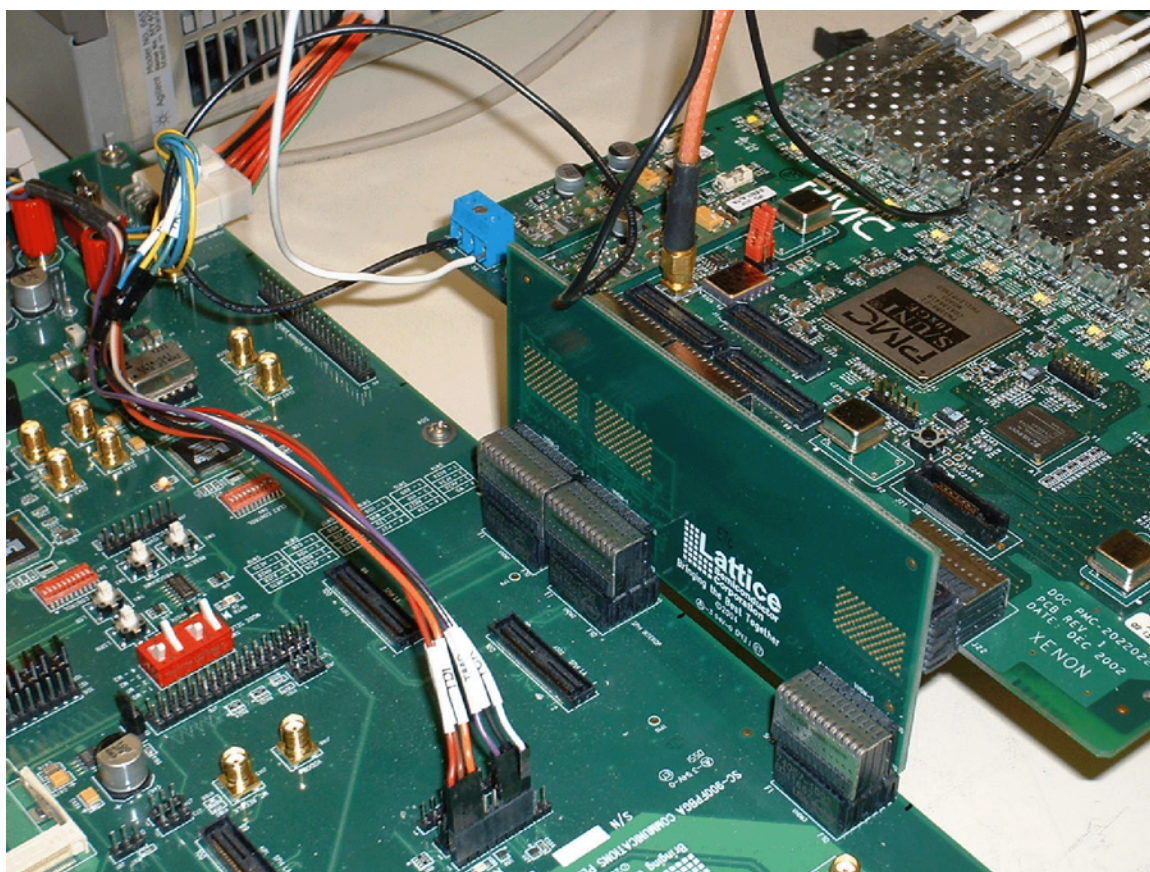
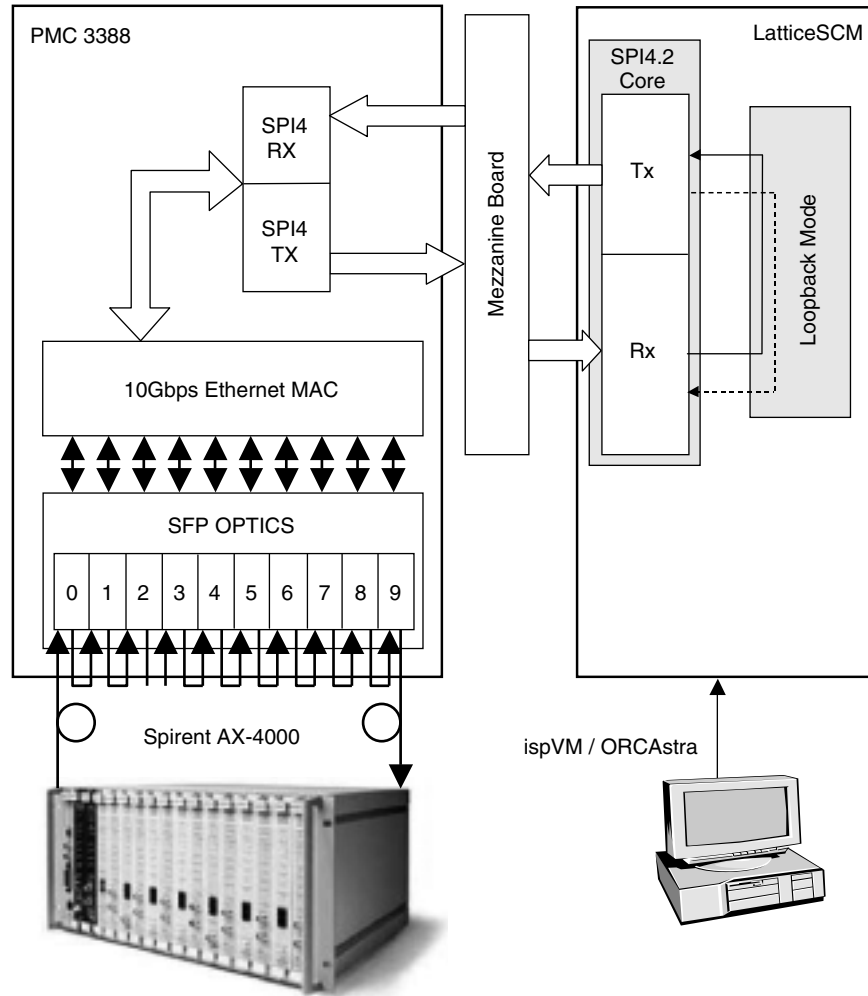


Figure 6. Test Setup



Test Configuration

The following test cases were used to verify the interoperability between the devices:

Data Path Synchronization

Data Path synchronization was successfully achieved by the transmitting and receiving training patterns between LatticeSCM SPI4 interface and the PMC-Sierra PM-3388 SPI4.2 interface.

Status Path Synchronization

Status Path Synchronization was successfully achieved between the two devices. Each device uses 10 ports. Therefore, the Calendar Length was sent to 10 and the value of Calendar_M was set to 1.

System Tests

These tests validate the SPI4.2 interoperability between the LatticeSCM device and the PMC-Sierra PM-3388 device.

Fixed Packet Data Test: 64 bytes of fixed packet data in the 1Gb Ethernet form was generated in the Spirent AX-4000 and transmitted over the Multimode Fiber link to the PMC-Sierra PM-3388 evaluation board. The data was successfully looped back from the LatticeSCM SPI4 interface back to the Spirent AX-4000.

Random Packet Data Test: 64 bytes to 1024 bytes of random packet data with Gaussian distribution in the 1Gb Ethernet form was generated in the Spirent AX-4000 and transmitted over the Multimode Fiber link to the PMC-

Sierra PM-3388 evaluation board. The data was successfully looped back from the LatticeSCM SPI4 interface back to the Spirent AX-4000.

SPI4.2 Parameters

Table 1 shows the SPI4.2 parameters used in the interoperability testing.

Table 1. SPI4.2 Parameters for Devices

SPI4.2 Parameter	LatticeSCM Configured Value	PMC PM-3388	Number of Ports
10	10	Calendar M	1
1	Alpha	0x0A	0x0A
Data_Max_T	40,000 HEX	40,000 HEX	Max_Burst1
N/A	0F	Max_Burst2	N/A
08	FPGA_Data_Width	128	128

Summary

In conclusion, LatticeSCM FPGA family offers users built-in SPI4.2 support and is compatible with the SPI4.2 interface (PL4 interface) on the PMC-Sierra PM-3388 device.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
August 2006	01.0	Initial release.