

Introduction

The System Packet Interface, Level 4, Phase 2 (SPI4.2) is a system level interface, published in 2001 by the Optical Internetworking forum (OIF), for packet and cell transfer between a physical layer (PHY) device and a link layer device, for aggregate bandwidths of OC-192 ATM, Packet over SONET/SDH (POS), and 10 Gbits/sec (Gbps) Ethernet applications. The interface specifies a source-synchronous interface with differential data rates of at least 622 Mbits/sec (Mbps).

Designed for packet transfer between a MAC device and a network processor or switch fabric, the SPI4.2 interface supports the aggregate bandwidths required of ATM and packet-over-Sonet/SDH (POS) applications. Moreover, SPI4.2 provides a common interface for 10Gbit/s wide area network (WAN), local area network (LAN), metro area network (MAN) and storage area network (SAN) technologies, and it is ideal for systems that aggregate low data rate channels into a single 10Gbit/s uplink for long haul or backbone transmission.

Typically, SPI4.2 has a 16-bit LVDS interface that operates at rates from 622Mbps to 900Mbps. These high data rates coupled with wide data paths make designers' tasks of managing skews between data and clocks extremely challenging. Traditionally, designers have used static constraints designed in the PCB to handle these skews. Unfortunately, this solution while working adequately under lower data rates, fails to solve the skew problems in today's leading edge designs. For this reason, SPI4.2 institutes a feature called dynamic alignment. Dynamic alignment utilizes a training sequence from the transmitter to the receiver to correct the clock/data skew within a +/-1-bit period. LatticeSC™ FPGAs support up to 1Gbps with dynamic phase alignment and up to 700Mbps in static alignment mode.

The objective of this technical note is to provide a report on the interoperability tests between a LatticeSC device and a SPI4.2 compliant ORCA® ORSPI4 FPGA. Specifically, this technical note discusses the following topics:

- Overview of LatticeSC devices and Lattice ORSPI4 (a SPI4.2 compliant device).
- SPI4.2 interoperability testing of the LatticeSC and ORSPI4 devices.

LatticeSC FPGA Overview

Features

The LatticeSC family equipped with ASIC-like system level building blocks was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding sub-layer), up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUXs that are required in today's high-end system designs.

SPI4.2 Features

LatticeSC FPGAs contain one or two SPI4.2 cores implemented in Lattice's Masked Array for Cost Optimization (MACO™ blocks). Each core is fully compliant with OIF-SPI4-02.0 specification, offering up to 256 logical ports, with transmit/receive data paths that are 16 bits wide with in-band port address, SOP, EOP indication, and error control.

The SPI4.2 features include:

- Up to two full-featured OIF-SPI4-02.0 compliant interfaces

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- Dynamic timing receive interface with bandwidth up to 500MHz DDR (1Gbps)
 - Static timing receive interface with speeds up to 350MHz DDR (700Mbps)
 - Transmit interface with speeds up to 500MHz DDR (1000Mbps)
 - 256 logical ports with embedded Calendar-based sequence port polling mechanism and bandwidth allocation
 - Simple FIFO interface to the FPGA logic enables ease of design and built-in clock domain transfers
 - Loopback modes provide system- and chip-level debug
 - Full-rate SPI4.2 interface running at 350MHz DDR (700Mbps) consumes 0.85W of power or less.
 - Interoperability simulations completed with ORSPI4 (a full-featured SPI4.2 compliant device)

ORSPI4 Description

Features

ORSPI4 is Lattice Semiconductor's industry leading FPGA device family with embedded SoC architectures. The device contains two SPI4.2 logic blocks, a high-speed memory controller, and four channels of 1.0-3.7Gbps SER-DES interfaces with 8b/10b encoding/decoding support.

The SPI4.2 features of the ORSPI4 include:

- OIF-SPI4-02.0 compliant interfaces
- Dynamic timing receive interface with bandwidth up to 450MHz DDR (900Mbps)
- Static timing receive interface with speeds up to 350MHz DDR (700Mbps)
- Transmit interface with speeds up to 450MHz DDR (900Mbps)
- 256 logical ports with embedded Calendar-based sequence port polling mechanism and bandwidth allocation; shadow Calendar support for smooth transition to new Calendar
- Simple FIFO interface to the FPGA logic enables ease of design and built-in clock domain transfers
- Configuration options as suggested in the OIF-SPI4-02.0 standard to configure parameters such as maximum burst size, calendar length, main and shadow calendars (1K deep each), length of training sequence etc.
- Loopback modes provide system- and chip-level debug
- Full-rate SPI4.2 interface running at 450MHz DDR (900Mbps/sec) consumes less than 2W of power or less. Much more efficient than FPGAs with soft-IP SPI4.2 solutions which can burn power in excess of 10W
- Interoperability simulations completed with ORSPI4 partners (NPU and framer vendors)

More importantly, the ORSPI4 family has demonstrated both full hardware and model interoperability with third party industry standard SPI4.2 devices including Intel IXF18101. Please refer to the following technical notes for details:

- TN1059: *Lattice ORSPI4 / Intel IXF1810 Physical Layer Device Interoperability*
- *ORSPI4 Partners Simulation Models Interoperability Report* (available from your local sales representative under an NDA)

Test Equipment

Below is the equipment used in the interoperability tests.

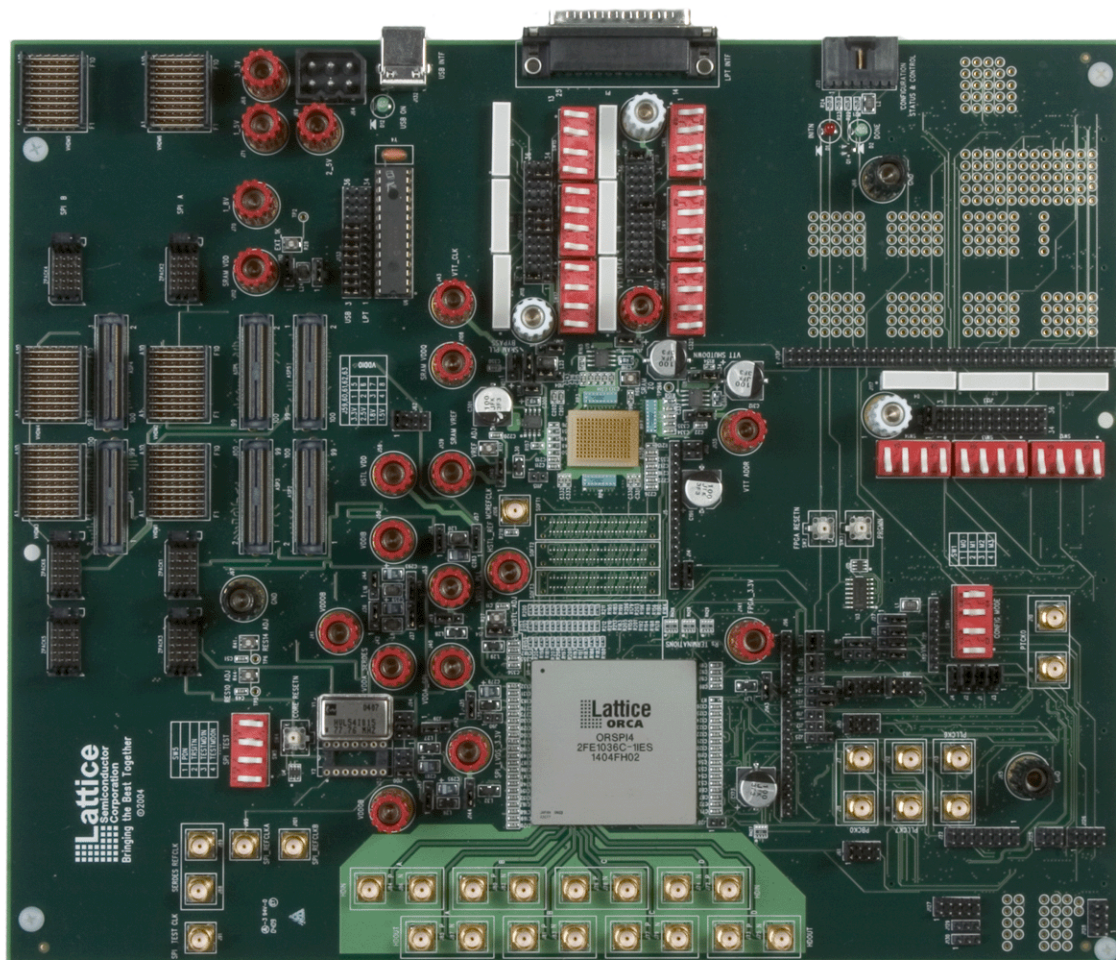
ORSPI4 ICM Board

The ORSPI4 evaluation board includes:

- An ORSPI4-2FE1036C device
- An on-board clock source (plus support for external clocks)
- Four 12-inch low-speed SMA cables (to facilitate various clocking setups)
- A USB cable for use with Lattice ORCAstra GUI configuration software
- An ICM power module board for complete power management
- Features Lattice ispPAC®-POWR1208 Power Manager
- A SPI4.2 loopback card
- An AC Adapter (US and EU compliant)
- ispDOWNLOAD® Cable pDS4102-DL2A

Figure 1 shows the ORSPI4 board.

Figure 1. ORSPI4 Evaluation Board



Lattice Semiconductor

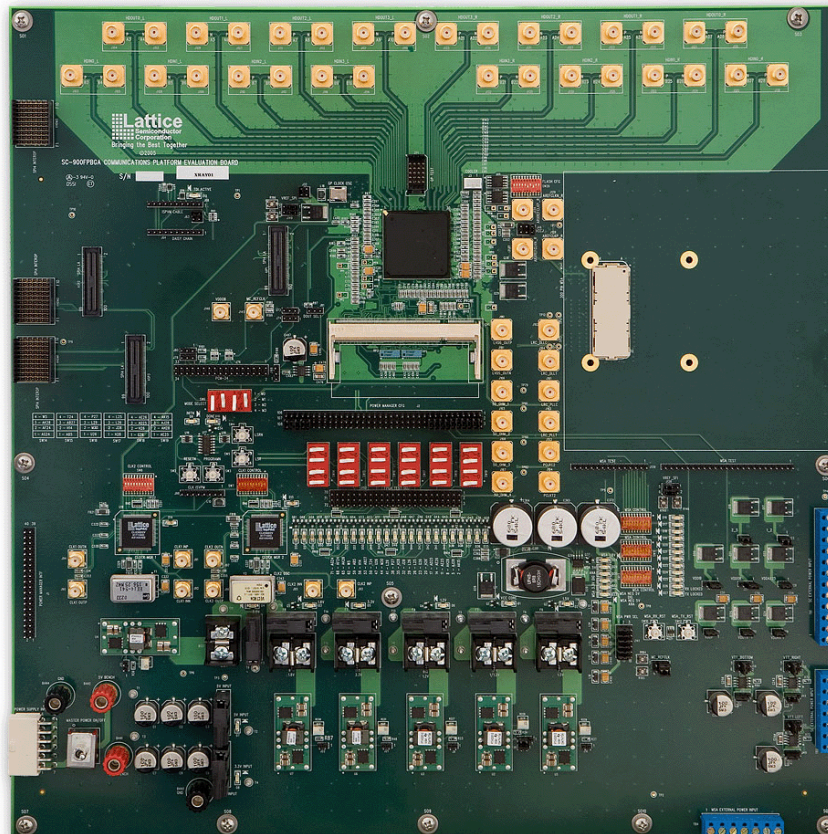
LatticeSC Evaluation Board

The LatticeSC Communications Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC FPGA or aid in development of custom designs. Each LatticeSC communications board contains:

- An LFSC3GA25E-6F900C FPGA device
- A 300-pin MSA transponder interconnection to evaluation Single Data Rate (SDR) performance for SFI-4.1/XSBI applications
- A Molex VHDM interconnection to system packet interface level 4-phase 2 (SPI4.2)
- A 200-pin SODIMM socket supporting 64-bit 200-pin DDR-2 SDRAM
- SMA test points for high-speed SERDES and Clock I/O
- On-board power connections and power sources
- An on-board interchangeable clock oscillator
- On-board reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- On-board Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 2 shows the LatticeSC Communications Board.

Figure 2. LatticeSC Communications Board



Agilent 16760A State and Timing Module

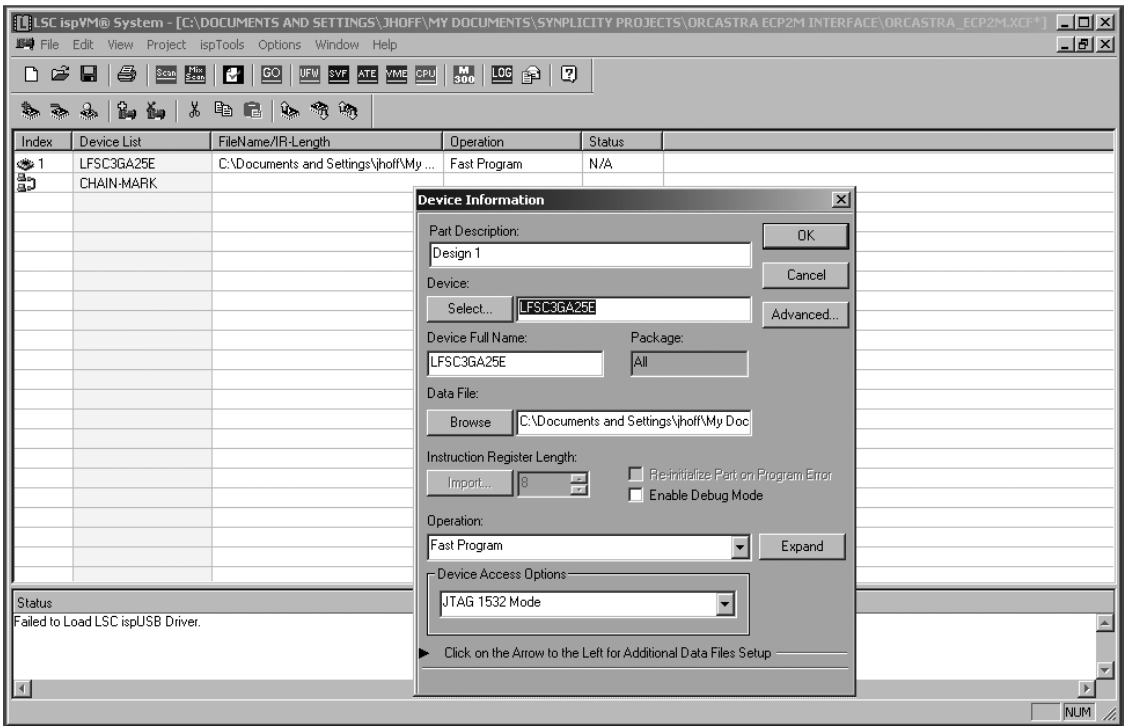
The Agilent 16760A state and timing module has differential inputs that can acquire signals at rates up to 1.5Gbps. For more information on 16760A module, please refer to the Agilent website: www.agilent.com.

ispVM® System

The ispVM System is included with ispLEVER®, and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and Bitstream files generated by Lattice Semiconductor, and other, design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

Figure 3 shows a screen shot of the ispVM System.

Figure 3. ispVM System

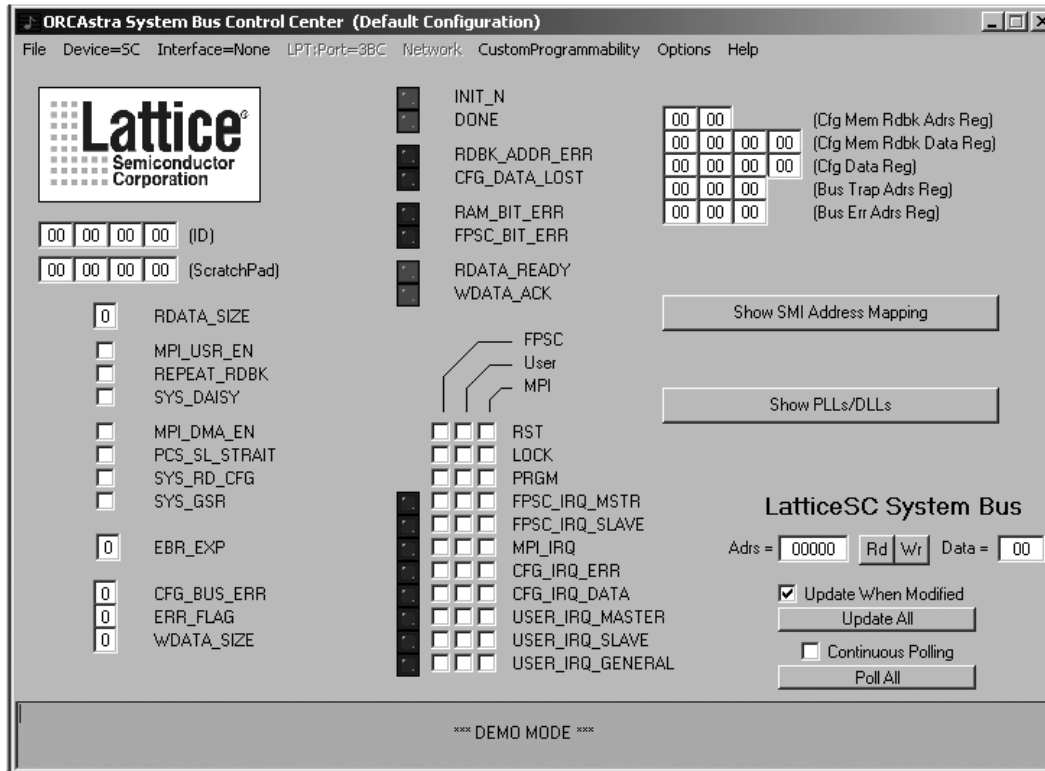


ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of a FPGA or FPSC by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to your board. Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the FPSC.

Figure 4 is a screen shot of the ORCAstra system

Figure 4. ORCAstra System



Interoperability Testing

This section provides details on the interoperability tests between a Lattice's proven SPI4.2 compliant ORSPI4 device and a LatticeSC FPGA. The purpose of these tests is to confirm the correct processing of SPI4.2 protocol between the two devices. Particularly, the tests verify:

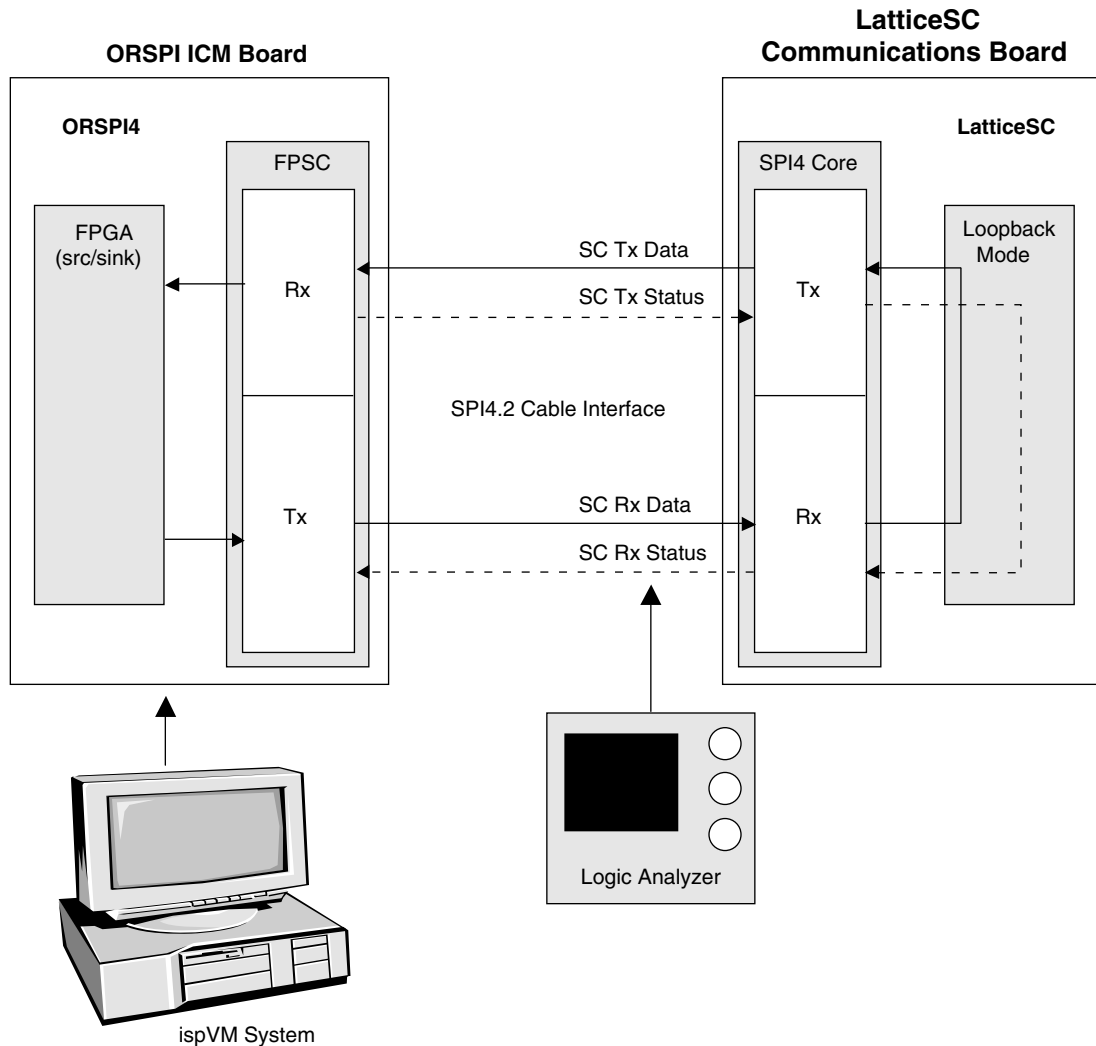
- The ability to handle fixed length packets.
- The ability to handle random length packets from 64 to 1024 bytes with single byte resolution.
- LatticeSC's ability to handle incrementing length packets with single byte resolution.

These tests are done in addition to lab characterization of the LatticeSC device at different process, voltage, and temperature corners.

Test Description

Figure 5 describes the block diagram. The set-up includes an ORSPI4 ICM board connected to a LatticeSC evaluation board through a short cable, roughly 12 inches. The ORSPI4 FPGA acts both as the source and sink of the SPI4 data. And, the LatticeSC device is loaded with a bit stream that includes the SPI4.2 MACO core and a user-side loopback module. In all of the tests, the data flow is monitored with an Agilent 16760A state and timing module.

Figure 5. Test Set-up



Test Configuration

The following test cases were used to verify the interoperability between the devices.

Training Pattern Generation Test

The goal of this test is to show that the device works with different MAX_T and ALPHA values.

Transmit line-side and user-side FIFO Threshold Test

This test case varies the threshold values of the FIFOs. Particularly, it forces the device to fail transmitting by writing wrong values into the threshold registers. The device resumes transmitting after the correct values are restored.

Transmit and Receive Status Path Test

DIP2 thresholds registers were verified. The In-Sync threshold determines the number of good DIP2 words before the device will declare In-Sync status. The out-of-sync threshold determines the number of bad DIP2 words before the device declares out-of-sync status. Please refer to LatticeSC SPI4 MACO core user guide for a discussion on the above mentioned registers.

Receive Input Alignment Test

The goal of this test is to validate both the static and dynamic alignment modes of the SPI4-MACO core

Receive User-side and Line-side FIFO Threshold Test

Resembling the test procedures done at the transmit side, this test case forces the device to fail transmitting by writing wrong values into the threshold registers. The device resumes transmitting after the correct values are restored.

DIP4 Threshold Test

As in the transmit and receive status path tests, the goal of this test is to ensure the DIP4 threshold registers are working properly.

Transmit and Receive Calendar Test

This test is to verify the functionality of the calendar length and Calendar-M.

RAM and Transparent Mode Test

The goal of this test is to confirm that RAM and transparent modes work accordingly.

Status Control Test

The functionality of the internal and external status control logic is confirmed with this test.

System Test

This test validates that LatticeSC's SPI4.2 functions under four-port and 32-port configurations.

Test Results and MACO Parameters

Table 1 shows the MACO parameter values used in the tests.

Table 1. MACO Parameters for Devices

MACO Parameter	LatticeSC Configured Value	ORSPI4 Configured Value
Number of Ports	1, 2, 4, 16, 32, 256	1, 2, 4, 16, 32, 256
Alpha	0x0A	0x0A
Data_Max_T	40,000 HEX	40,000 HEX
Max_Burst1	N/A	0F
Max_Burst2	N/A	08
Burst_Val	LatticeSC can handle any burst value.	4
FPGA_Data_Width	128	128

Table 2 summarizes the test results.

Table 2. Summary of the Interoperability Tests

Test	Status
Training Pattern Generation Test	Pass
Receive Calendar Test	Pass
Transmit line-side and user-side FIFO Threshold Test	Pass
Transmit and Receive Status Path Test	Pass
Receive Input Alignment Test	Pass
Receive User-side and Line-side FIFO Threshold Test	Pass
DIP4 Threshold Test	Pass
Transmit and Receive Calendar Test	Pass
RAM and Transparent Mode Test	Pass

Summary

In conclusion, the LatticeSC FPGA family offers users built-in SPI4.2 support and is fully inter-operable with ORSPI4, Lattice's SPI4.2 compliant device family. For details on ORSPI's hardware interoperability, please refer to Lattice technical note TN1059, *Lattice ORSPI4 / Intel IXP1810 Physical Layer Device Interoperability*.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
June 2006	01.0	Initial release.