

Introduction

The document provides a report on a XAUI interoperability test between a LatticeSC device and the Marvell 88X2040 device. Specifically, this technical note discusses the following topics:

- Overview of LatticeSC™ devices and Marvell Alaska 88X2040 devices
- XAUI interoperability testing of the LatticeSC and Marvell 88X2040 devices

XAUI Interoperability

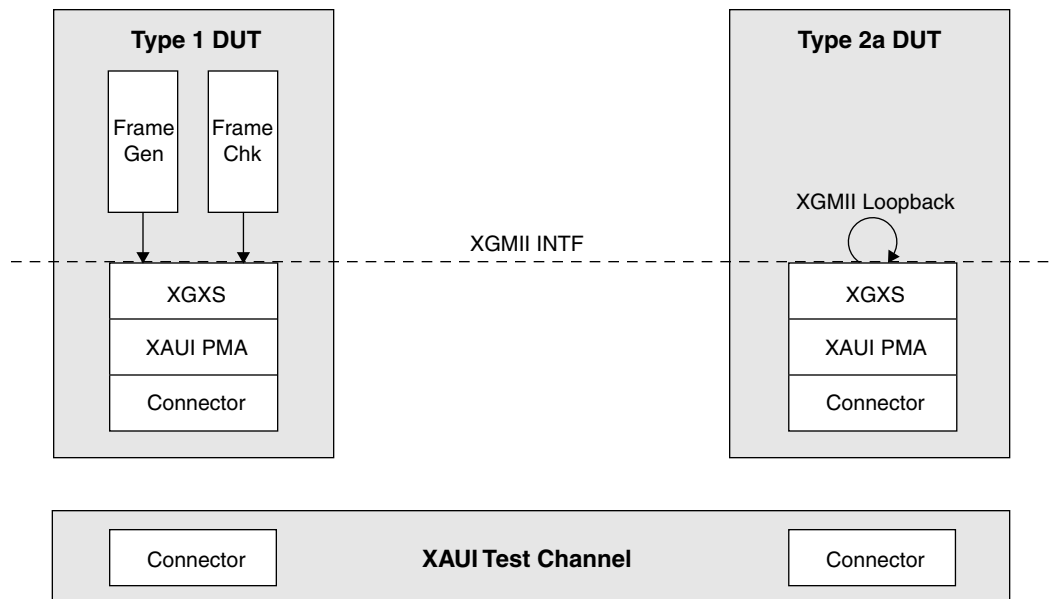
XAUI is a high-speed interconnect that offers reduced pin count and the ability to drive up to 20" of PCB trace on standard FR-4 material. In order to connect a 10-Gigabit Ethernet MAC to an off-chip PHY device, an XGMII interface is used. The XGMII is a low-speed parallel interface for short range (approximately 2") interconnects.

XAUI interoperability is based on the 10-Gigabit Ethernet standard (IEEE Standard 802.3ae-2002). Two XAUI link partners can be directly plugged into a XAUI backplane. Both boards are capable of generating and checking packets. The board that sources packets is capable of keeping a detailed count of the number of packets transmitted while the sink board is capable of keeping detailed statistics on the number of packets received and errors associated with the packets. The XAUI backplane is also called the XAUI test channel. A typical test setup is shown in Figure 1.

Each reference station must be a line card that is directly plugged into the XAUI test channel. Both DUTs are required to have their own clock domain. Synchronous clocking (distributing a single clock to the two DUTs) is not allowed. Local management indicators on the DUT (reference stations) that provide information on link level errors such as CRC errors are also needed.

A DUT is called a Type #1 device if it is capable of transmitting and checking packets. A DUT is called a Type #2a device if it receives packets and does a RX to TX loopback through XGMII and sends the packets back to the transmitting station, which is a Type #1 device. The Type #1 device then checks the received packets for errors. Figure 1 shows a setup where one DUT is of Type #1 and the other is of Type #2a.

CRPAT and CJPAT patterns are commonly used for XAUI testing. CRPAT provides broad spectral content and minimal peaking that can be used for the measurement of jitter. CJPAT exposes a receiver's CDR to large instantaneous phase jumps. The pattern alternates repeating low transition density patterns with repeating high transition density patterns.

Figure 1. Typical XAUI Interoperability Test Setup

The XAUI test is designed to verify the ability of two link partners to exchange packets with each other. The exchange of packets should produce a packet error ratio that is low enough to meet a desired bit error ratio. The bit error ratio, as specified in IEEE Standard 802.3ae-2002, is 10⁻¹². For this test, the selected test pattern is sent continuously for at least 5 minutes. This ensures that the bit error ratio is less than 10⁻¹² with 95% accuracy if no errors are observed. Optionally, a longer 30-minute test can be run to ensure that the bit error rate is less than 10⁻¹² with 99.999999% accuracy if no errors are observed.

LatticeSC/flexiPCS™ Overview

LatticeSC Features

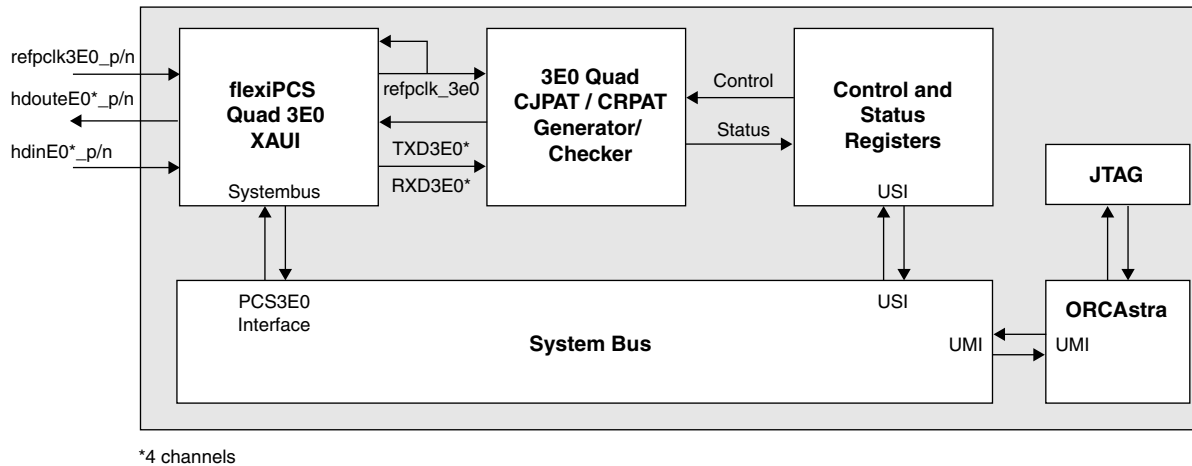
The LatticeSC family, equipped with ASIC-like system level building blocks, was designed as a platform technology to facilitate the implementation of the many connectivity challenges faced by designers. This family of devices includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide and phase shift PLLs, numerous DLLs and a dynamic glitch free clock MUX that are required in today's high-end system designs.

All LatticeSC devices feature up to 32 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

Each channel of flexiPCS logic contains dedicated transmit and receive SERDES

LatticeSC XAUI Solution

As shown in Figure 2, the LatticeSC XAUI interoperability solution combines both a flexiPCS block in XAUI mode and a CJPAT/CRPAT generator/checker in FPGA logic.

Figure 2. LatticeSC XAUI Interoperability Design Solution

LatticeSC flexiPCS in XAUI Mode

The XAUI mode of the flexiPCS (Physical Coding Sublayer) block supports full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard. XAUI Mode supports 10 Gigabit Ethernet as well as 10 Gigabit Fibre Channel applications.

Transmit Path Functionality (From LatticeSC Device to Line):

- Transmit State Machine which performs translation of XGMII idles to proper ||A||, ||K||, ||R|| characters according to the IEEE 802.3ae-2002 specification
- 8b10b encoding

Receive Path Functionality (From Line to LatticeSC Device):

- Word Alignment based on IEEE 802.3-2002 defined alignment characters
- 8b10b decoding
- Link State Machine functions incorporating operations defined in PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine compliant to the IEEE 802ae.3-2002 specification

LatticeSC XAUI CJPAT/CRPAT Generator/Checker Soft IP

The XAUI CJPAT/CRPAT generator/checker has the following characteristics:

- Four channels form an XGMII bus
- One XAUI Generator (CJPAT or CRPAT) transmits to all four TXD channels
- One XAUI Checker (CJPAT or CRPAT) checks all four RXD channels
- Control/Status interface to user registers
- One Error Counter (CJPAT or CRPAT) connected to user registers for monitoring

The System Bus controls the user registers via the User Slave Interface (USI). The System Bus is in turn controlled by the ORCAstra interface through JTAG.

Marvell Alaska 88X2040 Overview

Marvell Alaska 88X2040

The Marvell 88X2040 Quad transceiver is a fully integrated serialization/de-serialization device that incorporates four independent lanes, delivering high-speed bi-directional point-to-point baseband data transmission that supports cost-effective IEEE 802.3ae compliant 10 Gigabit Ethernet and 10 Gigabit Fibre Channel applications.

The 88X2040 Quad can be configured either as four separate high-speed lanes or as a single data path with four synchronized lanes. It supports a wide range of serial data rates from 1.0 Gbps to 3.1875 Gbps. The 88X2040 supports the 32-bit bi-directional 10 Gigabit Media Independent Interface (XGMII) with 8b/10b ENDEC option, and the extended Auxiliary Unit Interface (XAUI). The 88X2040 performs the parallel-to-serial, serial-to-parallel conversion with integrated Time Base Generator (TBG) and Clock/Data Recovery Circuit (CDRC). On-chip synthesis performed by the high performance, high frequency, and low jitter phase-locked loop on the 88X2040 transceiver allows the use of cost-effective, low frequency clock references.

On-chip clock synthesis is performed to meet compliance with the bit error rate (BER) requirement of associated ANSI, Bellcore, and ITU-T standards.

The 88X2040 supports pre-emphasis on the serial driver to compensate for losses in copper environment.

Marvell Alaska 88X2040 Features

- IEEE 802.3ae/10GFC compliant Quad 3.125 Gbps/lane transceiver
- Supports IEEE 802.3ae/10GFC XGMII parallel interface
- Supports IEEE 802.3ae/10GFC XAUI serial interface
- Allows maximum 20 Gbps full-duplex data throughput
- On-chip 8b/10b Encoding/Decoding (ENDEC)
- On-chip Time Base Generator
- Elastic buffering
- Supports pre-emphasis on the serial driver
- On-chip 50-ohm serial receiver termination
- IEEE 1149.1 JTAG test interface
- 1.5V, 3.3V, and 1.8V power supplies
- 1.5V or 1.8V HSTL I/O
- Selectable 62.5 MHz, 125 MHz, or 156.25/159.375 MHz reference clock input
- Exceeds IEEE 802.3ae jitter requirement
- Advance 0.15 μ m digital CMOS process

Test Equipment

The equipment used in the interoperability test is described below.

Marvell 88X2040 SMA to XGMII Evaluation Board

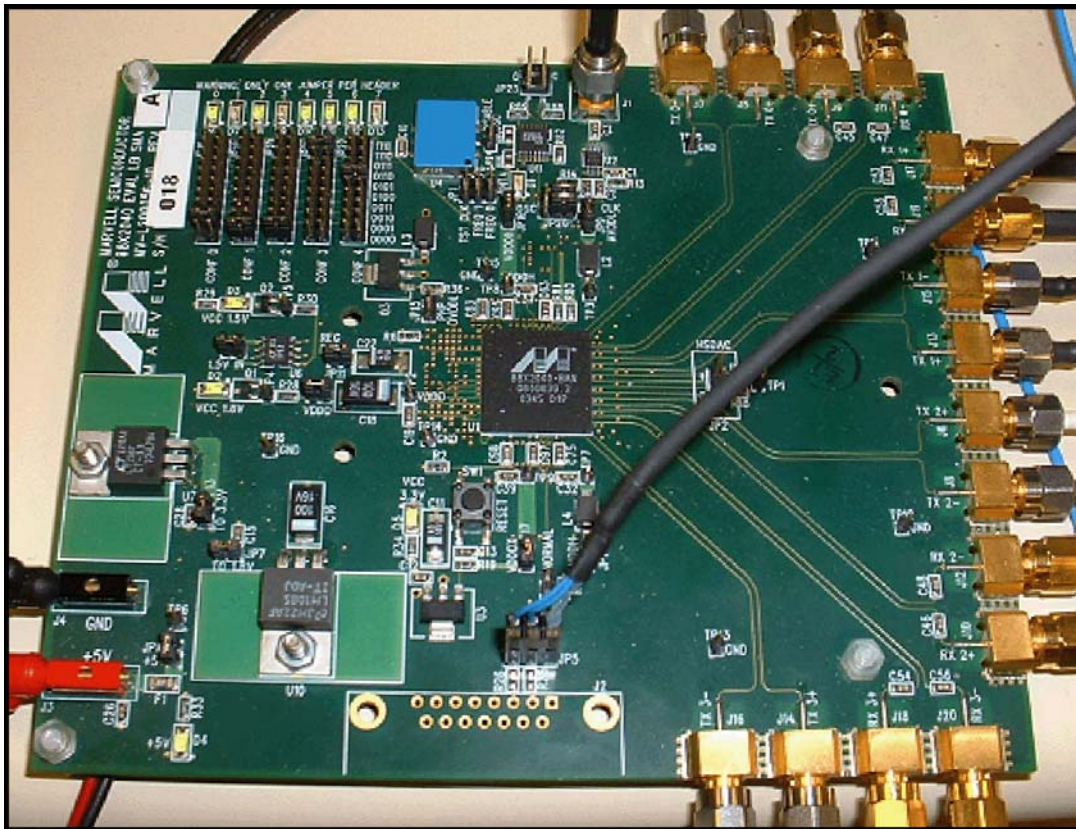
The 88X2040 is a quad 3.125 Gbps transceiver which serializes XGMII signals and de-serializes XAUI signals. On the 88X2040 board, the XGMII signals are looped back from the receive side to the transmit side and the XAUI signals are connected to SMA connectors. This evaluation board is designed to use the internal packet generator and receive packet counters to evaluate the transceiver.

The board includes:

- The capability to use an on-board 156.25 MHz oscillator clock source or an external source from an SMA input
- MDIO/MDC monitoring/control to both devices
- Eight Transmit SMAs and eight Receive SMAs for access to the 88X2040 SERDES

Figure 3 shows the 88X2040 evaluation board.

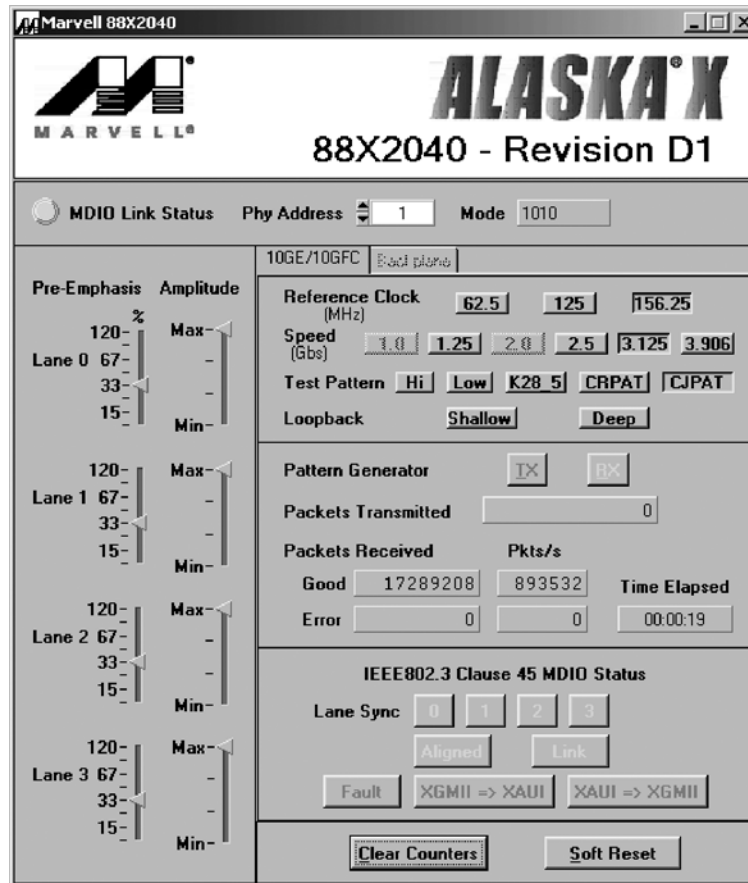
Figure 3. Marvell 88X2040 Evaluation Board



Marvell Alaska X 88X2040 Software

The Alaska X 88X2040 software GUI controls the 88X2040 devices and monitors status bits through MDIO/MDC. Figure 4 shows the GUI.

Figure 4. ALASKA Virtual Cable Tester Software GUI



The GUI is sub-divided into several sections.

Rate and Pattern Section:

- The reference clock is set to 156.25 MHz
- Speed is set to 3.125 Gbps (XAUI rate per channel)
- Either CJPAT or CRPAT can be selected for Test Pattern

Pattern Generator Section:

- Selecting the TX button transmits the above selected pattern to the SERDES outputs. The Packet Transmitted counter keeps track of the number of packets transmitted.
- De-selecting the TX button puts the 88X2040 board in external loopback mode. In this mode, the pattern at the XGMII RX side is looped back to the XGMII TX side and sent to the SERDES SMA outputs.
- Selecting the RX enables the counters to count the number and rate of Good and Error received packets (of the selected pattern).

Pre-Emphasis and Amplitude Control Section

This section provides amplitude and pre-emphasis control for all four XAUI SERDES channels.

Link Status Section

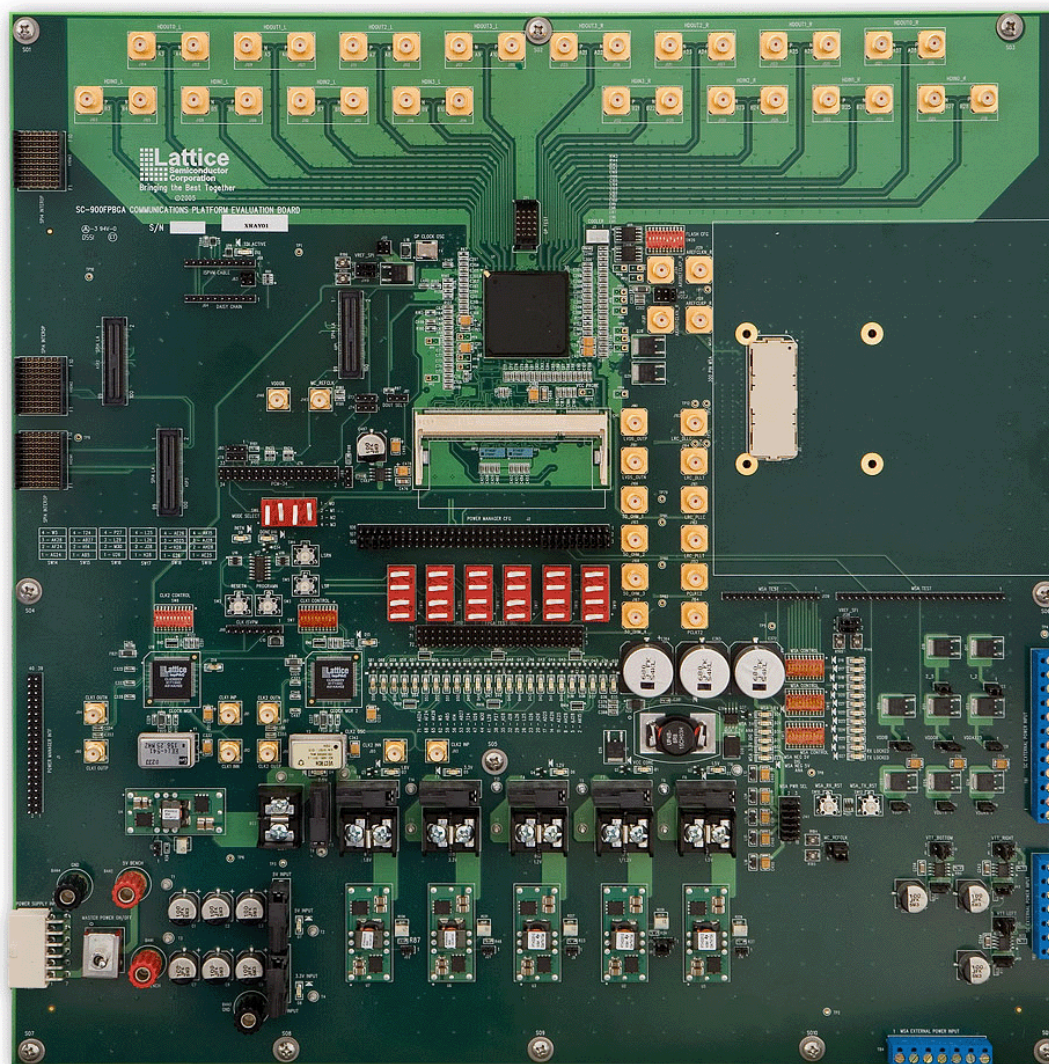
This section provides information on the status of the XAUI link. For proper linking, the individual Lane Sync indicators for all four channels, as well as the Aligned and Link indicators should all be green.

LatticeSC Evaluation Board

The LatticeSC Communications Board provides a stable yet flexible platform to quickly evaluate the performance of the LatticeSC FPGA or to aid in the development of custom designs. Each LatticeSC communications board contains:

- An LFSC3GA25E-6F900C FPGA device
- SMA test points for high-speed SERDES and clock I/O
- On-board power connections and power sources
- On-board interchangeable clock oscillator
- On-board reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- On-board Flash configuration memory
- Various LEDs, switches, connectors, headers and SMA connections for external clocking, and on-board power control

The LatticeSC Communications Board is shown in Figure 5.

Figure 5. LatticeSC Communications Board

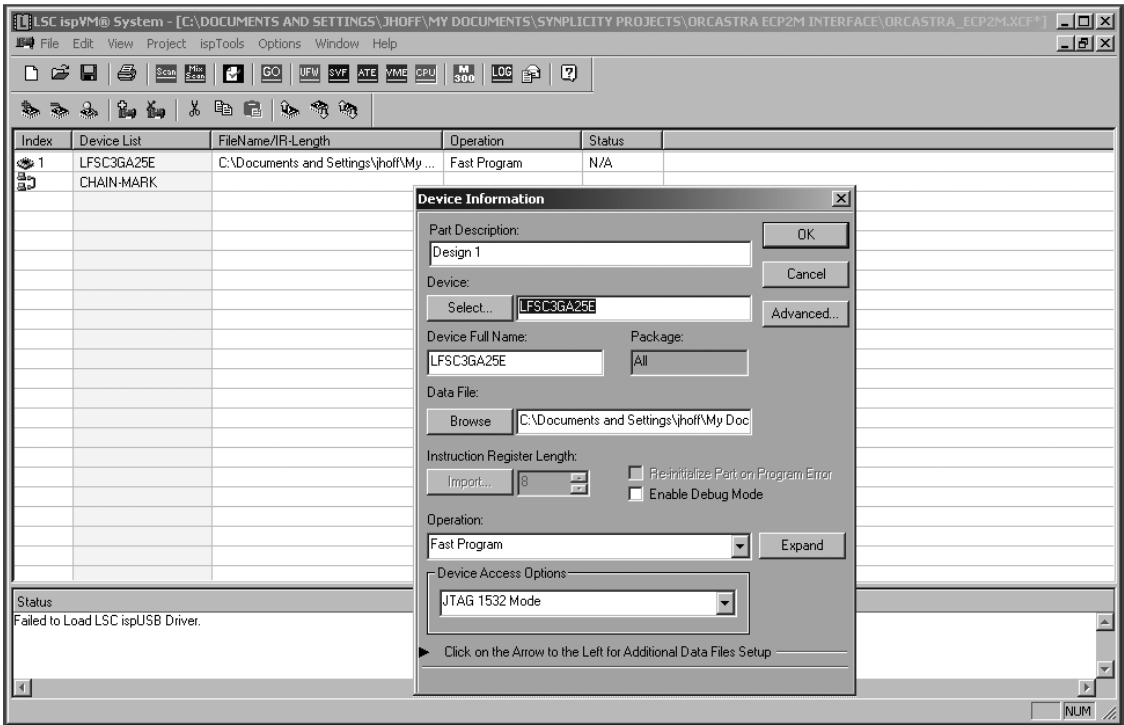
ispVM® System

ispVM System is included with Lattice's ispLEVER software, and is also available as a stand-alone device-programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice software and tools from other vendors. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

ispVM System is used in this interoperability test to download the LatticeSC bitstream to configure the FPGA in Gigabit Ethernet mode.

Figure 6 shows a screen shot of ispVM System.

Figure 6. ispVM System



ORCAstra System

Lattice ORCAstra software is a PC-based graphical user interface for configuring the operational mode of an FPGA or FPSC by programming control bits in the on-chip registers. This helps users to quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of ORCAstra software does not interfere with the programming of the FPGA portion of the FPSC.

Figure 7 is a screen shot of the ORCAstra system.

Figure 8 illustrates the flexiPCS view of the ORCAstra GUI. This view provides important information, such as CDR lock to data, loss of PLL lock, the status of link state machines, and channel alignment status in XAUI mode. The view also allows the user to directly control SERDES TX and RX terminations, and SERDES TX pre-emphasis and amplitude levels, among others.

Figure 7. ORCAstra System

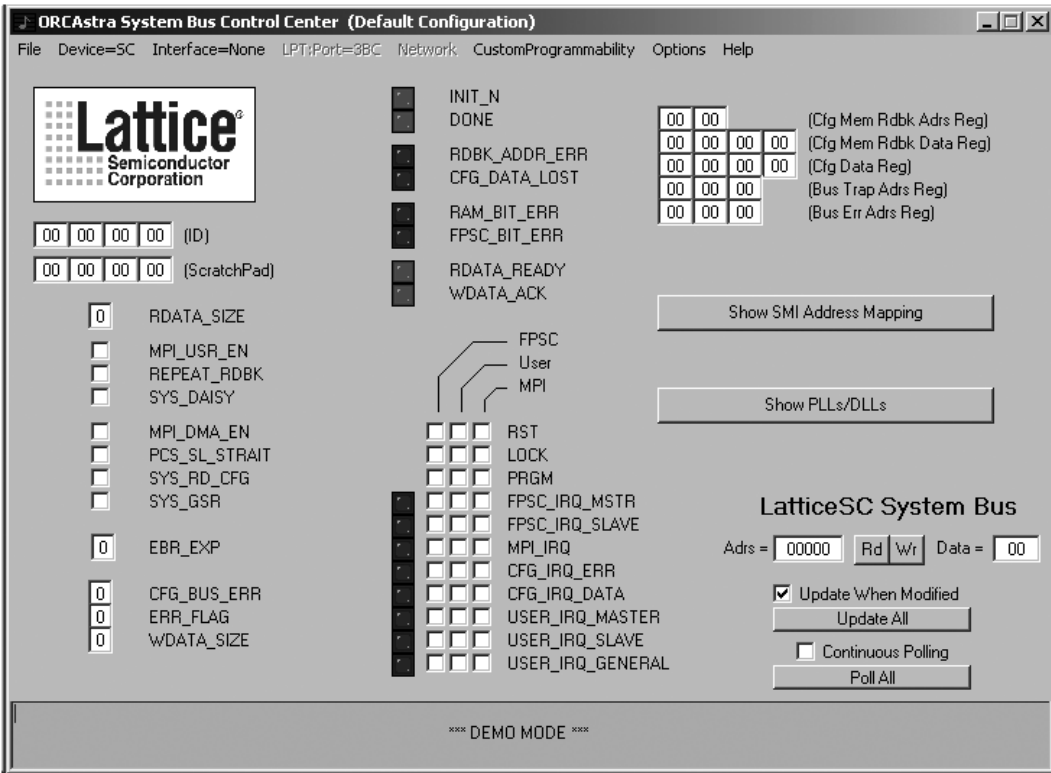
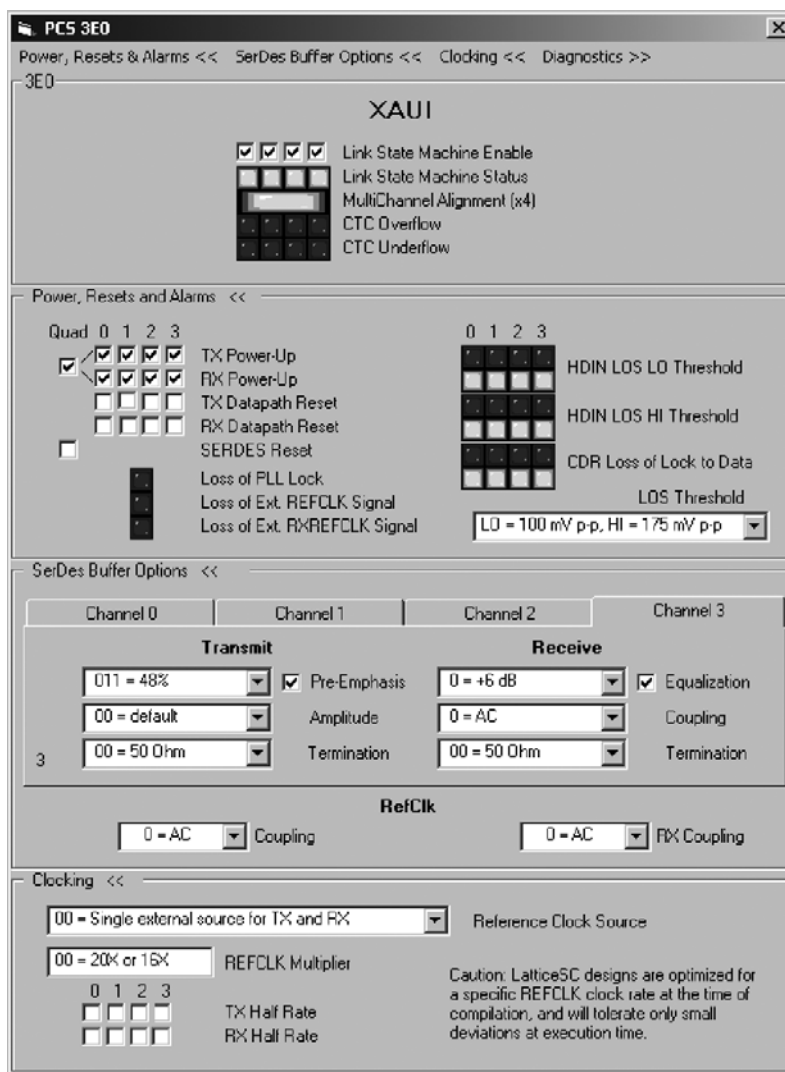


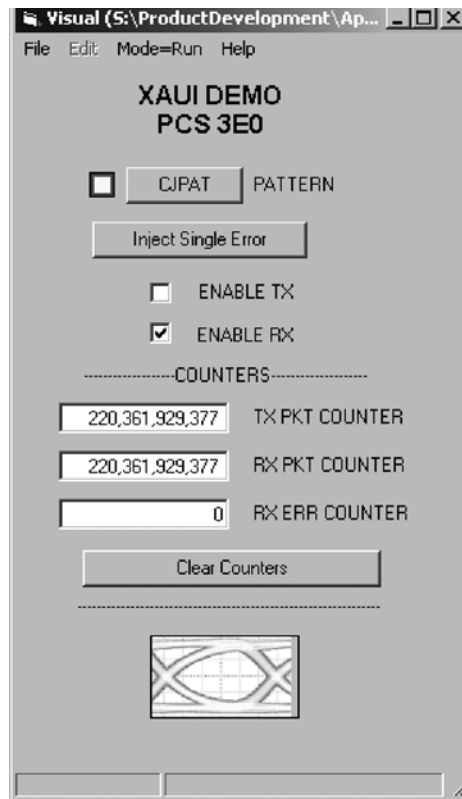
Figure 8. flexiPCS View of ORCAstra System



This demo also utilizes a CJPAT/CRPAT visual window as a plug-in to the base ORCAstra installation. Its purpose is to control and monitor the CJPAT/CRPAT generator/checker soft IP in the FPGA portion of the LatticeSC device. Figure 9 provides a screen capture of this window.

The visual window supports:

- The selection between CJPAT and CRPAT patterns
- The injection of a single error in the generator TX data
- Enabling and disabling both generator (TX) and checker (RX)
- Real-time statistics counters for number of packets generated (TX), received (RX), and the number of received packets with errors (RX ERR)

Figure 9. XAUI Generator/Checker ORCAstra Plug-in Visual Window

Agilent 8133A Pulse/Data Generator

Two Agilent 8133A pulse/data generators were used to supply external reference clock sources to the LatticeSC and Marvell 88X2040 devices.

For more information on this module, refer to the Agilent website at www.agilent.com.

Interoperability Testing

This section provides details on the XAUI interoperability test between the LatticeSC device and the Marvell 88X2040 device. The purpose of the test is to implement interoperability between one type #1 DUT (LatticeSC) and one Type #2a DUT (88X2040).

The test has the following characteristics:

- Independent (asynchronous) +/- 100 ppm clock sources clock the LatticeSC and 88X2040 devices. For these particular devices, the data rate across four lanes is $4 \cdot 8/10 \cdot 20 \cdot F$, where F is the source clock frequency. The data rate in XAUI mode is 10 Gbps. This means an independent clock source of 156.25 MHz (+/- 100 ppm) or larger clocks each device.
- The LatticeSC device transmits CJPAT data to the 88X2040 device
- The 88X2040 device loops the data at its XGMII interface back to the LatticeSC device

By the end of the test:

- The LatticeSC device RX ERR counters should remain at zero
- The LatticeSC device visual window counters should report as many TX packets generated as RX packets received

- The amount of test time should be longer than 30 minutes to ensure the error rate is less than 10⁻¹² with 99.999999% accuracy

Test Setup

The setup includes:

- A Tyco Backplane (using the 16" HM-ZD slots)
- Marvell 88X2040 evaluation LB SMA board (with the 88X2040 devices)
- LatticeSC Communications Platform evaluation board
- One SMA to HM-ZD daughter card to go from the Marvell SMA connections to the Tyco HM-ZD slot
- One SMA to HM-ZD daughter card to go from the LatticeSC SMA connections to the Tyco HM-ZD slot
- A PC for software control/monitoring
- Two Agilent 8133A Data/Pulse Generators to provide an external reference clock to each of LatticeSC and Marvell 88X2040 boards. The Agilent clock frequencies were set to 170 MHz. This corresponds to a data rate of $4 \times 8/10 \times 20 \times 170 = 10.89$ Gbps.
- About 12" of SMA cable to connect the Marvell board to its daughter card
- About 36" of SMA cable to connect the LatticeSC board to its daughter card

Figure 10 is a block diagram of the test setup.

Figure 11 shows the Marvell 88X2040 board, the LatticeSC board, and the TYCO backplane connections.

Figure 10. Test Setup Block Diagram

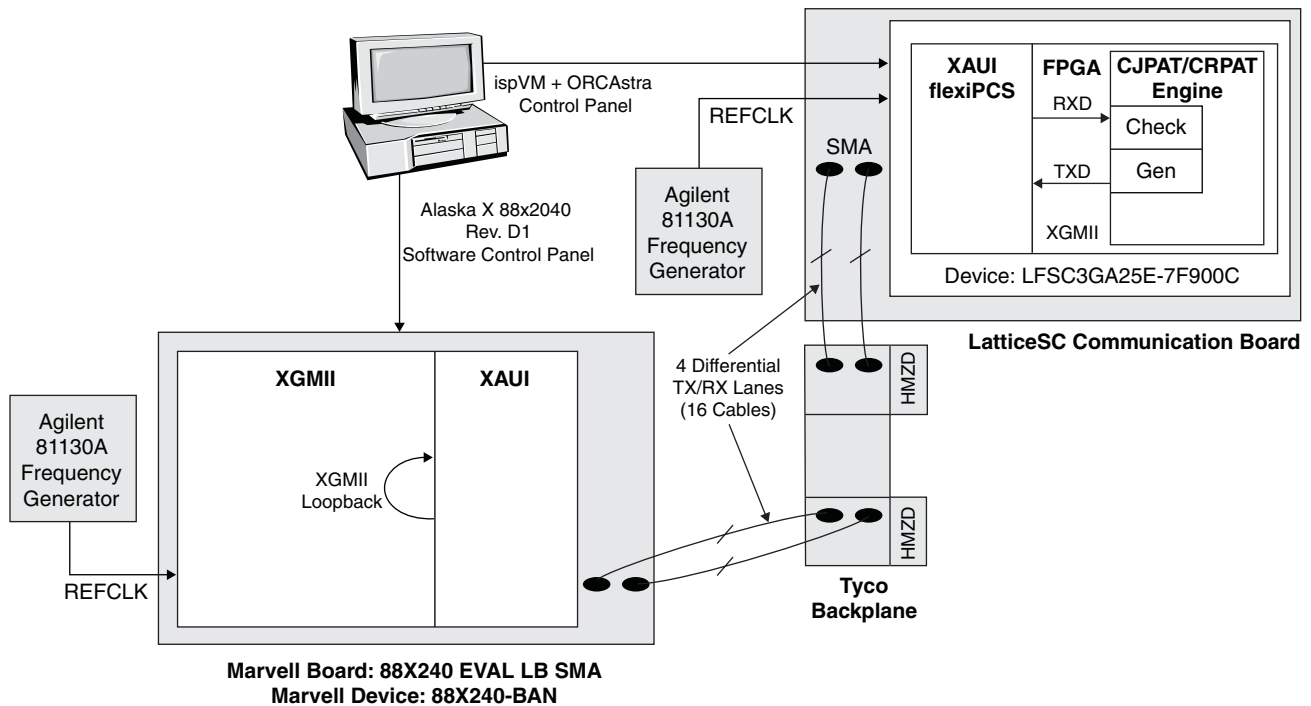
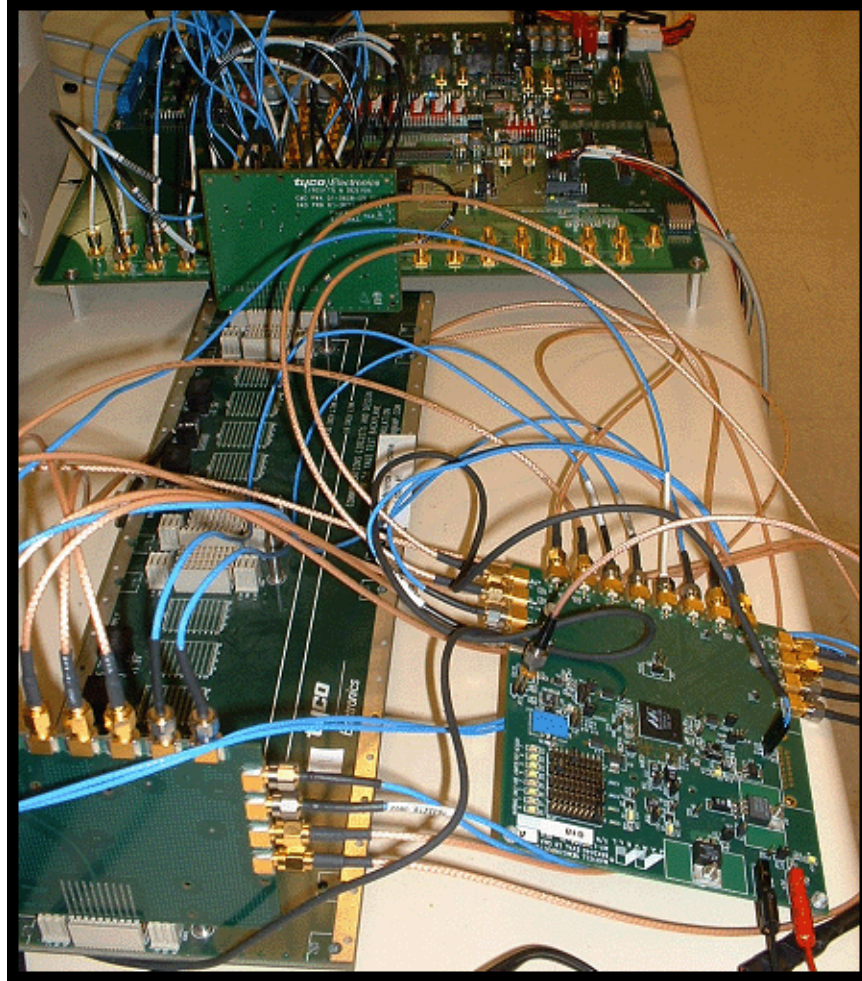


Figure 11. Board Connections of Test Setup



Test Description

LatticeSC Communications Platform Evaluation Board

In the TX direction, the LatticeSC device sends CJPAT data to the Marvell board.

In the RX direction, the LatticeSC device receives CJPAT data from the Marvell board. Meanwhile, the XAUI Quad generator/checker plug-in visual window (see Figure 9) records RX PKT, RX PKT, and RX ERR statistics.

Marvell 88X2040 Evaluation Board

The 88X2040 receives CJPAT data from the LatticeSC device and loops it back at its XGMII interface in the other direction.

Results

The setup ran for over 68 hours, during which over 220 billion packets were transmitted/received error-free (see Figure 9). The TX PKT and RX PKT counts were identical. The RX ERR counter remained at zero.

Summary

In conclusion, the LatticeSC FPGA family is fully XAUI interoperable with the Marvell 88X2040 device.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2006	01.0	Initial release.