

Introduction

The Serial Gigabit Media Independent Interface (SGMII) is a connection bus for Ethernet MACs and PHYs defined by Cisco Systems. It replaces the classic 22-wire GMII connection with a low pin count, 4-pair, differential SGMII connection. The classic GMII interface defined in the IEEE 802.3 specification is strictly for gigabit rate operation. However, the Cisco SGMII specification defines a method for operating 10Mbps, 100Mbps and 1000Mbps over the interface. Moreover, the Cisco SGMII specification is comprised of more than just a bus interface definition; it defines a bridging function between SGMII and GMII buses.

The transmit and receive data paths leverage the 1000BASE-SX PCS defined in the IEEE 802.3z specification (clause 36). Control information, as specified in Table 1, is transferred from the PHY to the MAC to signal the change of the control information. This is achieved by using the Auto-Negotiation functionality defined in clause 37 of the IEEE specification 802.3z. Instead of the ability advertisement, the PHY sends the control information via its tx_config_Reg[15:0], as specified in Table 1, whenever the control information changes. Upon receiving control information, the MAC acknowledges the update of the control information by asserting bit 14 of its tx_config_Reg[15:0] as specified in Table 1.

This document provides a report on the SGMII Physical Layer interoperability tests between a LatticeSC™ device and the Marvell 88E1111/88E1112 devices. Specifically, this technical note discusses the following topics:

- Overview of LatticeSC devices and Marvell Alaska Ultra 88E1111/ 88E1112 devices.
- SGMII Physical Layer Interoperability testing of the LatticeSC and Marvell 88E1111/88E1112 devices.

Table 1. Definition of Control Information Passed Between Links via tx_config_Reg[15:0]

Bit Number	tx_config_Reg[15:0] Sent From the PHY to the MAC	tx_config_Reg[15:0] Sent From the MAC to the PHY
15	Link: 1 = link up, 0 = link down	0: Reserved for future use
14	Reserved for Auto-Negotiation acknowledge as specified in 802.3z	1
13	0: Reserved for future use	0: Reserved for future use
12	Duplex mode: 1 = full duplex, 0 = half duplex	0: Reserved for future use
11-10	Speed: Bit 11, 10: 11 = Reserved 10 = 1000 Mbps: 1000BASE-TX, 1000BASE-X 01 = 100 Mbps: 100BASE-TX, 100BASE-FX 00 = 10 Mbps: 10BASE-T, 10BASE2, 10BASE5	0: Reserved for future use
9-1	0: Reserved for future use	0: Reserved for future use
0	1	1

LatticeSC/flexiPCS™ Overview

LatticeSC Features

The LatticeSC family equipped with ASIC-like system level building blocks was designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today. This family of devices includes features to meet the needs of today's communication network systems. These features include up to 7.8 Mbits of embedded block RAM, dedicated logic to support system level standards such as Rapid IO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. Furthermore, the devices in this family feature clock multiply, divide

and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUX that are required in today's high-end system designs.

All LatticeSC devices also feature up to 32 channels of embedded SERDES with associated Physical Coding Sub-layer (PCS) logic. The flexiPCS logic can be configured to support numerous industry standard high-speed data transfer protocols. Each channel of flexiPCS logic contains dedicated transmit and receive SERDES

LatticeSC SGMII Solution

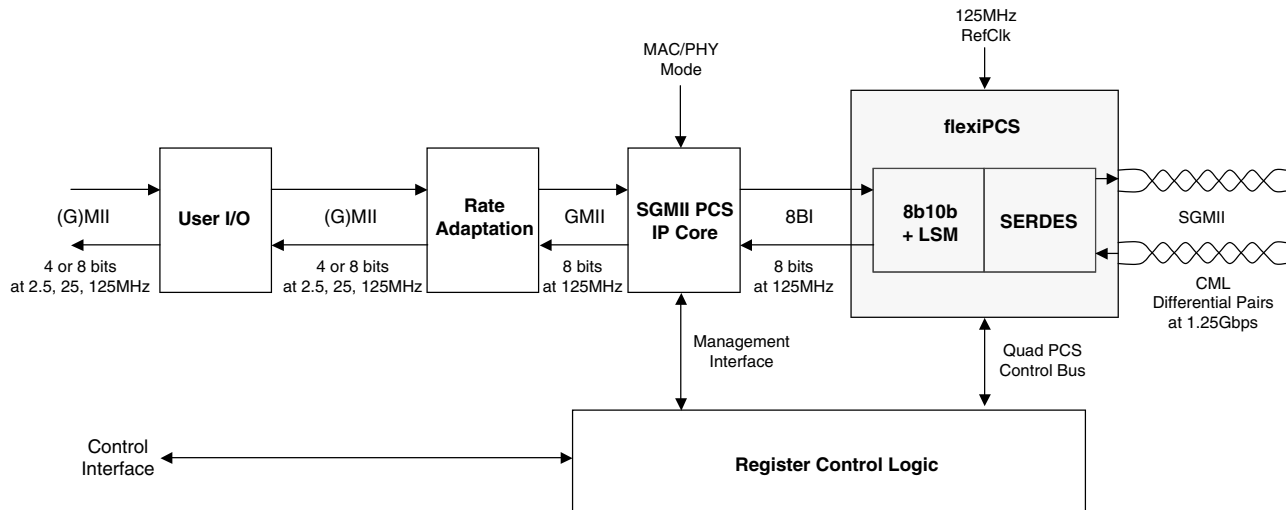
The LatticeSC achieves SGMII compliance by combining both a flexiPCS block and SGMII soft IP in FPGA logic.

The LatticeSC SGMII Solution has the following features:

- Word Alignment based on IEEE 802.3-2002 defined alignment characters (flexiPCS)
- 8b/10b encoding/decoding (flexiPCS)
- Link State Machine functions compliant with the IEEE 802.3-2002 specification (flexiPCS)
- Conforms to the Cisco SGMII Specification, Revision 1.7
- 4-bit or 8-bit (G)MII Interface operating at 10Mbps, 100Mbps, or 1Gbps
- Pin selectable MAC/PHY mode for auto negotiation
- Management registers access through serial or parallel control interface
- 2-wire, CML differential SGMII Interface operating at 1.25Gbps (flexiPCS)
- Transmit SGMII clock embedded in data stream (no external SGMII transmit clock) (flexiPCS)
- Receive SGMII clock recovered from data stream (no external SGMII receive clock) (flexiPCS)

Figure 1 illustrates the LatticeSC SGMII solution.

Figure 1. LatticeSC SGMII Solution



Marvell Alaska Ultra 88E1111/88E1112 Overview

88E1111/88E1112 Features

The Alaska Ultra 88E1111/88E1112 Gigabit Ethernet Transceivers are physical layer devices for Ethernet 1000BASE-T, 100BASE-TX, and 10BASE-T applications. They contain all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 3 and CAT 5 unshielded twisted pair.

The 88E1111/88E1112 devices support the Gigabit Media Independent Interface (GMII), Reduced GMII (RGMII), Serial GMII (SGMII), the Ten-Bit Interface (TBI), and Reduced TBI (RTBI) for direct connection to a MAC/Switch port.

The 88E1111/88E1112 devices incorporate a 1.25GHz SERDES, which may be directly connected to a fiber-optic transceiver for 1000BASE-T/1000BASE-X media conversion applications. Additionally, the 88E1111/88E1112 devices may be used to implement 1000BASE-T Gigabit Interface Converter (GBIC) or Small Form Factor Pluggable (SFP) modules.

The 88E1111/88E1112 devices use advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The devices achieve robust performance in noisy environments with very low power dissipation.

The Alaska Ultra 88E1111/88E1112 features include:

- 10/100/100BASE-T IEEE 802.3 compliant
- Support for GMII, TBI, RGMII, RTBI, and SGMII
- Integrated 1.25GHz SERDES for 1000BASE-X fiber applications
- The 88E1112 device also supports 100BASE-FX
- Four RGMII timing modes
- Three energy detect modes as well as a low power COMA mode
- Three loopback modes for diagnostics
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic polarity correction
- IEEE 802.3u compliant Auto-Negotiation
- CRC checker, packet counter
- Automatic detection of fiber or copper media
- Virtual Cable Tester (VCT)
- Selectable MDC/MDIO interface or Two-Wire Serial Interface

Test Equipment

The equipment below is used in the interoperability tests.

Spirent SmartBits 2000 Protocol Analyzer

Spirent Communications' SmartBits 2000 (SMB-2000) has become the industry standard for measuring the performance limits of everything from an emerging technology in a development lab to the largest enterprise network. The SMB- 2000 is widely used to test a variety of network devices and complex network configurations, including 10/100 Mbps Ethernet, Gigabit Ethernet, ATM, and Frame Relay.

Figure 2 illustrates the SMB-2000 analyzer with a 1000BASE-T copper module (GX-1420B, right-most module with RJ45 cable attached).

Figure 3 illustrates the GUI command console for the SMB-2000. The GX-1420B module is also shown to the right of the screen.

Figure 2. SmartBits 2000 Protocol Analyzer with 1000BASE-T Module

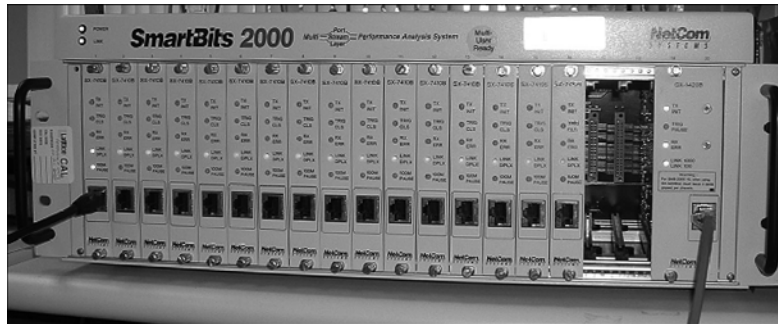
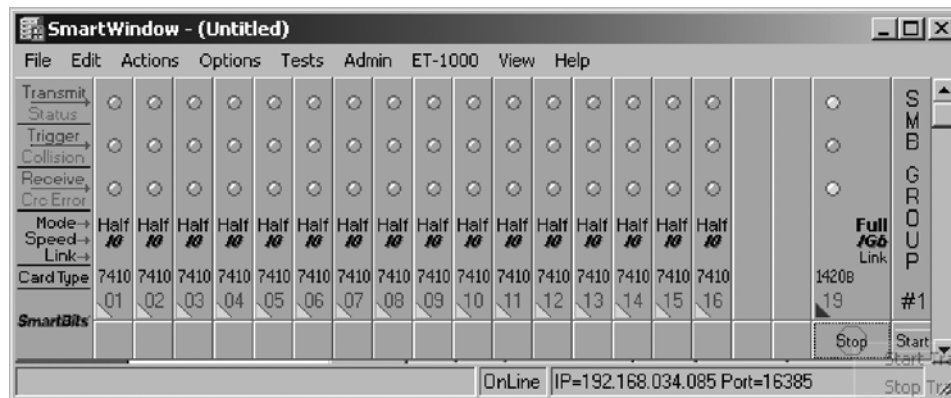


Figure 3. SmartBits 2000 GUI Controls



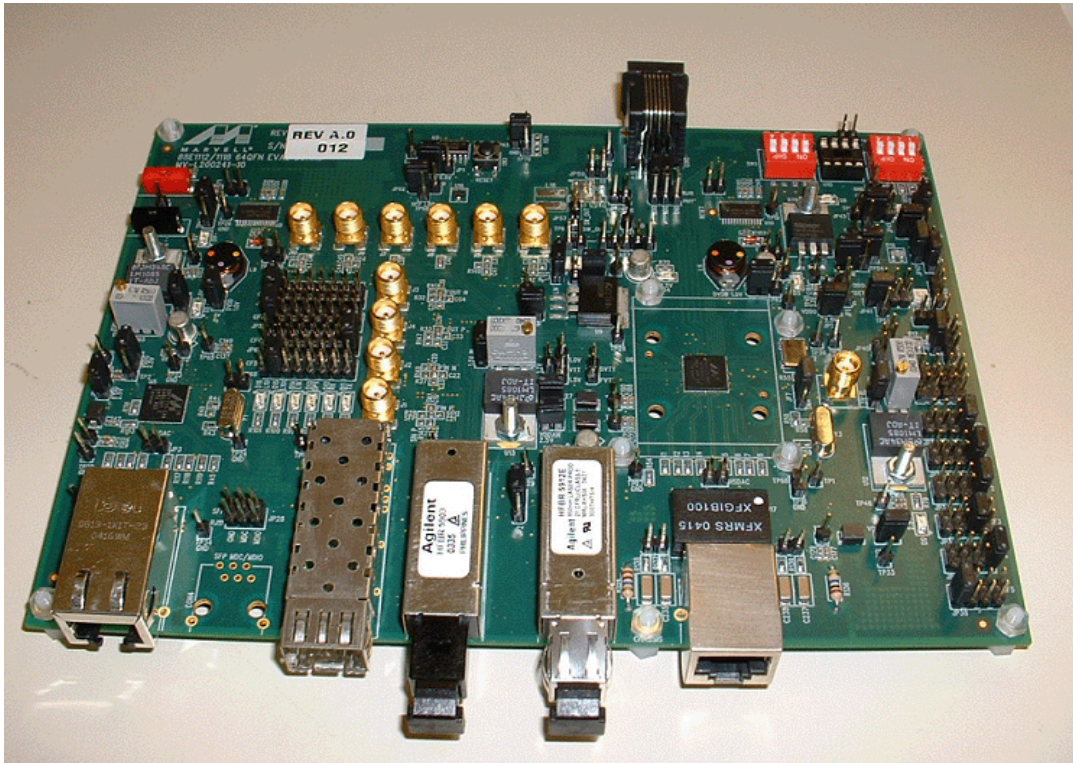
Marvell 88E1112 64 QFN Evaluation Board

The Marvell 88E1112 64 QFN evaluation board includes:

- 88E1111 device
- 88E1112 device
- On-board oscillator clock sources
- MDIO/MDC monitoring/control to both devices
- SGMII interface between the 88E1111 and the 88E1112
- RJ-45 connector for MDI access to the 88E1111
- Two Transmit SMAs and two Receive SMAs for access to the 88E1112 SERDES

Figure 4 illustrates the 88E1112 64 QFN evaluation board.

Figure 4. Marvell 88E1112 64 QFN Evaluation Board



Marvell Alaska Virtual Cable Tester Software

The Alaska Virtual Cable Tester Software GUI controls the 88E1111/88E1112 parts and monitor status bits. Figure 5 shows the VCT GUI. The GUI is mainly used for 1000-BASE-T or 1000BASE-X modes.

In SGMII mode, the PHY Register Control Panel is used instead to control and monitor the 88E1112 registers. Figure 6 illustrates the PHY Register Control Panel.

Figure 5. ALASKA Virtual Cable Tester Software GUI

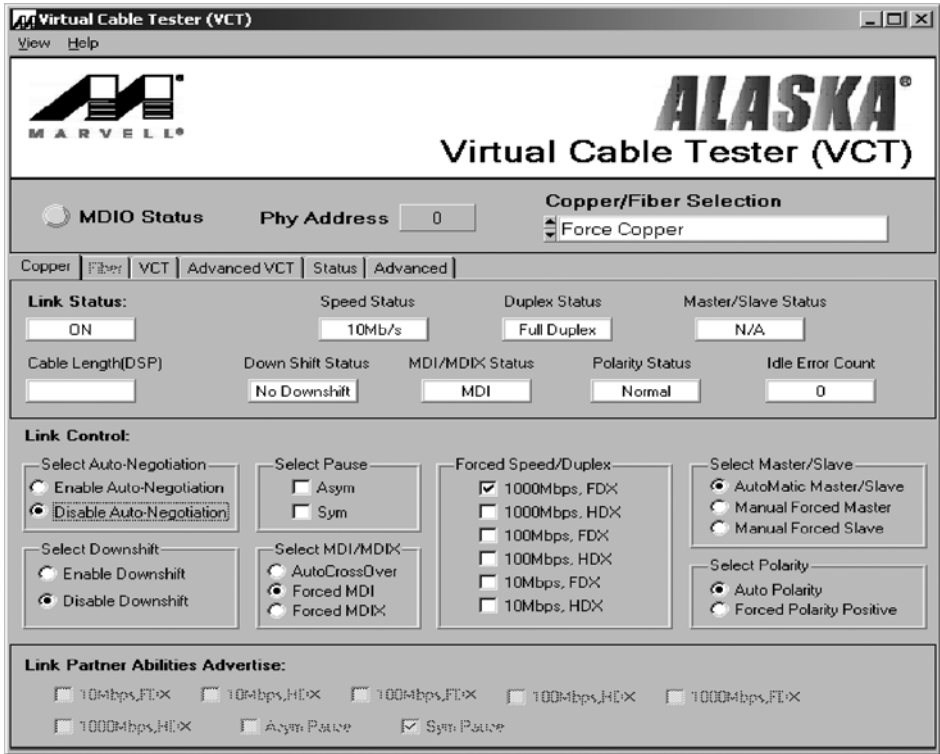
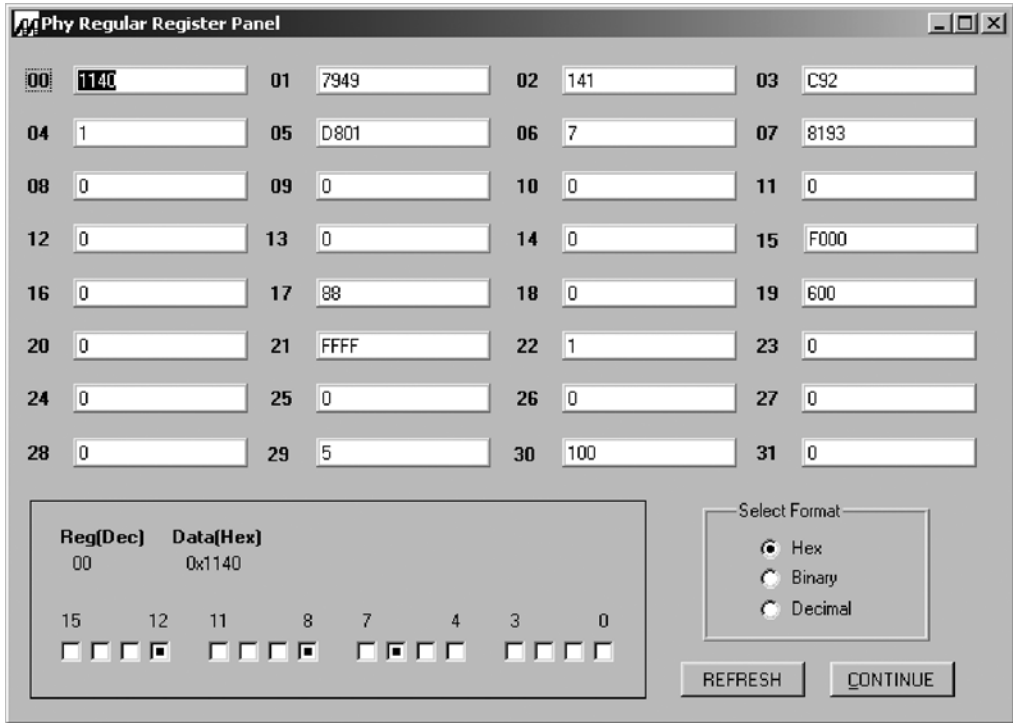


Figure 6. PHY Register Control Panel



Agilent 81130A Pulse/Data Generator

The Agilent 81130A pulse/data generator was used to supply an external 125MHz reference clock source to the LatticeSC flexiPCS.

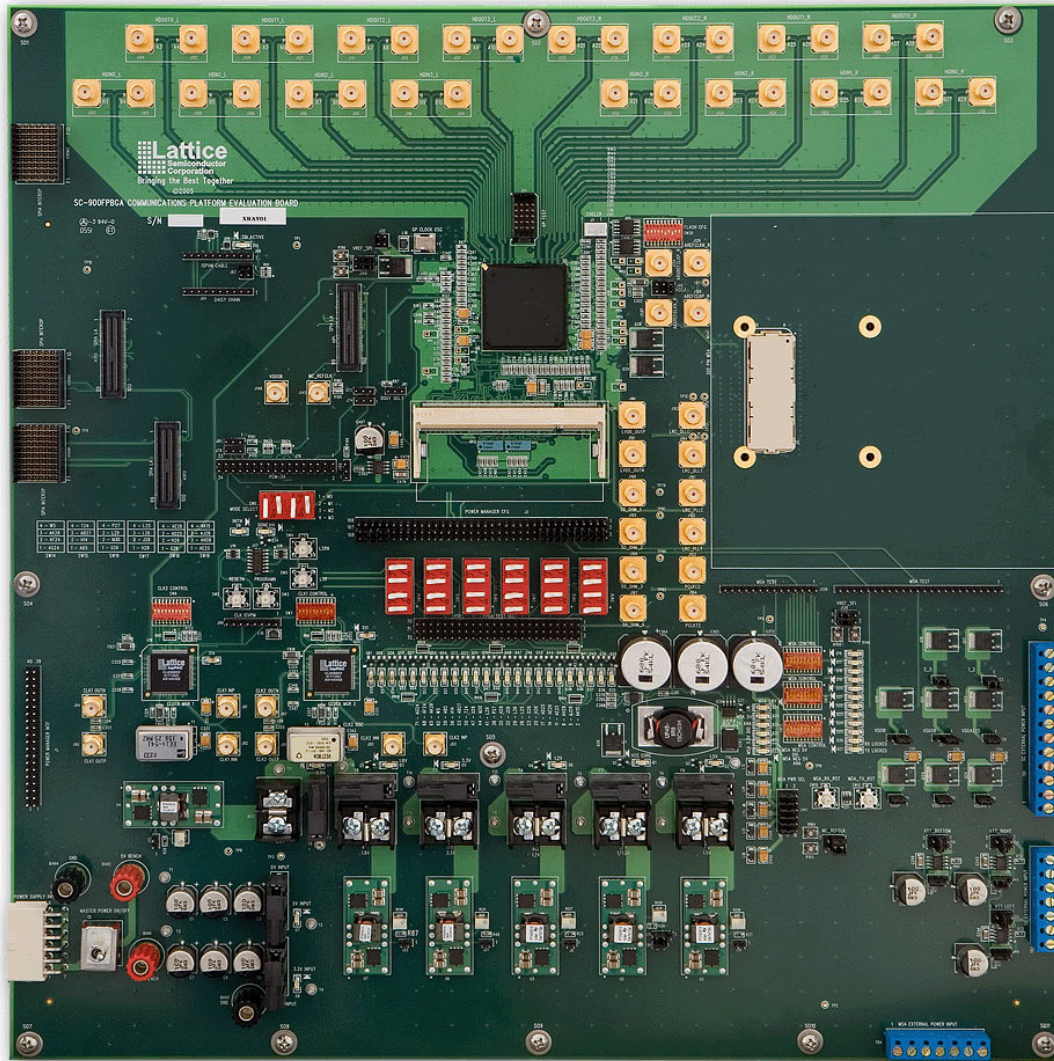
For more information this module, please refer to Agilent's website: www.agilent.com.

LatticeSC Communications Platform Evaluation Board

The LatticeSC Communications Platform Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeSC FPGA or aid in development of custom designs. Each LatticeSC Communications Platform Evaluation Board contains:

- LFSC3GA25E-6F900C FPGA Device
- SMA test points for high-speed SERDES and Clock I/O
- On-board power connections and power sources
- On-board interchangeable clock oscillator
- On-board reference clock management using Lattice ispClock™ devices
- Various high-speed layout structures
- On-board Flash configuration memory
- Various LEDs, switches, connectors, headers, SMA connections for external clocking, and on-board power control

Figure 7 shows the LatticeSC Communications Platform Evaluation Board.

Figure 7. LatticeSC Communications Platform Evaluation Board

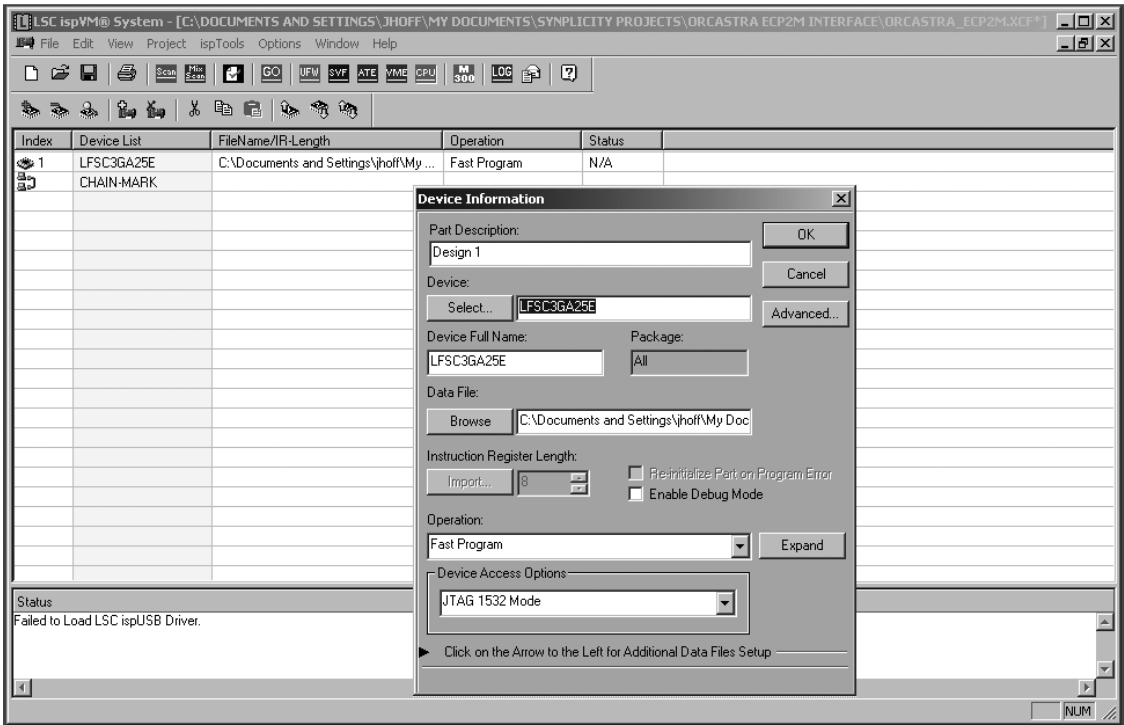
ispVM® System Software

The ispVM System is included with Lattice's ispLEVER® software, and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP™ devices using JEDEC and bitstream files generated by Lattice Semiconductor and other design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeSC bitstream to configure the FPGA in SGMII mode.

Figure 8 shows a screen shot of the ispVM System.

Figure 8. ispVM System



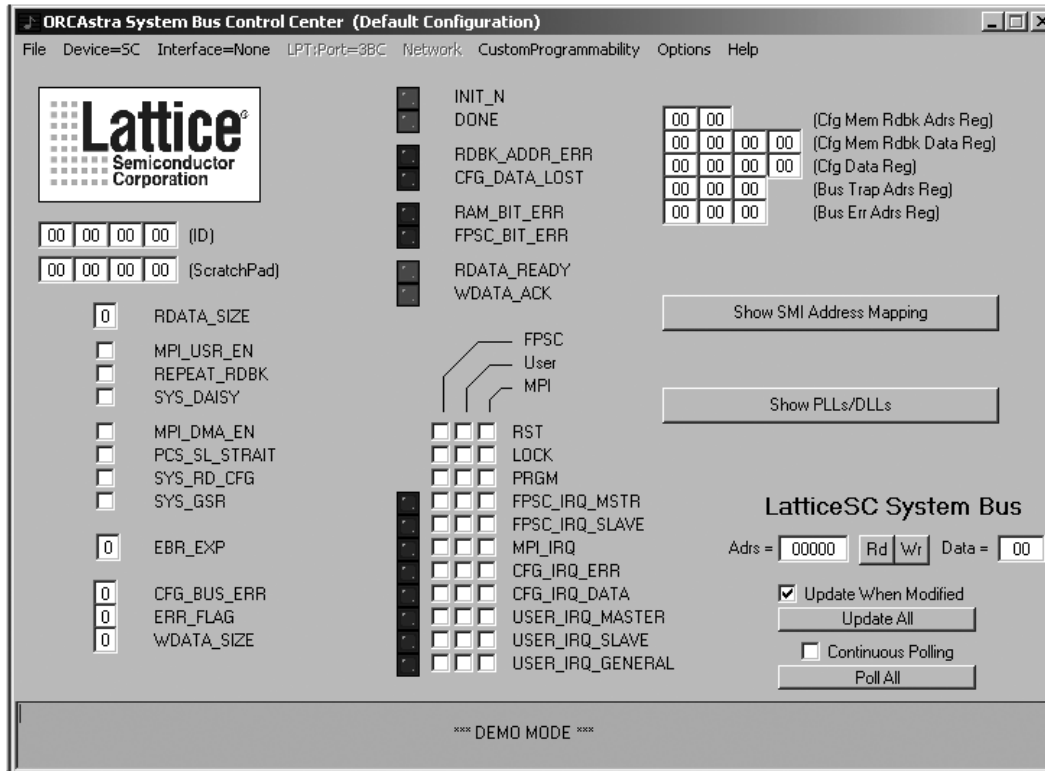
ORCAstra System

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA or FPSC by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to the board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of an FPSC.

Figure 9 is a screen shot of the ORCAstra system

Figure 9. ORCAstra System



Interoperability Testing

This section provides details on SGMII Physical Layer interoperability tests between the LatticeSC device and the Marvell 88E1111/ 88E1112 devices. The purpose of these tests is to confirm the correct processing of 1000BASE-T copper protocol from the SMB-2000, through the 88E1111/88E1112 devices, and ending at the LatticeSC (G)MII interface, and then back in the other direction. Particularly, the tests verify:

- The ability to auto negotiate successfully
- The ability to transfer packets across the system in an asynchronous way

Test Setup

Figure 10 shows the test set-up. Figure 11 is a block diagram of the test set-up.

The set-up includes:

- Spirent SMB-2000 with a GX-1420B module
- Marvell 88E1112 evaluation board (with the 88E1111/88E1112 devices)
- LatticeSC Communications Platform evaluation board
- PC for software control/monitoring
- Agilent 811130A Data/Pulse Generator to provide an external 125MHz reference clock to the LatticeSC flexi-PCS.

Figure 10. Test Setup

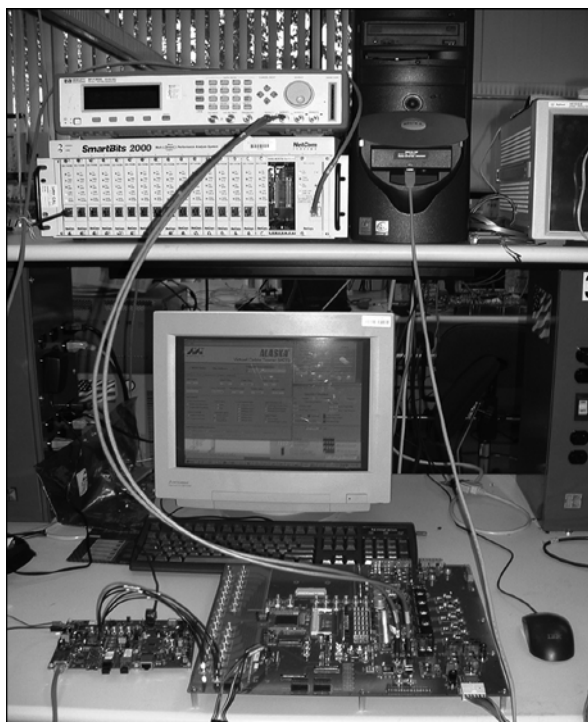
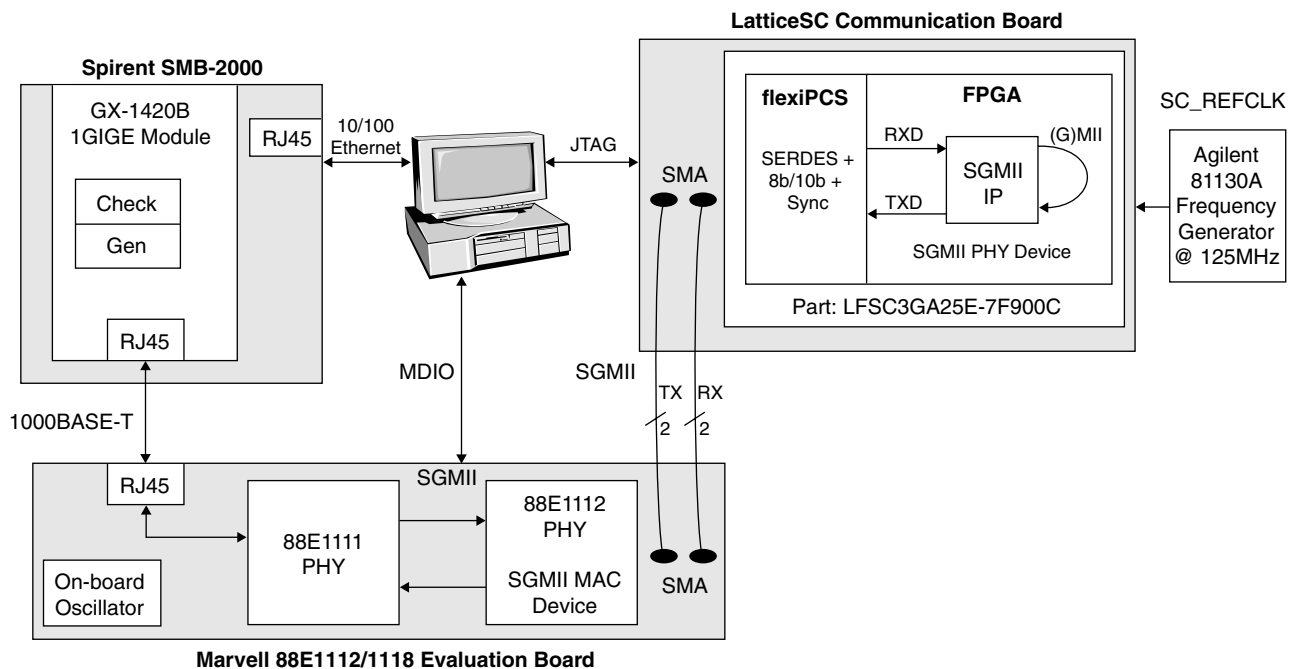


Figure 11. Test Setup Block Diagram



Test Description

The following describes how the SGMII Physical Layer Interoperability is achieved.

SMB-2000

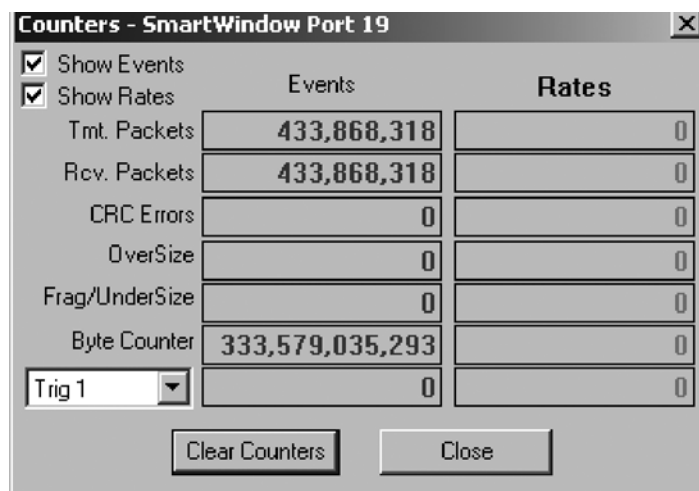
The GX-1420B module generates and checks full protocol compliant gigabit ethernet packets. The setup is as follows:

- Random source/destination addresses
- Random payload content
- Random payload length
- 0.096µsec IPG GAP

Figure 12 illustrates the SMB-2000 counter window used to keep track of transmission and reception statistics.

The SMB-2000 connects to the Marvell 88E1112/ 88E1118 evaluation board via an RJ-45 cable. It transmits the gigabit Ethernet packets to the 88E1111 device in the TX direction, and checks them back from the 88E1111 device in the RX direction.

Figure 12. SMB-2000 Counter Window



Marvell 88E1112/88E111 Evaluation Board

In one direction, the 88E1111 device receives 1000BASE-T packets from the SMB-2000 and sends it to the 88E1112 device via its SGMII interface. In the other direction, the opposite flow of data occurs.

In one direction, the 88E1112 part receives SGMII packets from the 88E1111 and sends it to the LatticeSC board via SMAs on its SGMII interface. In the other direction, the opposite flow of data occurs.

Note that because the 88E1112 is configured as an SGMII MAC device, the LatticeSC SGMII IP is programmed as a PHY device via register settings.

LatticeSC Communications Platform Evaluation Board

In the RX direction, The LatticeSC flexiPCS recovers SGMII packets from the 88E1112 device and the SGMII IP converts them into (G)MII format.

The (G)MII loopback logic in the FPGA portion loops the (G)MII data back into the TX direction. The LatticeSC device then transmits the SGMII packets back to the 88E1112 device. The LatticeSC SGMII IP is programmed as an SGMII PHY device.

Results

Correct auto negotiation was verified by monitoring both the LatticeSC SGMII solution status signals and registers and the Marvell PHY Register Panel (see Figure 6). The tx_config_Reg[15:0] content transmitted from the SGMII PHY (LatticeSC) to the SGMII MAC (88E1112) was also read back at register 5 of page 1 (see Figure 6). The content of that register was hD801. According to Table 1, this corresponds to the following LatticeSC SGMII PHY information:

- Link is up
- Auto-negotiation acknowledgement
- Full duplex operation
- Advertised speed of 1000Mbps at the (G)MII interface

The Smartbits SMB-2000 GX-1420B counter window (as shown in Figure 12) was monitored for error-free packet transmission and reception. Additionally, the Lattice ORCAstra System GUI was also monitored for proper link synchronization. The setup ran for over 40 minutes, during which about 433 million packets were transmitted/received error-free (see Figure 12).

Summary

In conclusion, the LatticeSC FPGA family offers users SGMII Physical Layer support and is fully inter-operable with Marvell 88E1111/88E1112 devices.

Technical Support Assistance

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Revision History

Date	Version	Change Summary
November 2006	01.0	Initial release.