LatticeSC PCI Express x8 Evaluation Board

User's Guide

April 2007
Revision: EB19_01.3

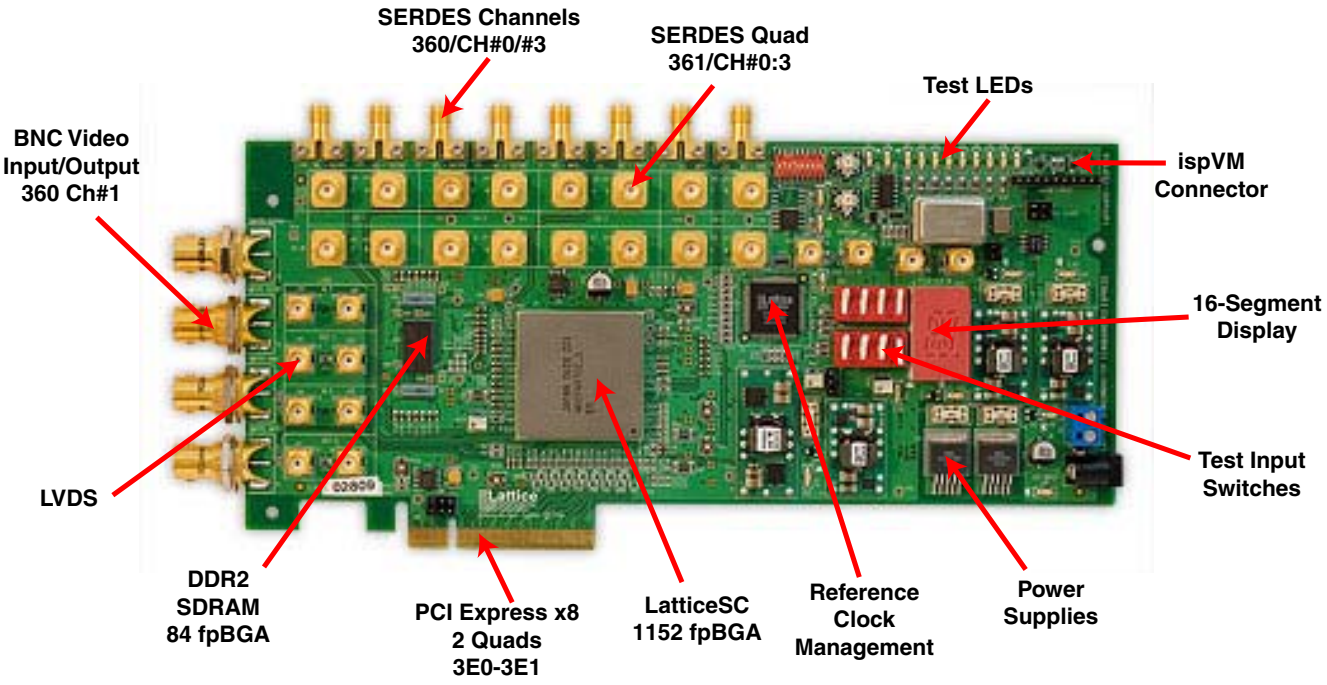
Introduction

This user's guide describes the LatticeSC PCI Express x8 Evaluation Board featuring the LatticeSC LFSCM3GA80EP1-6FC1152C FPGA device. This stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that require high-speed SERDES interfaces and/or PCI Express protocols.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete user evaluation of the LatticeSC device. This user's guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeSC FPGA.

Figure 1. LatticeSC PCI Express x8 Evaluation Board



Features

- LatticeSCM-80 device in 1152 fcBGA package
- SERDES interface to x8 PCI Express edge fingers
- DDR2 memory device
- SERDES high-speed interface SMA test points and clock connections
- Power connections and power sources
- ispVM® programming support
- On-board and external reference clock sources
- Interchangeable clock oscillators
- On-board reference clock management using Lattice ispClock™ devices
- ORCAstra demonstration software interface via standard ispVM JTAG connection

- Various high-speed layout structures
- User-defined input and output points
- SMA connectors included (10) for high-speed clock or data interfacing
- Performance monitoring via test headers, LEDs and switches

This user's guide includes top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 2 shows the functional partitioning of the board.

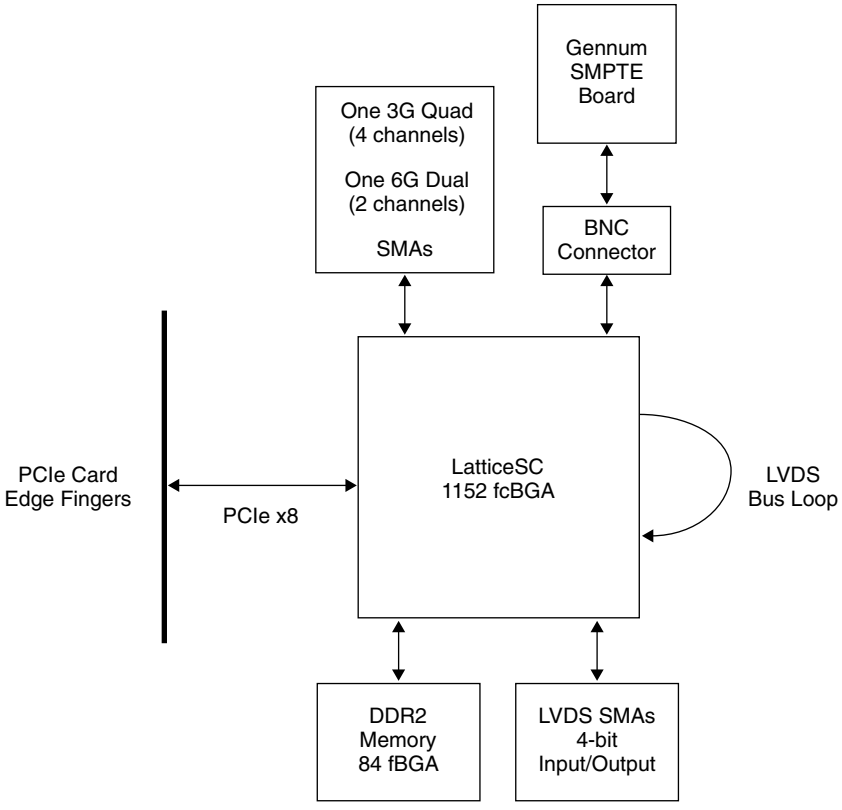
Additional Resources

For additional information and resources related to this board, including updated documentation and hardware/software demos, please see the Lattice web site at: www.latticesemi.com/boards, and navigate to the appropriate page for this board.

A PCI Express demonstration is also available on-line, including a GUI and drivers for a PCI Express solution using this board.

Lattice makes its best effort to provide evaluation board designs to help users with evaluation and development. However it remains the user's responsibility to verify proper and reliable operation of Lattice products in their end application by consulting documentation provided by Lattice. Differences in component selection and/or PCB layout in the user's application may significantly affect circuit performance and reliability.

Figure 2. Evaluation Board Block Diagram



Note: This board not included with Evaluation Kit.

LatticeSC Device

This board features a LatticeSC FPGA with a 1.2V core supply. It can accommodate all pin compatible LatticeSC devices in the 1152-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeSC Family Data Sheet on the Lattice web site at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFSCM3GA80 device. Available I/Os and associated sysIO™ banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeSC PCI Express x8 Evaluation Board is ready to power on. The evaluation board can be supplied with power from an AC wall-type transformer power supply shipped with the board. Or it can be supplied from a bench-top supply via terminal screw connections. It also has provisions to be supplied from the PCI Express edge fingers from a host board.

To supply power from the factory-supplied wall transformer, simply connect the output connection of the power cord to J3 and plug the wall transformer into an AC wall outlet.

Power Supplies

(see Appendix A, Figure 4)

The evaluation board incorporates an alternate scheme to provide power to the board. The board is equipped to accept a main supply via the TB1 connection. This connection is provided to use with a bench-top supply adjusted to provide a nominal 12V DC.

All input power sources and on-board power supplies are fused with surface mounted fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 1. Board Power Supply Fuses- (see Appendix A, Figure 4)

F1	1.0V/1.2V Fuse
F2	3.3V Fuse
F3	1.5V Fuse
F4	1.2V Fuse
F5	2.5V Fuse
F6	1.8V Fuse

Table 2. Board Power Supply Indicators- (see Appendix A, Figure 4)

D14	1.0V/1.2V VCC Core Source Good Indicator
D15	1.5V Source Good Indicator
D16	1.8V Source Good Indicator
D12	2.5V Source Good Indicator
D13	3.3V Source Good Indicator
D17	1.2V Source Good Indicator

Alternatively, external power can be connected rather than the wall transformer power pack.

Table 3. Board Supply Disconnects- (see Appendix A, Figure 3)

TB1	Screw terminal for 12V DC Pin1(square PCB pad) -> +12V DC Pin2 -> Ground

PCI Express Power Interface

(see Appendix A, Figure 5)

Power can be sourced to the board via the PCB Edge Finger (CN1). This interface allows the user to provide power from a PCI Express host board.

Programming/FPGA Configuration

(see Appendix A, Figure 2)

A programming header is provided on the evaluation board, providing access to the LatticeSC JTAG port.

Note: An ispDOWNLOAD® Cable is included with each ispLEVER® design tool shipment. Cables may also be purchased separately from Lattice.

ispVM Download Interface

J2 is a10-pin JTAG connector used in conjunction with the ispVM System software and ispDOWNLOAD Cable to program and control the device.

Table 4. JTAG Programming Connector (see Appendix A, Figure 2)

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE
Pin 10	INITN

Programming Daisy Chain

This board includes two Lattice programmable devices that can be programmed in a daisy chain. A jumper setting of J93 controls the chain. Both devices are in the programming chain from the JTAG header J2 with jumpers across Pins{1-2} and Pins{3-4}. If the user desires to only program U1, only a jumper should be across Pins{2-4}.

Download Procedures

Requirements

- PC with ispVM System v.14.3 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). *Note: An option to install these drivers is included as part of the ispVM System set-up.*
- ispDOWNLOAD Cable (HW-USBN-2A, HW-DLN-3C, etc.)

JTAG Download

The LatticeSC device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

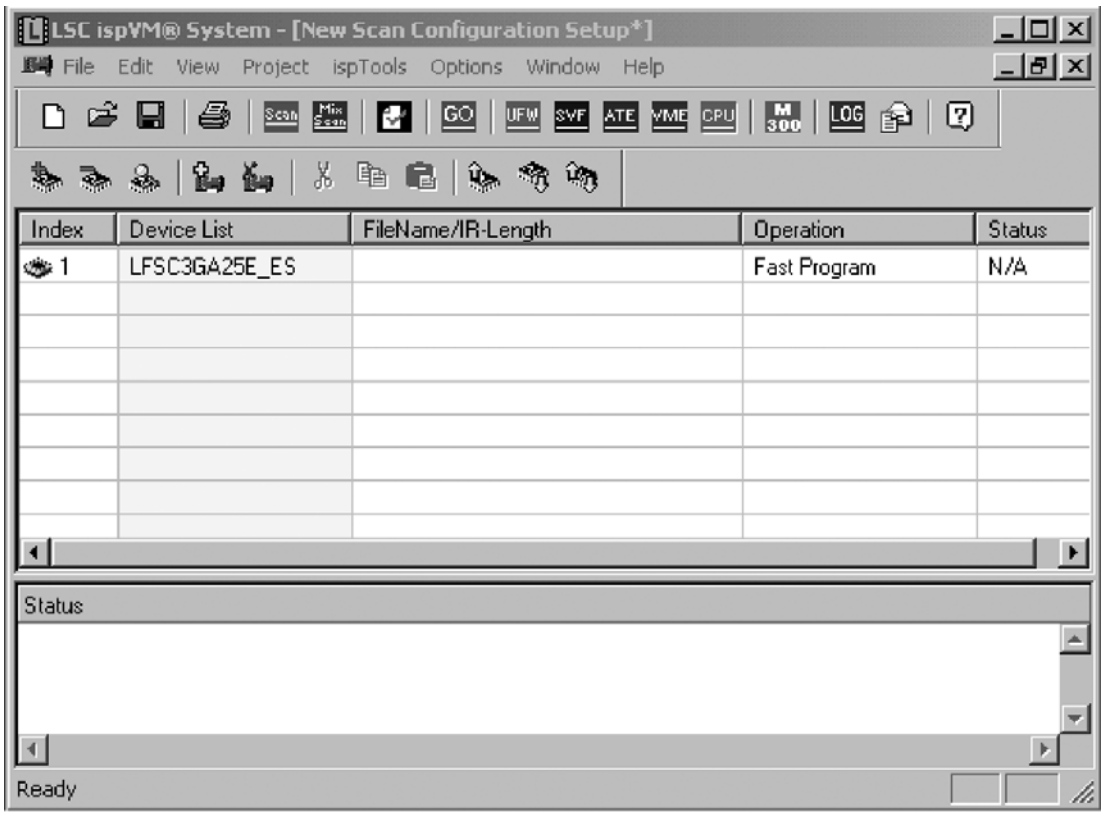
1. Connect the ispDOWNLOAD cable to the appropriate header. J2 is used for the 1x10 cable.

   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any*

other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeSC FPGA device and render the board inoperable.

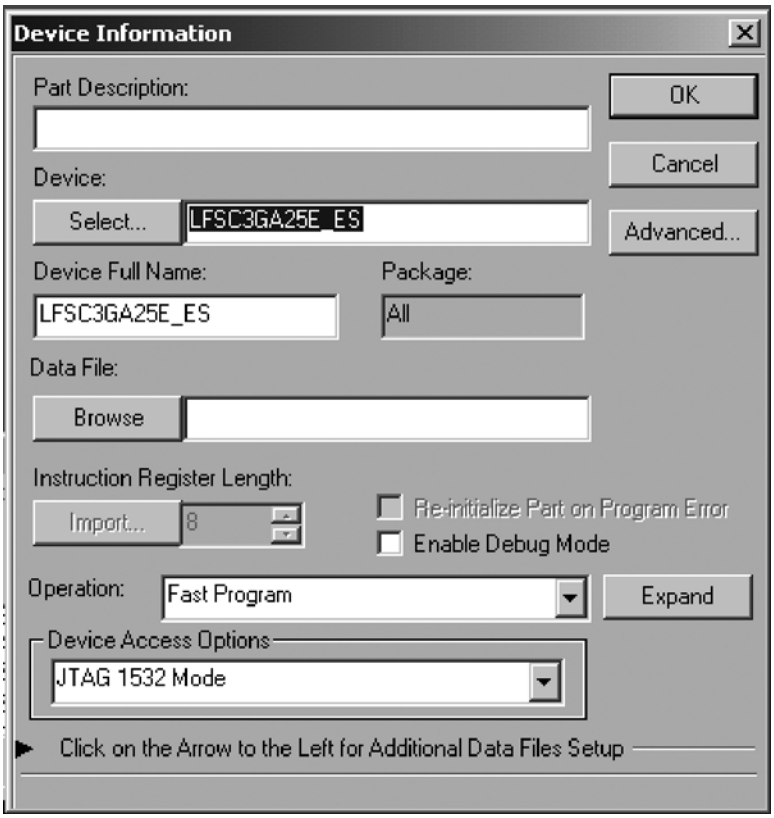
2. Connect the LatticeSC Evaluation Board to the appropriate power sources and power up the board.
3. Start the ispVM System software.
4. Press the **SCAN** button located in the toolbar. The LatticeSC device should be automatically detected.

Figure 3. ispVM Main Window



5. Double-click the device to open the device information dialog. In the device information dialog, click the **Browse** button located under **Data File**. Locate the desired bitstream file (.bit). Click **OK** to both dialog boxes.

Figure 4. Device Information Dialog Box



6. Click the green **GO** button. This will begin the download process into the device. Upon successful download, the device will be operational.

Configuration Status Indicators
(see Appendix A, Figure 2)

These LEDs indicate the status of configuration to the FPGA.

- D1 illuminated (red) – This indicates that the programming was aborted or reinitialized driving the INITN output low.
- D4 illuminated (green) – This indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D11 illuminated (green) – Flashes to indicate TDI activity.
- D21 illuminated (red) – This indicates that PROGRAMN is low.
- D23 illuminated (red) – This indicates that GSRN is low.

PROGRAMN & RESETN
(see Appendix A, Figure 2)

These push-button switches assert/de-assert the logic levels on the PROGRAMN (SW5) and RESETN (SW4). Depressing the button drives a logic level "0" to the device.

MODE [3:0]
(see Appendix A, Figure 2)

The FPGA MODE pins are preset on the board for SPI03 programming mode. JTAG programming is independent of the MODE pins and is always available to the user

On-Board Flash Memory
(see Appendix A, Figure 2)

Three memory devices (U2, U3 and U22) are on board for non-volatile configuration memory storage. SW3 is used to control writing and reading from the memory. U2 and U3 are 4M 8-pin SOIC Flash devices and U22 is a 64M 16-pin TSSOP Flash device. U22 is located on the bottom side (secondary) of the PCB. U2 and U22 occupy the same connections. Therefore, they can not be populated simultaneously. U22 is typically installed at assembly.

Refer to Lattice technical note TN1100, *SPI Serial Flash Programming Using ispJTAG on LatticeSC FPGAs* for recommended procedures and software usage.

To use both SPI Flash devices to program the LatticeSC device, the user must write to the Flash devices individually. This is accomplished by setting SW3 accordingly. Writing to Flash #1 (U2), close 3 and 5 switch positions (ON) and open all others.

Writing to Flash #2 (U3), close 2 and 4 switch positions (ON) and open all others.

For reading from the Flash devices individually, use the same switch settings as described for writing. For reading from both Flash devices in a cascading format, close switch positions (1, 3, 4, 5, 8).

FPGA Clock Management

(see Appendix A, Figure 9)

The evaluation board includes various features for generating and managing on-board clocks. The clocks are generated from either input provided from SMAs (see Table 5) or from crystal oscillators (Y1 and Y3. Y1 is socketed for interchangeability and Y3 is a 312.5MHz surface-mount with an enable/disable jumper J101).

Both of these input clock sources are routed through the Lattice ispClock5620A Programmable Clock Management devices (U21). These clock management devices allow for clock synthesis and buffering.

Table 5. Reference Clock Input SMA Connections

J91	U21 Reference + Input
J92	U21 Reference - Input

U21 are Lattice ispClock5620A In-System-Programmable analog circuits. These devices allow designers to implement clock distribution networks supporting multiple synchronized output frequencies using a single integrated circuit. By integrating a Phase-Locked Loop (PLL) along with multiple output dividers, the ispClock5620A can derive up to five separate output frequencies from a single input reference frequency. The PAC-Designer® software (available from the Lattice web site at www.latticesemi.com) is used to program the ispClock features.

ispClock supports reference clocks in the range of 10 to 320 MHz. The duty cycle of the clock source need not be 50%; the only requirement is that both the HIGH and LOW times of this signal must be 1.25ns or longer. The following standards are supported with either minimal or no external components: LVTTL / LVCMOS / SSTL2 / SSTL3 / HSTL / LVDS / LVPECL.

When the ispClock5620A is in a LOCKED state, the LOCK output pin goes LOW. The LOCKN pins are connected to amber LED D21 and will illuminate when the LOCKN pin goes low. The lock detector has two operating modes; phase lock mode and frequency lock mode. In phase-lock mode, the LOCK signal is asserted if the phases of the reference and feedback signals match, whereas in frequency-lock mode the LOCK signal is asserted when the frequencies of the feedback and reference signals match.

U21 is controlled by SW8 or from predefined connection to U1(LatticeSC). The DIP switch controls the ispClock device. The reference clock selection and device reset is controlled using the switches. The switches control the ispClock outputs can be synchronously controlled by the SGATE output on a bank-by-bank basis or tri-stated on an output-by-output basis using the OEXb and OEYb inputs. All outputs may be tri-stated by bringing the GOEb input high.

The VCCO voltage is board connected to 2.5V or 3.3V, based on the on-board connection of FB21 or FB22.

The output clocks of U21 are routed to devices to provide system level clocking. These pre-defined board clocks are routed to input LatticeSC input clock pins for SERDES reference clocks, primary clocks, PLL inputs and DLL inputs as well as connection to an SMA (J99). This SMA is 50-ohm terminated for off-board interconnection to test equipment.

A 100.0MHz surface-mounted oscillator (Y2) is also provided and fanned-out to four general-purpose FPGA inputs.

A clock input to the ispClock device can be provided from the PCI Express Edge Fingers. This is accomplished by configuring the on-board resistor jumpers R181, R182, R183, R184 (see Appendix A, Figure 9).

SERDES

(see Appendix A, Figure 5)

SERDES Reference Clock

The 50-ohm terminated SMA connectors provide the supply reference clocks directly to the LatticeSC device from the ispClock management device. This device with drive clocks to both SERDES quads via 100-ohm LVDS signaling. On-board clock oscillators mentioned in the previous sections can be chosen to drive the same SERDES reference clocks.

SERDES Channels

Surface Mounted SMA Connections

(see Appendix A, Figure 5)

DC coupled top-mounted SMA connectors connect to the SERDES Tx and Rx channels of Quad B SERDES on the left side (PCS 361). These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

Table 6. SERDES Connectors (see Appendix A, Figure 5)

J11	B_HDINN0_L
J6	B_HDINP0_L
J20	B_HDINN1_L
J16	B_HDINP1_L
J27	B_HDINN2_L
J23	B_HDINP2_L
J31	B_HDINN3_L
J28	B_HDINP3_L

J10	B_HDOUTN0_L
J5	B_HDOUTP0_L
J19	B_HDOUTN1_L
J15	B_HDOUTP1_L
J26	B_HDOUTN2_L
J22	B_HDOUTP2_L
J30	B_HDOUTN3_L
J28	B_HDOUTP3_L

Edge Launched SMA Connections
(see Appendix A, Figure 5)

DC coupled high-performance edge-launch SMA connectors connect to the SERDES Tx and Rx channels of Quad A SERDES on the left side (PCS 360). These pins are directly coupled to the designated SMA connector, creating a path for both input and output differential data.

Table 7. SERDES Connectors (see Appendix A, Figure 5)

J12	A_HDINN0_L
J7	A_HDINP0_L
J24	A_HDINN3_L
J17	A_HDINP3_L

J13	A_HDOUTN0_L
J8	A_HDOUTP0_L
J25	A_HDOUTN3_L
J18	A_HDOUTP3_L

SERDES SMPTE Channels
(see Appendix A, Figure 5)

A single-channel 75-ohm SERDES channel is connected to BNC edge connectors. These connections are provided to connect to SMPTE video equipment. The channels include the appropriate passive components for interoperability to SMPTE devices.

Table 8. SERDES SMPTE BNC Connectors (see Appendix A, Figure 5)

J9	A_HDINN1_L
J4	A_HDINP1_L
J21	A_HDOUTN1_L
J14	A_HDOUTP1_L

SERDES PCI Express Channels
(see Appendix A, Figure 5)

This board is equipped to communicate directly as an add-on card to a PCI Express host. It is designed with edge-fingers (CN1) to fit directly into an x8 host receptacle. Power can be supplied directly from the PCI Express host via the edge-finger connections.

FPGA Test Pins
(see Appendix A, Figure 7)

General-purpose FPGA pins are available for user applications. FPGA pins are connected to switches and LEDS designated according to the following table.

Table 9. FPGA Test Pins (see Appendix A, Figure 7)

Switch	BGA	Netname
SW2D	A20	Switch1
SW2C	K22	Switch2
SW2B	K21	Switch3
SW2A	G20	Switch4
SW1D	F20	Switch5
SW1C	J22	Switch6
SW1B	H22	Switch7
SW1A	B19	Switch8

LED	BGA	NetName
D2	A19	RED1
D5	J21	YELLOW1
D7	H21	GREEN1
D9	B18	BLUE1
D3	A18	RED2
D6	H20	YELLOW2
D8	H19	GREEN2
D10	E19	BLUE2

Note: LEDs will illuminate if connected to an un-programmed FPGA pin. It is recommended that a pull-down be programmed on FPGA output pins.

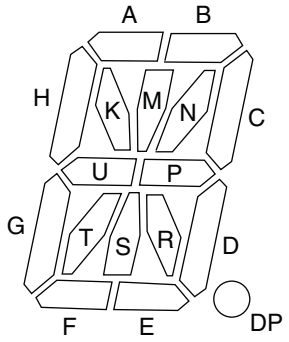
17-Segment LED Display

(see Appendix A, Figure 7)

General-purpose FPGA pins are connected to a 17-segment display according to the following table. These pins can be driven low to illuminate the display segments.

Table 10. 17-Segment LED Display

Segment	BGA
A	AC33
B	AA30
C	AD34
D	AA28
E	AA33
F	AB34
G	AA29
H	Y31
K	Y32
M	W24
N	W33
P	Y34
R	W26
S	V34
T	W25
U	U33
DP	Y27



Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit the evaluation of several FPGA I/O buffer types. The use of several termination schemes permits easy interfaces for each buffer type.

Table 11. FPGA I/O Test SMA Connectors

SMA Designation	Name	LFSC80 Signal	1152 BGA	Termination Description	Termination Resistor(s)
See Appendix A, Figure 7					
J36	LVDS_INP0	PL22A	E34	DC-Coupled	n/a
J38	LVDS_INN0	PL22B	F34	DC-Coupled	n/a
J33	LVDS_INP1	PL24A	F33	DC-Coupled	n/a
J35	LVDS_INN1	PL24B	G33	DC-Coupled	n/a
J40	LVDS_INP2	PL25A	K30	DC-Coupled	n/a
J42	LVDS_INN2	PL25B	L30	DC-Coupled	n/a
J44	LVDS_INP3	PL26A	G34	DC-Coupled	n/a
J46	LVDS_INN3	PL26B	H34	DC-Coupled	n/a
J37	LVDS_OUTP0	PL17A	F31	100-ohm Differential Termination	R114
J32	LVDS_OUTN0	PL17B	G31	100-ohm Differential Termination	
J34	LVDS_OUTP1	PL18A	D33	100-ohm Differential Termination	R116
J39	LVDS_OUTN1	PL18B	E33	100-ohm Differential Termination	
J41	LVDS_OUTP2	PL20A	F32	100-ohm Differential Termination	R117

Table 11. FPGA I/O Test SMA Connectors (Continued)

SMA Designation	Name	LFSC80 Signal	1152 BGA	Termination Description	Termination Resistor(s)
J43	LVDS_OUTN2	PL20B	G32	100-ohm Differential Termination	
J45	LVDS_OUTP3	PL21A	H30	100-ohm Differential Termination	R118
J47	LVDS_OUTN3	PL21B	J30	100-ohm Differential Termination	
See Appendix A, Figure 8					
J48	URC_PLLT	PR16A/URC_PLLC_IN_A	F5	50-ohm Ground Termination	R166
J49	URC_PLLC	PR16B/URC_PLLT_IN_A	G5	50-ohm Ground Termination	R167
J50	PCLKT3_1	PR50C	U6	50-ohm Ground Termination	R168
J51	PCLKC3_1	PR50D	V6	50-ohm Ground Termination	R169

High Speed Test Point

DP1
(see Appendix A, Figure 7)

General-purpose FPGA pins are available via a differential test pad. These connections allow a high-impedance probe to measure the performance of a coupled- differential output buffer pair.

DDR2 Memory

U18
(see Appendix A, Figure 10)

The LatticeSC Evaluation Board is equipped with an 84-BGA DDR2 SDRAM memory device such as a Micron MT47H16M16BG-3 device. The DDR2 memory interface includes a 16-bit wide device. The evaluation board includes termination of address and command signals. It includes all power and external components needed to demonstrate the memory controller of the LatticeSC device.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeSC PCI Express x8 Evaluation Board	LFSC80E-P8-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
October 2006	01.0	Initial release.
December 2006	01.1	Includes new SERDES schematic in Appendix A.
March 2007	01.2	Added Ordering Information section.
		Minor text changes to On-Board Flash Memory section.
April 2007	01.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.

Appendix A. Schematics

Figure 5.

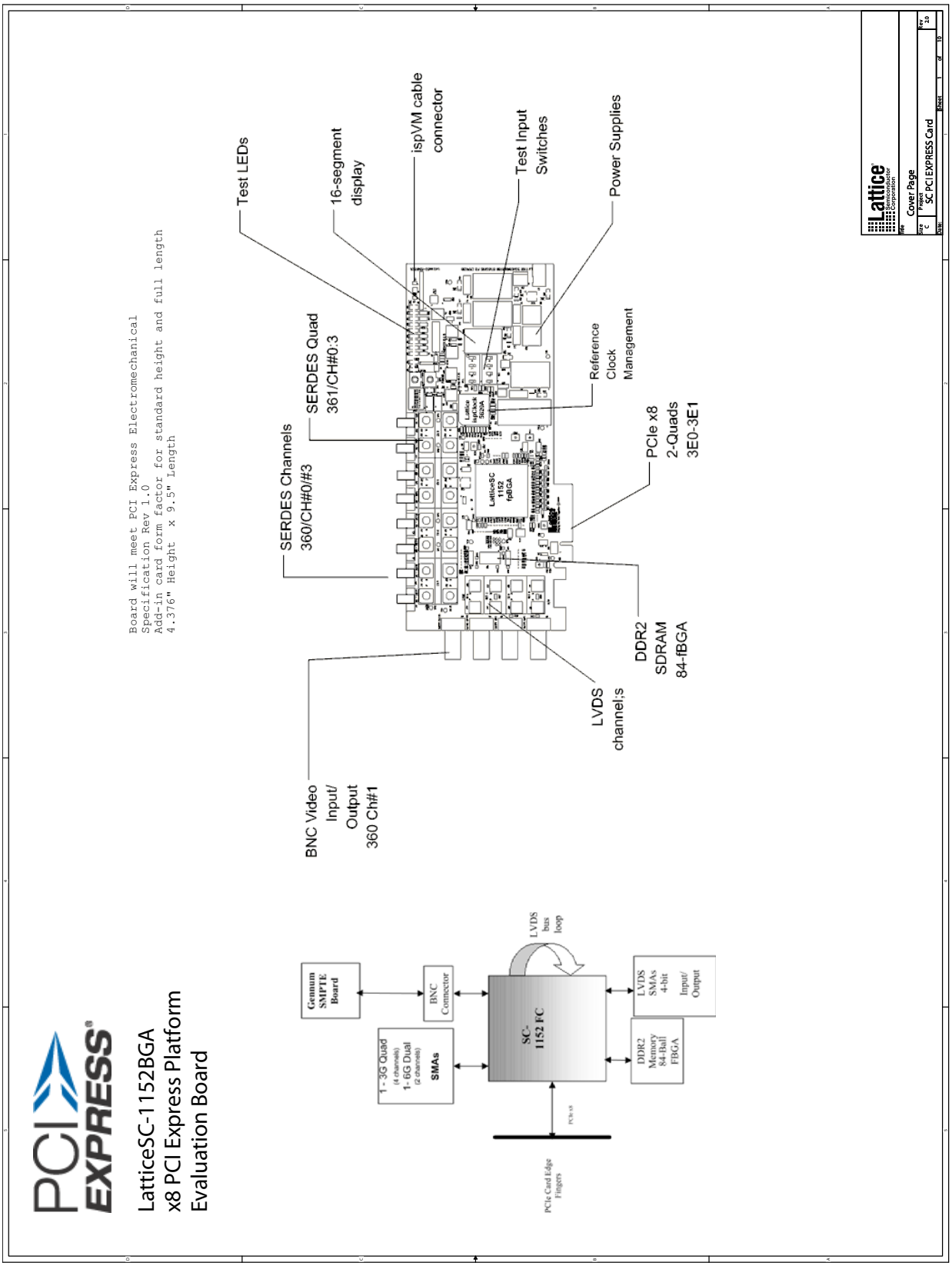


Figure 6. Configuration/Testpoints

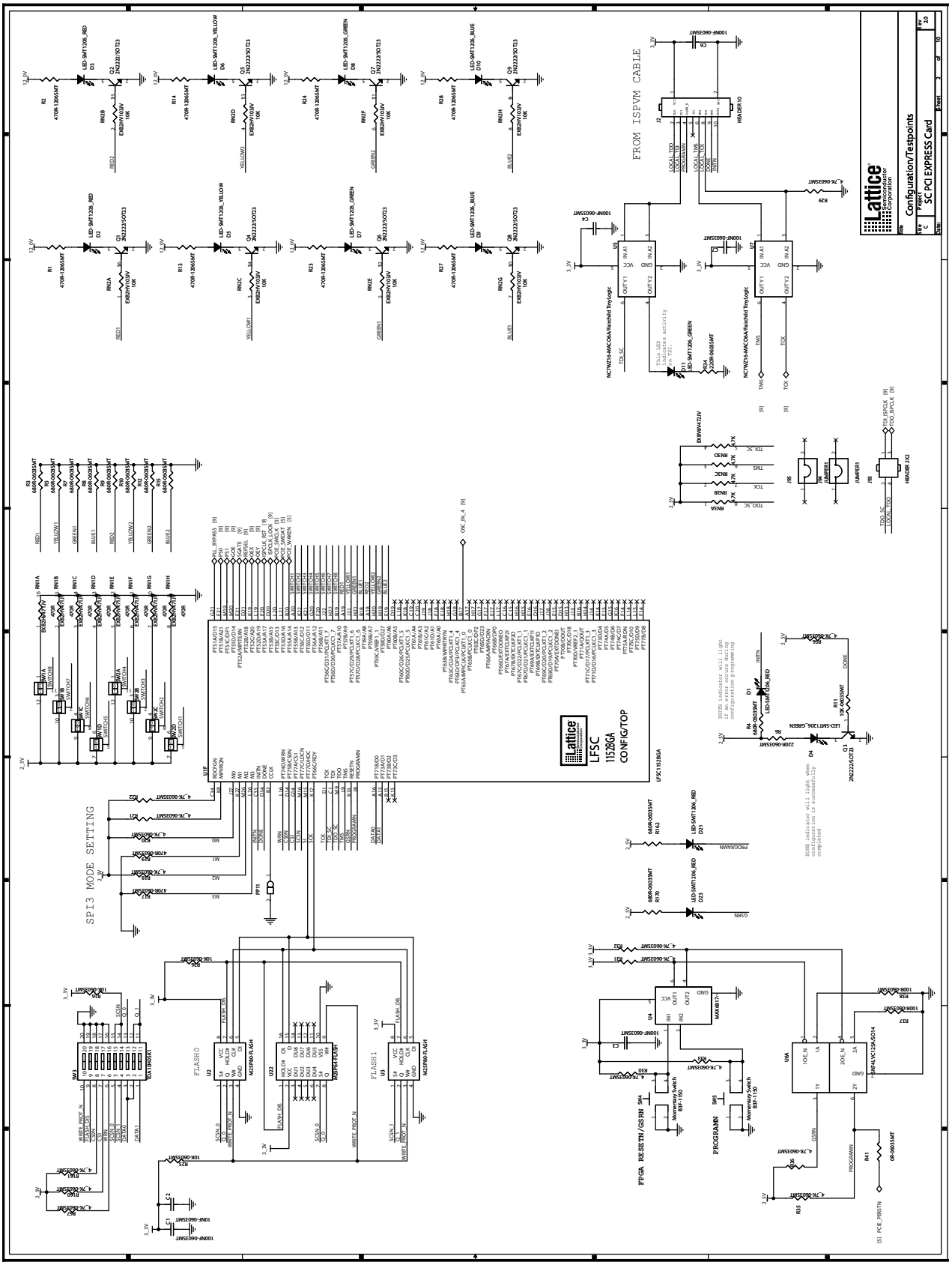


Figure 7. Power Supplies

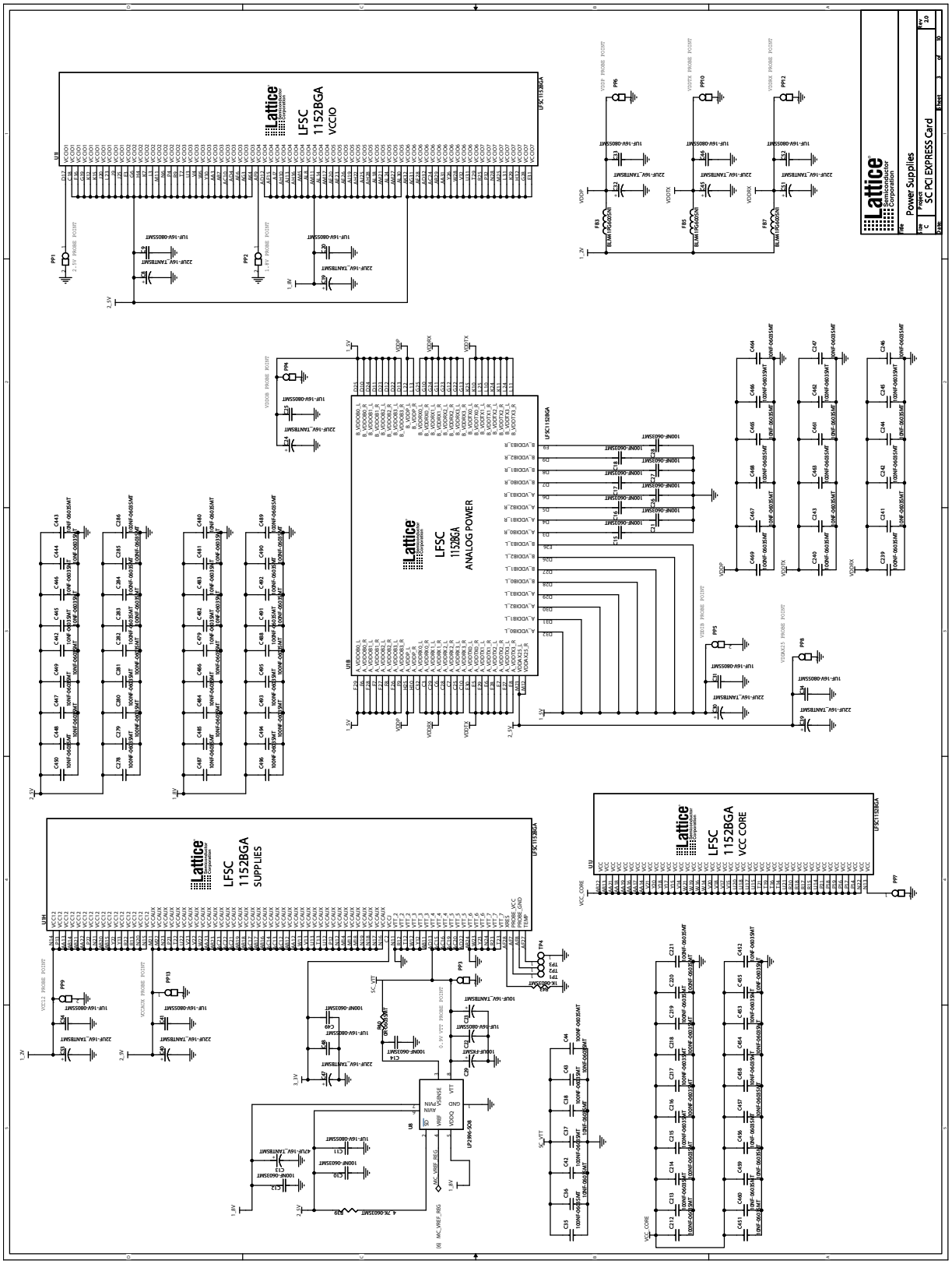


Figure 8. DC/DC Conversion

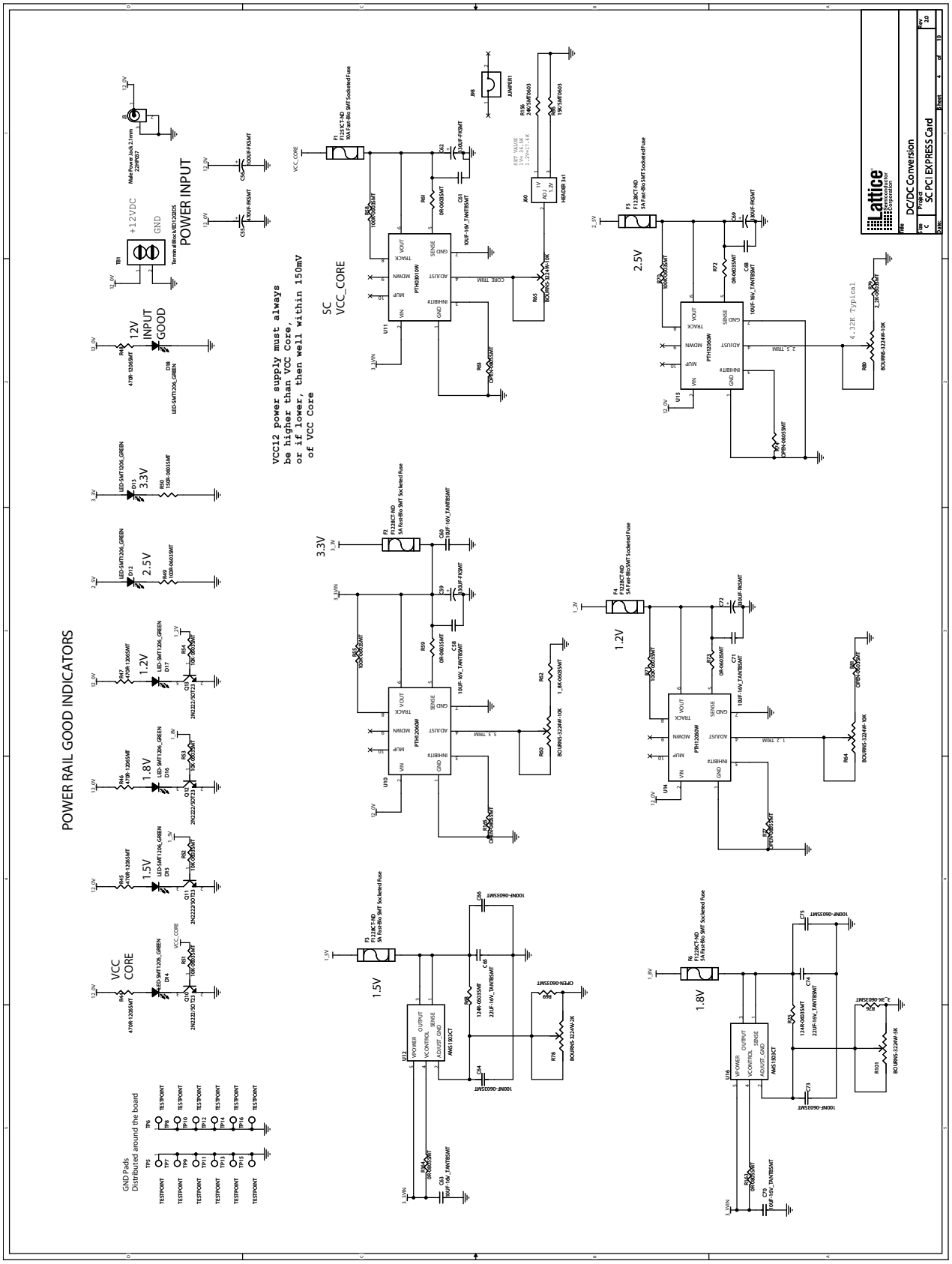


Figure 9. SERDES

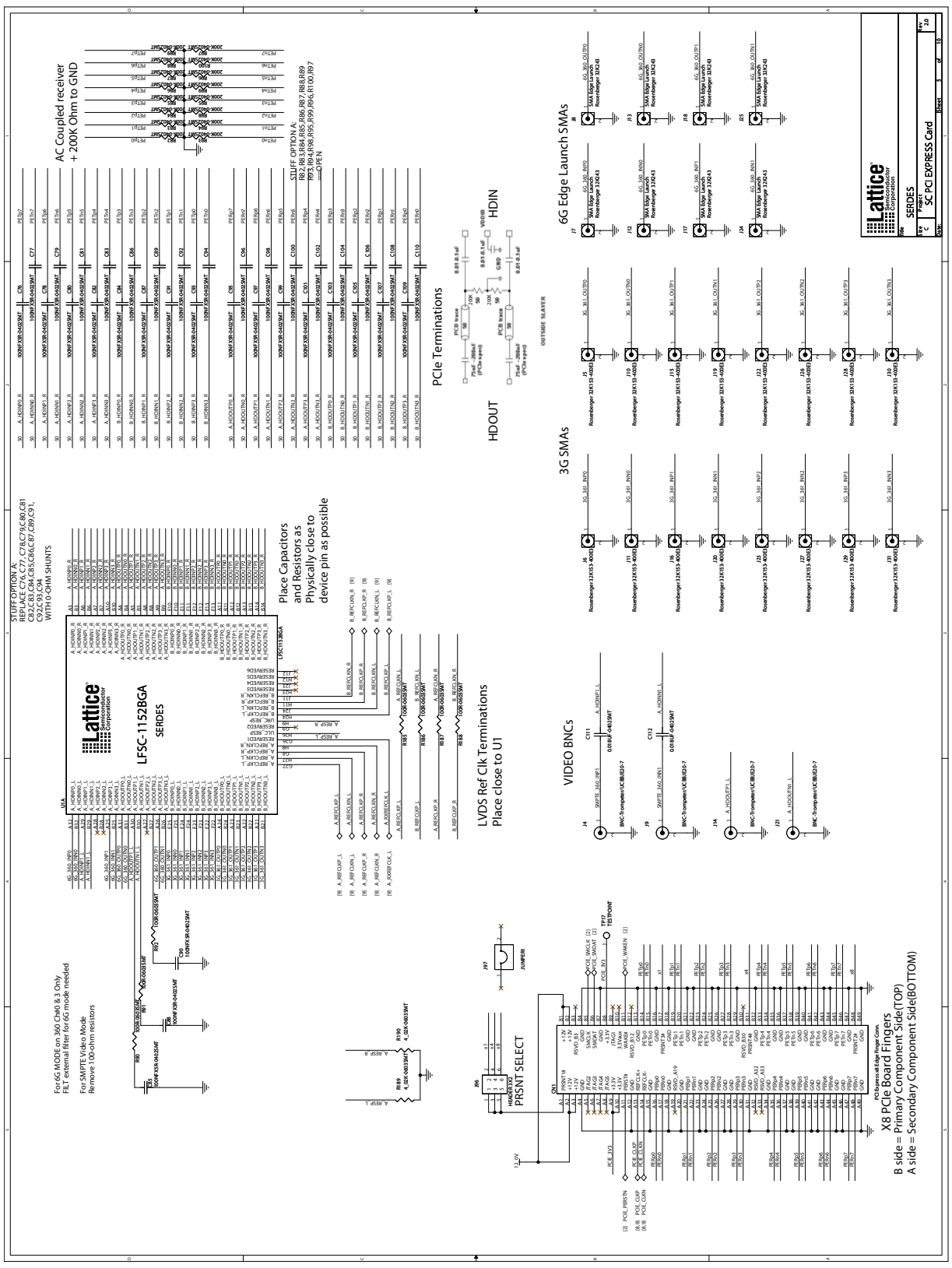


Figure 10. DDR2

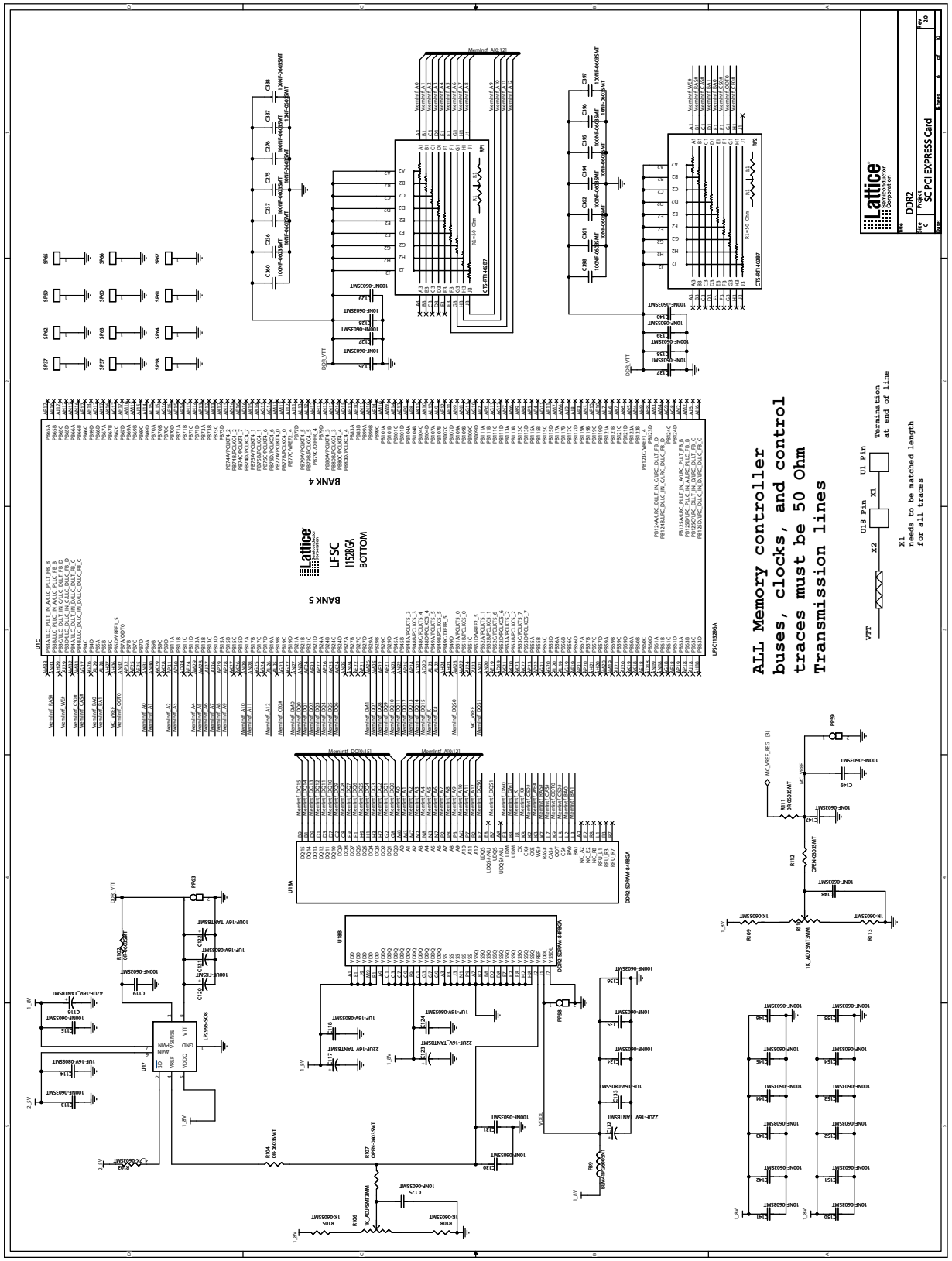


Figure 11. Differential I/O Test SMAs

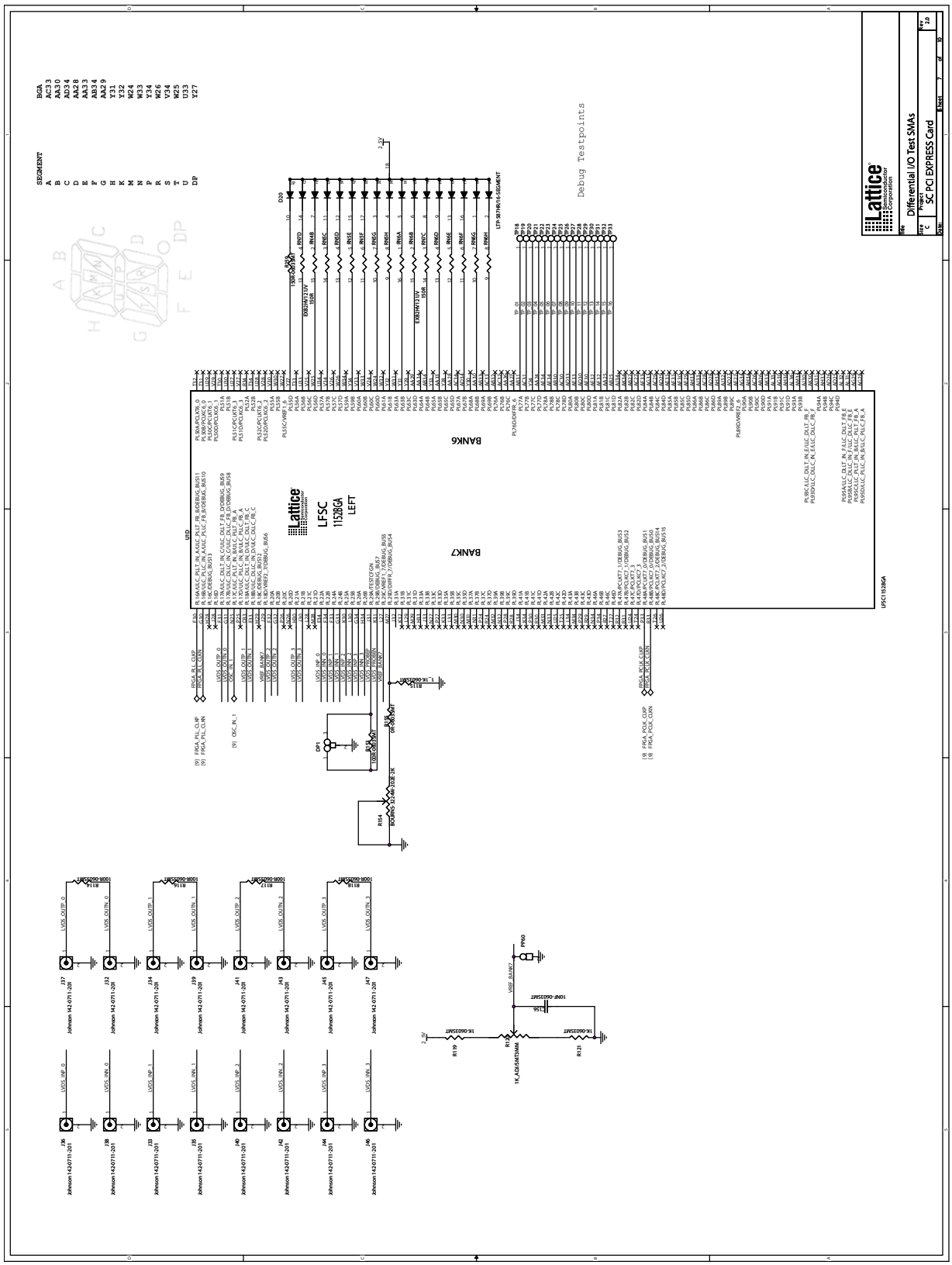


Figure 12. Differential I/O Loops

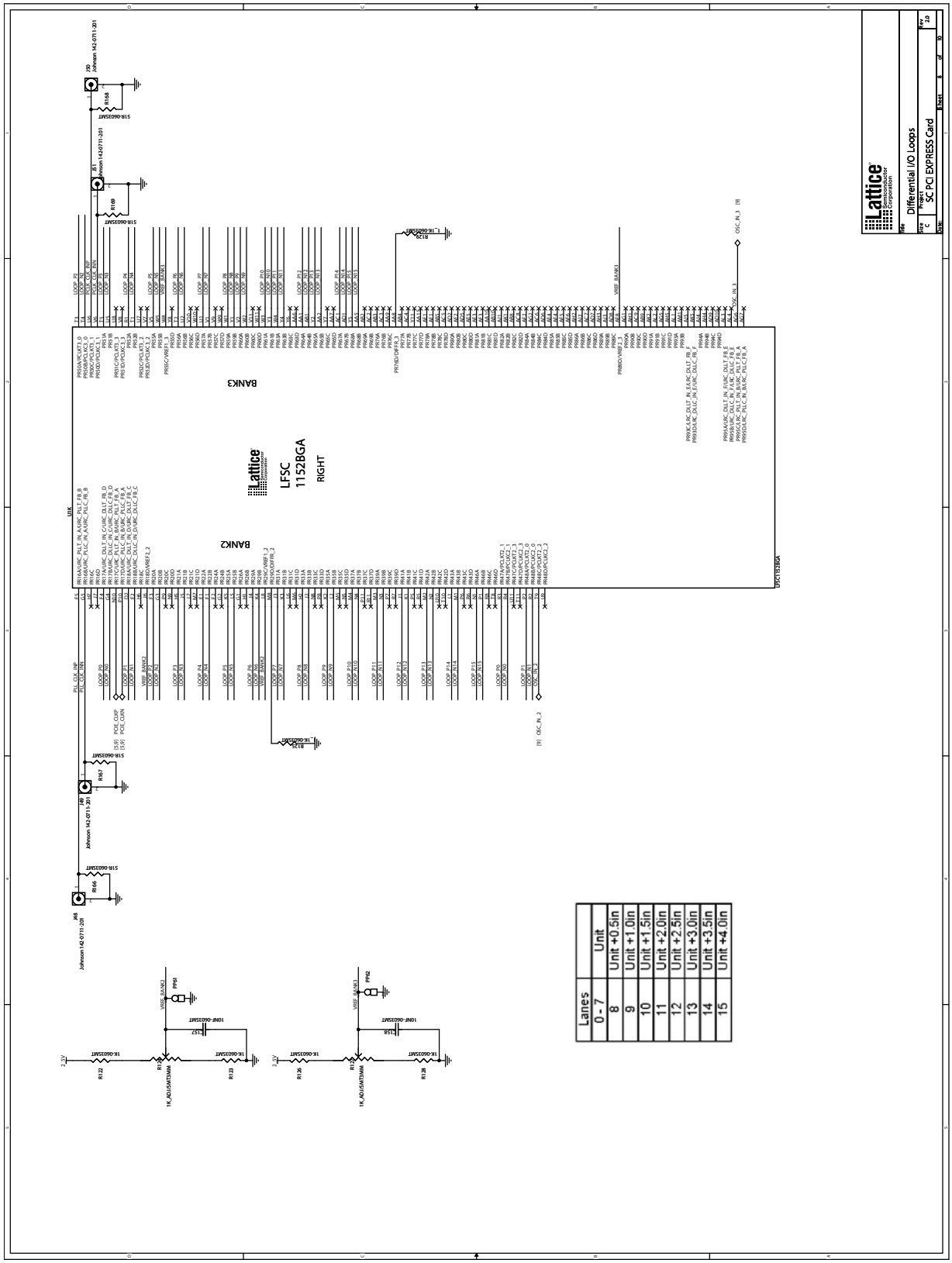


Figure 13. Clocks

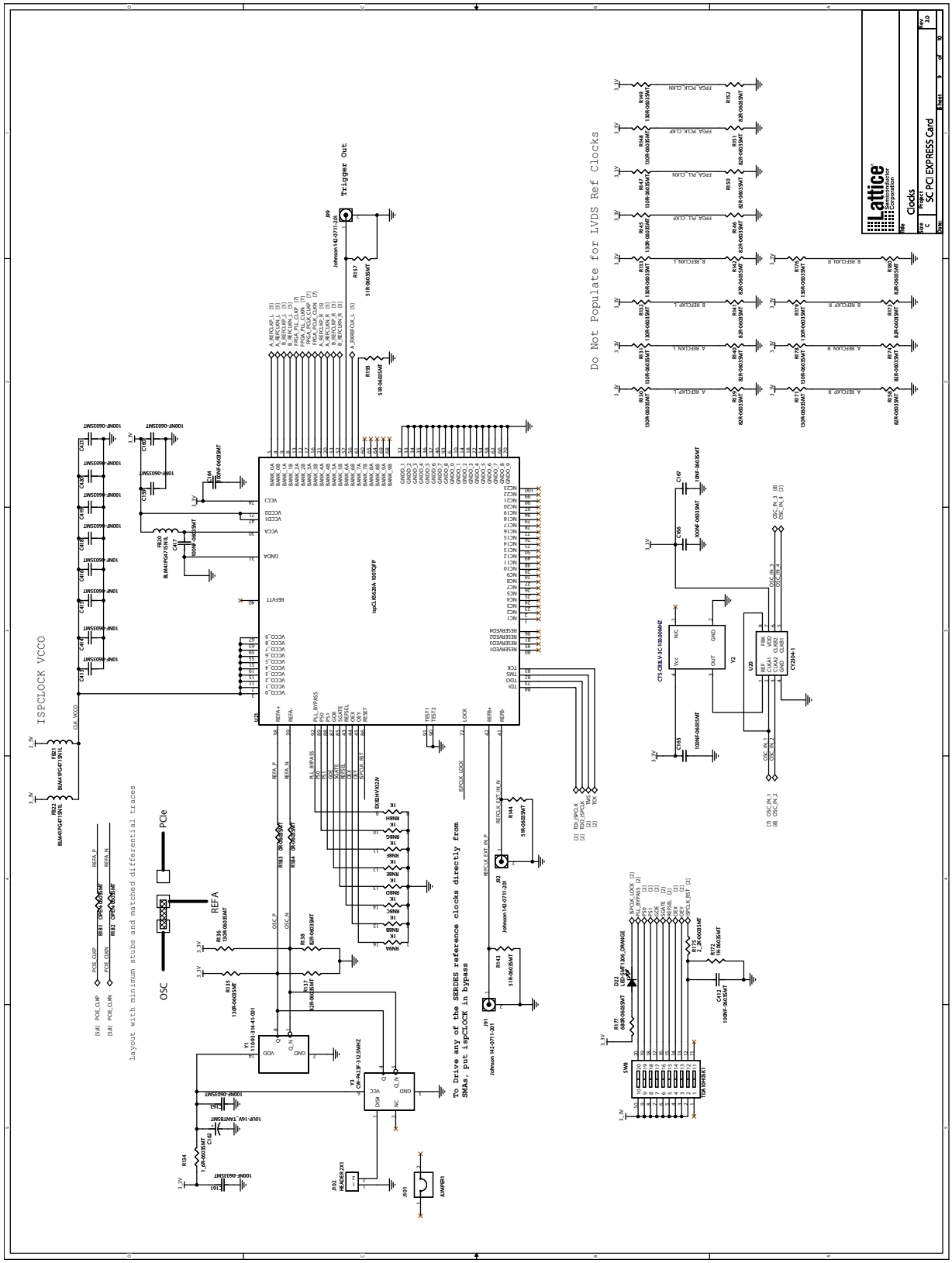


Figure 14. VSS/Decoupling