LatticeECP2™ Advanced Evaluation Board

User's Guide

January 2009
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Introduction

The LatticeECP2 Advanced Evaluation Board provides a convenient platform to evaluate, test and debug user designs and IP cores targeted to the LatticeECP2-50 device. The main features of this board are listed below:

- LatticeECP2 FPGA with a 1.2V DC core in a 672-ball fpBGA package (default LatticeECP2-50 FPGA)
- SPI Serial Flash device included for low-cost, non-volatile configuration storage
- Two 64-bit DDR2 SO-DIMM module connectors (DDR2 DIMMs are not included)
- VHDM connectors for SPI4.2 transmit and receive interfaces
- Tri-speed (10/100/1000 Mbit) Ethernet PHY that includes RJ-45, magnetics and spark gap
- Directly wired RJ-45 connector
- Samtec TFM-140-31-S-D-LC connector for interfacing with TI DSP motherboards through the peripheral interface
- RS-232 interface chip and 9-pin D-sub connector
- USB 1.1 transceiver and USB type-A and type-B connectors
- Two 8-bit DIP switches
- Discrete LEDs and 7-segment LED
- Compact Flash connector for type I and type II Compact Flash cards (Compact Flash cards not included)
- LCD module connector (LCD module not included)
- Prototyping areas with access to 103 I/O pins
- Selectable I/O bank voltages
- Four pairs of SMA connectors for high speed differential signals
- Oscillator socket for both half-size and full-size oscillators
- 3.3V, 2.5V, 1.8V, 1.2V and ADJ (adjustable voltage) powers generated from a single 5V to 28V power source
- Power Manager ispPAC®-POWR1220AT8 chip for monitoring 3.3V, 2.5V, 1.8V, 1.2V, ADJ voltages and DDR V_{REF}, V_{TT} voltages
- Interface for ispVM® System programming support

Also Included:

- 5V/3A AC adapter with international wall plugs
- ispDOWNLOAD® Cable (HW-DL-3C or equivalent)

Additional Resources

Additional resources related to the LatticeECP2 Advanced Evaluation Board (including updated documentation, and sample programs) can be found at the following URL:

www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2advancedevaluationboa.cfm.

Electrical, Mechanical, and Environmental Specifications

The nominal board dimensions are 7.5 inches by 8.5 inches. The environmental specifications are as follows:

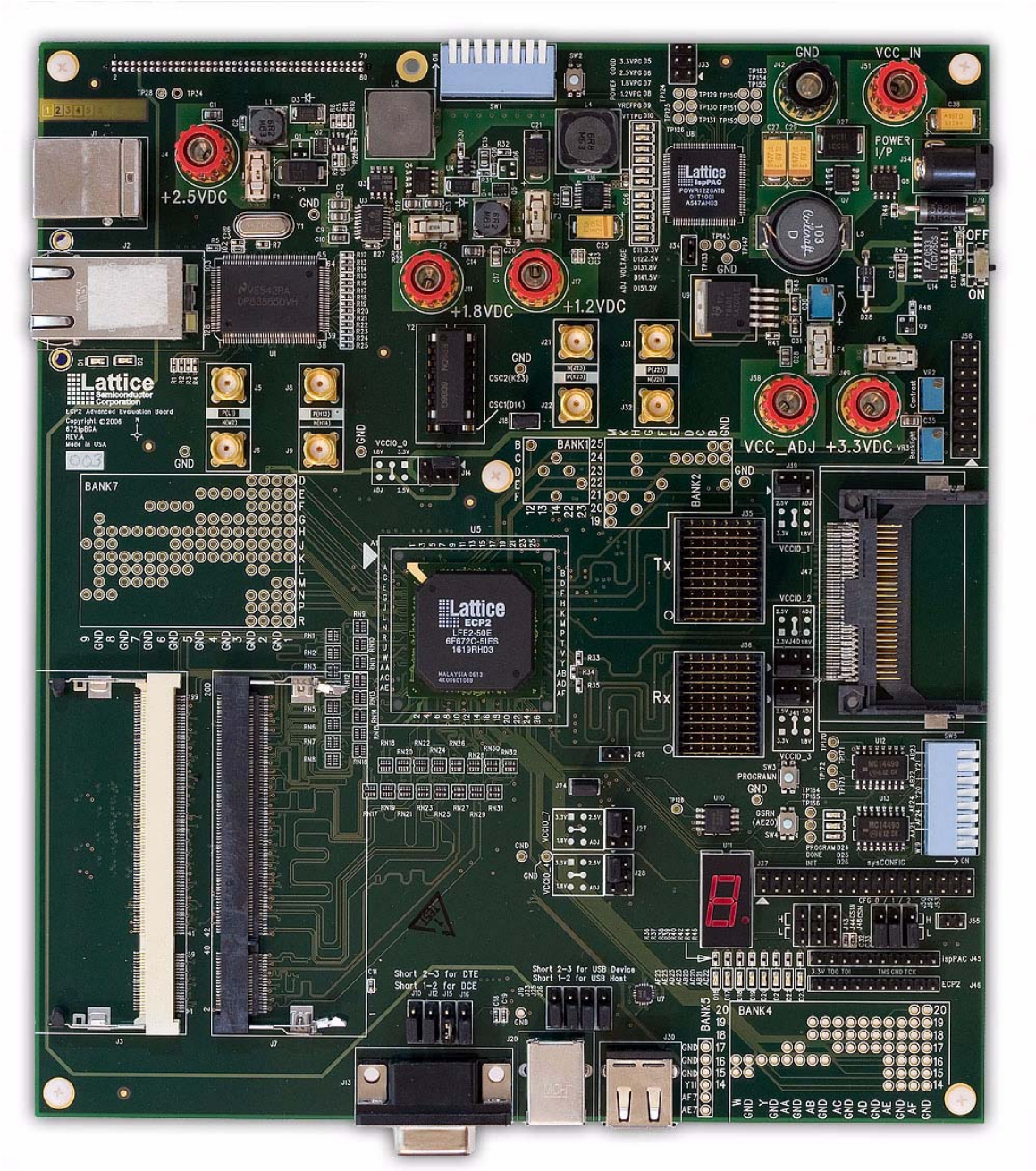
- Operating temperature: 0°C to 55°C
- Storage temperature: -40°C to 75°C

- Humidity: <95% without condensation
- 5V to 28V DC (20 watts max.)

Resources relating to the LatticeECP2 Advanced Evaluation Board can be found at:

www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2advancedevaluationboa.cfm

Figure 1. LatticeECP2 Advanced Evaluation Board



Features

LatticeECP2 Device

This board features a LatticeECP2 FPGA with a 1.2V DC core in a 672-ball fpBGA package. Any LatticeECP2 density in this package can be accommodated, though the default density is the LatticeECP2-50. A complete description of this device can be found in the LatticeECP2 Family Data Sheet on the Lattice web site at www.latticesemi.com.

General Board Functions and Settings

Other than specific functions such as LCD, CF, DDR2 or SPI4.2, the general board functions and their settings are described in this section.

Power Setup

The board is supplied by a single 5V to 28V DC power supply. On-board regulators will provide the necessary supply voltages. The on-board regulators supply 3.3V, 2.5V, 1.8V, 1.2V, and an adjustable voltage (VCC_ADJ). The adjustable voltage is set by the potentiometer VR1 and can be set to a value between 1.22V and 3.25V. The DC power may be applied through the power jack at J54 using an AC adapter with a 5V to 28V DC output range. Requirements for the power jack are listed in Table 1. Other than using the AC adapter, the DC power may also be applied using a workbench power supply through the banana jacks at J51 (VCC_IN) and J42 (GND). The workbench power supply voltage has to be between 5V and 28V.

Table 1. Power Jack J54 Specifications

Polarity	Positive Center
Inside Diameter	0.1" (2.5mm)
Outside Diameter	0.218" (5.5mm)
Current Capacity	Up to 4A

Power may also be supplied directly for each individual supply rail using banana jack connectors. To enable this mode of operation, the appropriate fuses must be removed. All power sources must be regulated to the specifications in Table 2. No special power sequencing is required for the evaluation board.

Table 2. Individual Control of Supplies

Supply	Jack	Fuse	Requirement
3.3V	J49	F5 (3.0A)	+/- 5%
2.5V	J4	F1 (3.0A)	+/- 5%
1.8V	J11	F2 (10.0A)	+/- 5%
1.2V	J17	F3 (3.0A)	+/- 5%
VCC_ADJ	J38	F4 (1.5A)	User-defined

Power Voltage Monitoring

Lattice's ispPAC Power Manager II device, the ispPAC-POWR1220AT8, is used for monitoring various voltages on the board. There are six LEDs used to indicate the status of the monitoring voltages. If the monitoring voltage is not in the +/- 5% voltage window, the corresponding LED will flash; otherwise, the LED will stay ON. Table 3 shows these six voltages and the corresponding LEDs.

Table 3. Individual Monitoring of Six Power Voltages

Voltage	LED	Monitoring Voltage Range
3.3V	D5	3.3V +/- 5%
2.5V	D6	2.5V +/- 5%
1.8V	D7	1.8V +/- 5%
1.2V	D8	1.2V +/- 5%
V_{REF}	D9	0.9V +/- 5%
V_{TT}	D10	0.9V +/- 5%

For the VCC_ADJ adjustable voltage, the ispPAC-POWR1220AT8 will detect the voltage rail and show the status using five LEDs. Each of these five LEDs indicates a particular voltage range. If the VCC_ADJ is in one of the voltage ranges, the corresponding LED will be turned ON and the other LEDs will be turned OFF; otherwise, these five LEDs will be turned ON and then OFF sequentially so that you will see a light moving between the LEDs. The five LEDs and corresponding voltages are listed in Table 4.

Table 4. Monitoring of VCC_ADJ Power Voltages

LED	Indicating Voltage Range
D11	3.3V +/- 5%
D12	2.5V +/- 5%
D13	1.8V +/- 5%
D14	1.5V +/- 5%
D15	1.2V +/- 5%

LatticeECP2 I/O Bank Voltage Setting

The jumpers listed in Table 5 allow the user to select the voltage (V_{CCIO}) applied to each of the eight I/O banks of the LatticeECP2 device. Certain restrictions apply depending on which features of the board are being used.

Table 5. V_{CCIO} Selection Jumper

sysIO™ Bank	Jumper	Jumper on Pins
0	J14	1-3 -> VCC_3.3V 2-4 -> VCC_2.5V 3-5 -> VCC_1.8V 4-6 -> VCC_ADJ
1	J39	
2	J40	
3	J41	
4	J28	
7	J27	
5	NA	Tied to 1.8V (Cannot be changed)
6		

Depending on the optional devices installed, some sysIO banks may have restrictions. For J14, J27, J28, J39, J40, and J41, select only one bank voltage position at that jumper. For example, attaching more than one jumper to J14's six square pins will short supplies.

Table 6. sysIO Bank Considerations

Bank	Setting
0	2.5V if Ethernet interface used. 3.3V if TI peripheral interface used.
1	3.3V if LCD, Compact Flash or on-board oscillator used.
2	2.5V if SPI4.2 interface used.
3	2.5V if SPI4.2 interface used.
4	3.3V if USB or RS-232 interfaces used.
5	Tied to 1.8V (cannot be changed).
6	
7	Any

The following tables detail the various I/O standards supported by the LatticeECP2 sysIO structures. More information can be found in TN1102, LatticeECP2 sysIO Usage Guide.

Table 7. Mixed Voltage I/O Support

	Input sysIO Standards					Output sysIO Standards				
V_{CCIO}	1.2V	1.5V	1.8V	2.5V	3.3V	1.2V	1.5V	1.8V	2.5V	3.3V
1.2V	Yes			Yes	Yes	Yes				
1.5V	Yes	Yes		Yes	Yes		Yes			
1.8V	Yes		Yes	Yes	Yes			Yes		
2.5V	Yes			Yes	Yes				Yes	
3.3V	Yes			Yes	Yes					Yes

For example, if V_{CCIO} is 3.3V, signals from devices powered by 1.2V, 2.5V, or 3.3V can be input and the thresholds will be correct, assuming the user has selected the desired input level using ispLEVER® software. Output levels are tied directly to V_{CCIO}.

Table 8. sysIO Standards Supported per Bank

Description	Top Side Banks 0-1	Right Side Banks 2-3	Bottom Side Banks 4-5	Left Side Banks 6-7
I/O Buffers	Single-ended	Single-ended and Differential	Single-ended	Single-ended and Differential
Output Standards Supported	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18_I, II SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I, II SSTL25 Class I, II SSTL33 Class I, II HSTL15 Class I HSTL18 Class I, II SSTL18D Class I, II SSTL25D Class I, II SSTL33D Class I, II HSTL15D Class I, II HSTL18D Class I, II LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I HSTL18 Class I, II SSTL18D Class I, II SSTL25D Class I, II, SSTL33D Class I, II HSTL15D Class I HSTL18D Class I, II PCI33 LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]	LVTTL LVCMOS33 LVCMOS25 LVCMOS18 LVCMOS15 LVCMOS12 SSTL18 Class I SSTL2 Class I, II SSTL3 Class I, II HSTL15 Class I, III HSTL18 Class I, II, III SSTL18D Class I, SSTL25D Class I, II, SSTL33D_I, II HSTL15D Class I HSTL18D Class I, II LVDS LVDS25E[1] LVPECL[1] BLVDS[1] RSDS[1]
Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
Clock Inputs	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential	All Single-ended, Differential
PCI Support	PCI33 without clamp	PCI33 without clamp	PCI33 with clamp	PCI33 without clamp PCI33 with clamp (ECP2M)
LVDS Output Buffers		LVDS (3.5mA) Buffers[2]		LVDS (3.5mA) Buffers[2]

1. These differential standards are implemented by using a complementary LVCMOS driver with external resistor pack.
2. Available only on 50% of the I/Os in the bank.

Prototype Areas

For general purpose I/O testing or monitoring, numerous test points are provided for direct access. The test points are grouped together and arranged in a grid pattern according to their associated I/O bank and are labeled with the associated pin locations on the silkscreen of the board. For bank 4 and bank 7, each test point also comes with an adjacent GND via.

Differential Signal Connections

There are four pairs of SMA connectors and one RJ-45 connector connected directly to the LatticeECP2 differential I/O pairs.

The eight SMA connectors are provided for clocks or general purpose, user-definable signals. The center pin is wired to an I/O pin and the outer case is soldered to ground. Table 9 details to which I/O pin each SMA connector is wired.

Table 9. SMA Connectors

Location	I/O Ball	Polarity	SysIO Bank	Description
J5	L1	Pair#0 P	7	PL25A / LUM0_SPLLT_IN_A
J6	M2	Pair#0 N	7	PL25B / LUM0_SPLLC_IN_A
J22*	K23*	Pair#1 P	2	RUM0_SPLLT_IN_A / PR25A
J21	J23	Pair#1 N	2	RUM0_SPLLC_IN_A / PR25B
J31	J25	Pair#2 P	2	RUM0_SPLLT_IN_A / PR26A
J32	J26	Pair#2 N	2	RUM0_SPLLC_IN_A / PR26B
J8	H13	Pair#3 P	0	PCLKT0_0 / PT46A
J9	H14	Pair#3 N	0	PCLKC0_0 / PT46B

Note: The SMA connector on J22 is shared with the on-board oscillator. When this SMA connector is used, the jumper on J18 must be removed.

RJ-45 Connectors

There are two RJ-45 connectors, J1 and J2, on the evaluation board. J1 is a simple RJ-45 female connector provided for general-purpose interfacing to the LatticeECP2 device. J2 is a full-featured Ethernet PHY connection with internal magnetics and spark gap. The connections for J1 are listed in Table 10. J2 is described in more detail in the Ethernet section later in this user's guide.

Table 10. J1 RJ-45 Connections

J1 Pin	I/O Ball	Polarity	sysIO Bank	Description
1	J19	Pair#0 P	2	PR13A
2	K19	Pair#0 N	2	PR13B
3	H22	Pair#1 P	2	PR15A
6	J22	Pair#1 N	2	PR15B
4	L19	Pair#2 P	2	PR17A
5	K20	Pair#2 N	2	PR17B
7	G25	Pair#3 P	2	PR19A
8	G26	Pair#3 N	2	PR19B

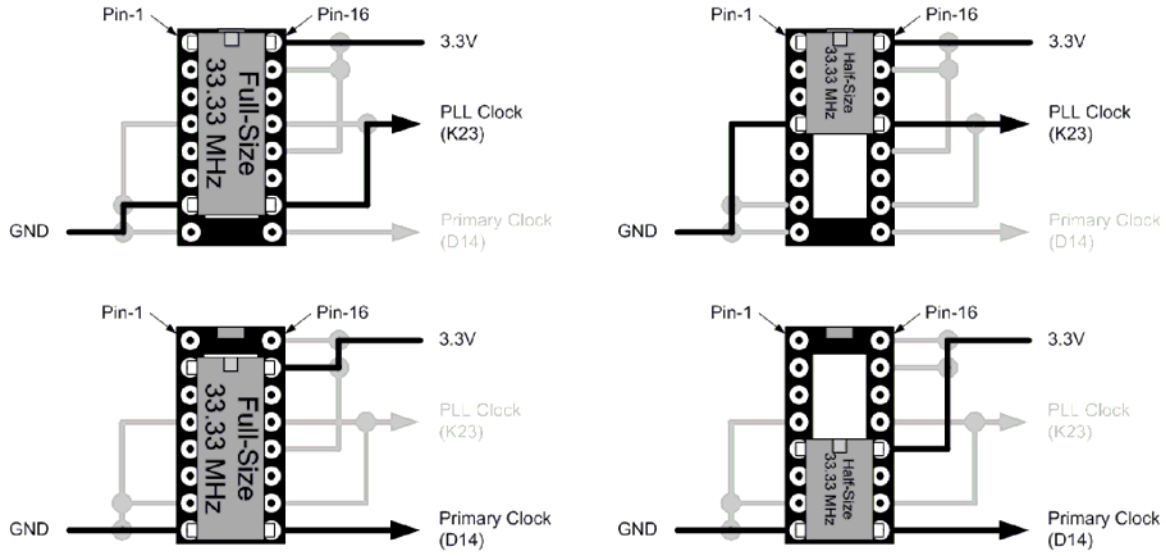
Oscillator

The 3.3V oscillator socket (Y2) accepts both full-size and half-size oscillators and can route to different clock inputs, depending on its position within the socket, see Figure 2. The board is shipped with an EPSON programmable oscillator programmed to 33.33MHz.

The 16-pin socket will allow connection to PLL clock pin K23 when the top of the oscillator is aligned to socket pins 1 and 16. Note that the SMA connector on J22 is shared with the on-board oscillator. When installing the oscillator, connect the clock to PLL clock pin K23. The SMA connector on J22 cannot be used and the jumper on J18 needs to be installed.

When the bottom of the oscillator is aligned to socket pins 8 and 9, the clock is provided to primary clock pin D14.

Figure 2. On-board Oscillator



SPI Serial Flash

SPI Serial Flash are available in three package styles. The device included on this board is an 8-pin, 16 Mbit SPI Flash, sufficient to store two bitstreams simultaneously in order to support SPIm mode.

Configuration/Programming Headers

Two programming headers are provided on the evaluation board, providing access to the LatticeECP2 JTAG port and sysCONFIG™ port. The JTAG connector is a 1x10 header and the sysCONFIG connector is a 2x17 header. The JTAG port also provides loop-through connectors to allow for easy daisy chaining of multiple boards. With proper jumper selection (see next section) standard IDC ribbon cable can be used without the need to swap any wires on the cable.

The pinouts for these headers are provided in the following tables.

Note: A parallel port ispDOWNLOAD® cable is included with each LatticeECP2 Advanced board. When using a parallel port (1x8) ispDOWNLOAD cable, connect pin 1 of the cable to pin 1 of the 1x10 JTAG header.

LatticeECP2 Configuration

Two programming headers, J45 and J46, are provided on the evaluation board, providing access to the LatticeECP2 JTAG port and the ispPAC-POWR1220AT8 JTAG port. The pinouts for the headers are provided in Table 11.

Table 11. JTAG Programming Headers

Pin	Jumper on J34 (None on J55)		Jumper on J55 (None on J34)	
	J45 Function	**J46 Function**	**J45 Function**	**J46 Function**
1	V_{CC} (3.3V)	V_{CC} (3.3V)	V_{CC} (3.3V)	Not used
2	TDO of ispPAC-POWR1220AT8	TDO of LatticeECP2	TDO of ispPAC-POWR1220AT8	Not used
3	TDI of ispPAC-POWR1220AT8	TDI of LatticeECP2	TDI of LatticeECP2	Not used
4	NC	NC	NC	Not used
5	NC	NC	NC	Not used
6	TMS of both chips	TMS of both chips	TMS of both chips	Not used
7	GND	GND	GND	Not used
8	TCK of ispPAC-POWR1220AT8	TCK of LatticeECP2	TCK of both chips	Not used
9	NC	DONE of LatticeECP2	NC	Not used
10	NC	INITN of LatticeECP2	NC	Not used

J34 and J55 control the functions of the two programming headers. When a jumper is installed on J34, the programming header J45 is connected to the JTAG port of the ispPAC-POWR1220AT8 and is used for programming the ispPAC-POWR1220AT8 only; the programming header J46 is connected to the JTAG port of LatticeECP2 and used for programming the LatticeECP2 only.

When the jumper is moved from J34 to J55, the JTAG ports of the LatticeECP2 and ispPAC-POWR1220AT8 are chained together. In this case, the programming header J45 is connected to the JTAG port of the LatticeECP2 first and then chained with the JTAG port of ispPAC-POWR1220AT8. The programming header J46 should not be used when the JTAG ports are chained together.

Table 12. sysCONFIG Header Pinout (J37)

Function	Pin		Function
CCLK	1	2	Ground
BUSY / SISPI	3	4	D6
DI/D0[1]	5	6	VCC_3.3V
D7 / DOUT[1]	7	8	INITN
DONE	9	10	PROGRAMN
D7	11	12	Ground
D6	13	14	Ground
D5	15	16	Ground
D4	17	18	Ground
D3	19	20	Ground
D2	21	22	Ground
D1	23	24	Ground
D0	25	26	Ground
CSN[1]	27	28	WRITEN
CS1N[1]	29	30	CFG0
VCC_3.3V	31	32	CFG1
Ground	33	34	CFG2

1. See section below on jumpers

Switches

The board includes three push-button switches and two 8-bit switches for implementing basic static input functions.

Switches 2, 3 and 4 (SW2, SW3 and SW4) are momentary switches. The pull-up resistors associated with these switches are wired to 3.3V. Pushing the switches down produces a low (0), otherwise it produces a high (1). The signals controlled by SW3 and SW4 are debounced by MC14490 (U12) before connecting to an LatticeECP2 I/O pin. Table 13 shows the control relationship between the switches, LatticeECP2 and ispPAC-POWR1220AT8 I/O pins.

Table 13. Momentary Switches

	SW4	SW3	SW2[1]
Connection	**AE20 of LatticeECP2**	**V19 of LatticeECP2 (PROGRAMN)**	**Pin 97 of ispPAC-POWR1220AT8[1]**
User-definable	Yes	No	Yes[1]
Debounced	Yes	Yes	No

1. SW2 signal is also connected (wire-AND) to position#1 of SW1. Therefore, when position#1 of SW1 is in the down position, the SW2 signal (ispPAC-POWR1220AT8 pin 97) will be low even when SW2 is not being pushed.

Switch 1 and 5 (SW1 and SW5) on the right side and the upper side of the board are 8-pin DIP switches. The pull-up resistors associated with these switches are wired to 3.3V. A switch in the down position produces a low (0), the up position produces a high (1). Same as SW3 and SW4, all signals of SW5 are debounced before connecting to LatticeECP2 I/O pins. Table 14 shows the SW5 connections to the LatticeECP2 and Table 15 shows the SW1 connections to the ispPAC-POWR1220AT8 I/O pins.

Table 14. 8-Position Switch SW5

Switch (Position#)	LatticeECP2 I/O Ball	sysIO Bank
SW5 (position#1)	W19	4
SW5 (position#2)	AA21	4
SW5 (position#3)	AF24	4
SW5 (position#4)	AE24	4
SW5 (position#5)	Y20	4
SW5 (position#6)	AB22	4
SW5 (position#7)	Y21	4
SW5 (position#8)	AB23	4

Table 15. 8-Position Switch SW1

Switch (Position#)	ispPAC-POWR1220AT8 I/O Pin	Pin Name
SW1 (position#1)	97	IN1
SW1 (position#2)	1	IN2
SW1 (position#3)	2	IN3
SW1 (position#4)	4	IN4
SW1 (position#5)	6	IN5
SW1 (position#6)	7	IN6
SW1 (position#7)	89	VPS0
SW1 (position#8)	90	VPS1

LEDs

Eight user-definable LEDs are provided on the lower right side of the board. These LEDs are each wired to a separate general purpose I/O as defined in Table 16. The current limiting resistors associated with these LEDs are wired to 2.5V, but it is safe to use any FPGA I/O voltage. The LED will light when its associated I/O pin is driven low.

Table 16. Connection between LEDs and LatticeECP2

LED	LatticeECP2 I/O Ball	Bank	LED	LatticeECP2 I/O Ball	Bank
D16	AF23	4	D20	AB20	4
D17	AE23	4	D21	AC20	4
D18	AD23	4	D22	AB21	4
D19	AC23	4	D23	AC22	4

Table 17 describes the three LEDs associated with the dedicated programming pins.

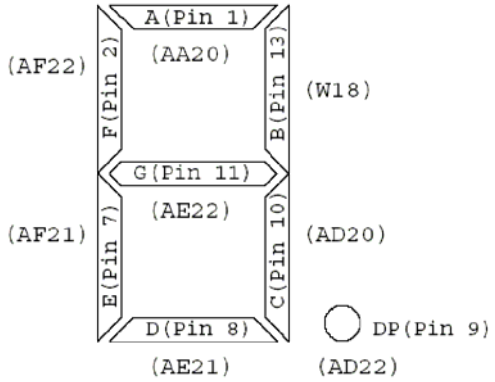
Table 17. Programming LEDs

LED	Pin	Color	Function
D24	PROGRAMN	Yellow	On when signal is low
D26	INIT	Red	On when initializing
D25	DONE	Green	On when configuration is complete

7-Segment Display

The 7-segment LED located near the eight LEDs is controlled by the LatticeECP2 bank 4 I/O pins. The connections of the segments are shown in Figure 3.

Figure 3. 7-Segment Display



LCD Module Connector (LCD Module Not Included)

The LCD module connector (J56) is a 2x9 header. This 18-pin header is compatible with quite a few character LCD modules. Table 18 shows the pin function of the header and the connections to bank 1 of the LatticeECP2 FPGA.

Table 18. LCD Header Connection

Pin #	Function	LatticeECP2 I/O Ball	Pin #	Function	LatticeECP2 I/O Ball
1	Anode	—	2	Cathode (GND)	—
3	VSS (GND)	—	4	VDD(5V)	—
5	VO	—	6	RS	B13
7	R/W	A12	8	E	A13
9	DB0	E14	10	DB1	A15
11	DB2	G14	12	DB3	C15
13	DB4	H15	14	DB5	F15
15	DB6	H17	16	DB7	D15
17	Anode	—	18	Cathode (GND)	—

The VR3 potentiometer is used to limit the current that flows through the backlight LED on the LCD module. The VR2 potentiometer is used to adjust the VO voltage that controls the LCD contrast.

When the following LCD modules are used, connect pin 1 to 16 to the backlight LCD module or connect pin 1 to 14 to the non-backlight LCD module.

- Optrex
  - C-51505 Series: 20 characters x 2 lines

When the following LCD modules are used, connect pin 3 to 18 to the backlight LCD module or connect pin 3 to 16 to the non-backlight LCD module.

- Lumex
  - LCM-S01601 Series: 16 characters x 1 line
  - LCM-S00802 Series: 8 characters x 2 lines
  - LCM-S01602 Series: 16 characters x 2 lines
  - LCM-S02002 Series: 20 characters x 2 lines
  - LCM-S02402 Series: 24 characters x 2 lines
  - LCM-S04002 Series: 40 characters x 2 lines
  - LCM-S02004 Series: 20 characters x 4 lines
  - LCM-S02404 Series: 24 characters x 4 lines

- Varitronix
  - MDLS-20189 Series: 20 characters x 1 line
  - MDLS-20265 Series: 20 characters x 2 lines
  - MDLS-24265 Series: 24 characters x 2 lines
  - MDLS-40266 Series: 40 characters x 2 lines

CompactFlash

The CompactFlash connector (J47) on the board accepts both type-I and type-II CompactFlash cards. The connections between the connector pins and the LatticeECP2 I/Os are shown in Table 19. All the pins are connected to bank 1 I/Os.

Table 19. CompactFlash Connection

Pin #	Function	LatticeECP2 I/O	Pin #	Function	LatticeECP2 I/O
1	GND	—	26	CD1	G17
2	D3	B15	27	D11	B19
3	D4	A16	28	D12	D19
4	D5	G15	29	D13	B20
5	D6	E15	30	D14	B21
6	D7	D17	31	D15	C19
7	CE1/CS0	C17	32	CE2/CS1	E19
8	A10	B16	33	VS1	A21
9	OE/ATASEL	C18	34	IORD	A22
10	A9	B17	35	IOWR	D20
11	A8	A17	36	WE	C20
12	A7	H18	37	READY/IREQ/INTRQ	B23
13	VCC	—	38	VCC	—
14	A6	F16	39	CSEL	B22
15	A5	G16	40	VS2	E20
16	A4	E16	41	RESET	C22
17	A3	A18	42	WAIT/IORDY	F19
18	A2	B18	43	INPACK/DMARQ	E21
19	A1	D18	44	REG/DMACK	A23
20	A0	E17	45	BVD2/SPKR/DASP	A24
21	D0	A19	46	BVD1/STSCHG/PDIAG	H19
22	D1	A20	47	D8	F20
23	D2	F17	48	D9	J18
24	WP/IOIS16/IOCS16	G19	49	D10	G20
25	CD2	E18	50	GND	—

USB 1.1

To implement the USB interface, the board contains a USB 1.1 transceiver MAX3454EETE (or NCN2500MNR2 from On Semiconductor), a type-A connector and a type-B USB connector.

Table 20. Header Settings for Configuring USB Interface as USB Host

Header/Connector	Jumper Position	Description
J26	Pin 1 and 2	Drive USB transceiver ENUM pin to GND to disconnect the internal 1.5K resistor between Vtrm and D+ or D-.
J25 (D+)	Pin 1 and 2	Pull D+ signal low through an external 15K resistor.
J23 (D-)	Pin 1 and 2	Pull D- signal low through an external 15K resistor.
J19	Pin 1 and 2	Provide 5V power to the external USB device.
J30 (USB type A)	—	Type A is used while implementing USB host.
J20 (USB type B)	—	This connector is not used in this configuration.

Table 21. Header Settings for Configuring USB Interface as a USB Device

Header/Connector	Jumper Position	Description
J26	Pin 2 and 3	Drive USB transceiver ENUM pin to 3.3V to connect the internal 1.5K resistor between Vtrm and D+ or D-.
J25 (D+)	Pin 2 and 3	Disconnect D+ signal from the external 15K pull-down.
J23 (D-)	Pin 2 and 3	Disconnect D- signal from the external 15K pull-down.
J19	Pin 2 and 3	No 5V power is provided when implementing USB device.
J30 (USB type A)	—	This connector is not used in this configuration.
J20 (USB type B)	—	Type A is used while implementing USB host.

The connections between the USB 1.1 transceiver MAX3454EETE (or NCN2500MNR2 from On Semiconductor) and the LatticeECP2 I/O are shown in Table 22.

Table 22. Connections Between USB 1.1 Transceiver and LatticeECP2

Pin #	MAX3454EETE	NCN2500MNR2	LatticeECP2 I/O	Description
1	SPD	DSPD	AB17	Connect to LatticeECP2 bank 4 I/O
2	RCV	RCV	AE13	Connect to LatticeECP2 bank 4 I/O
3	VP	VP	AD15	Connect to LatticeECP2 bank 4 I/O
4	VM	VM	AC15	Connect to LatticeECP2 bank 4 I/O
5	NC	EN_Vobus#	—	Connect to 3.3V
6	GND	GND	—	Connect to GND
7	SUS	SPND	AF13	Connect to LatticeECP2 bank 4 I/O
8	NC	NC	—	No connect
9	OE#	OE#	Y15	Connect to LatticeECP2 bank 4 I/O
10	D-	D-	—	Connect to USB connectors through 33 Ohm resistor
11	D+	D+	—	Connect to USB connectors through 33 Ohm resistor
12	Vtrm	Vreg	—	Connect to GND though a capacitor
13	ENUM	Vobus	—	Connect to J26 pin 2
14	Vbus	Vusb	—	Connect to USB connectors
15	VL	Vcc	—	Connect to 3.3V
16	NC	EN_RPU	—	Connect to J26 pin 2

RS-232

The RS-232 interface on this board includes a RS-232 interface chip (MAX3232), a 9-pin D-sub female connector and four headers. This RS-232 interface can be configured to DCE or DTE by changing the jumper settings of J10, J12, J15 and J16 headers. These headers are used to connect the MAX3232 to the D-sub connector. Installing jumpers on pin 1 and pin 2 of these headers configures the RS-232 to DCE. Installing jumpers on pin 2 and pin 3 of these headers configures the RS-232 to DTE. The connections and functions of the signals between MAX3232 and LatticeECP2 stay the same for DCE and DTE configurations. They are listed in Table 23.

Table 23. Connections Between MAX3232 and ECP2

Signal Name	MAX3232 Pin	LatticeECP2 I/O Ball	LatticeECP2 Bank	LatticeECP2 I/O
/CTS	9 (R2OUT)	AA19	4	Input
RXD	12 (R1OUT)	W17	4	Input
TXD	11 (T1IN)	Y19	4	Output
/RTS	10 (T2IN)	Y17	4	Output

DDR2

Two 200-pin SODIMM sockets included on the board provide a built-in 64-bit interface to standard 1.8V DDR2 SDRAM memory modules. The required VREF and VTT voltages, as well as termination of each signal to VTT are provided. Performance has been verified at above the 533Mbps data rate for one module with 1T clocking. The control lines for both modules are wired to drive as a 2T connection. Expect some reduction in max data rate when driving two modules with 1T signaling. Write mode dynamic ODT at the memory modules is fully supported, while read mode ODT at the controller (FPGA) is approximated with external terminations optimized for best performance.

Socket J3 is a reverse orientation version of socket J7. On some boards, the information "2.5V STD 52" is written in raised-lettering on this socket component. Ignore this marking. This is a 1.8V DDR2 socket. Additionally, please exercise caution when using DDR2 memory modules in J7 sockets with this marking. It is possible for modules to physically shift position, which in turn will short Pin 1 to pin 3, shorting VREF to VSS, and shutting down the power regulator for VTT and VREF. This will not damage the board or memory module, but the DDR2 memory will not respond when this situation is present.

When using a single DDR2 memory module, use socket J7.

The following memory modules are examples which can be used in the 200-pin SODIMM socket. This list is provided for reference purposes only, and is not intended to be a complete list or endorsement of these products.

- Crucial (Micron) MT8HTF6464HDY (512MB)
- Patriot PSD251253382S (512MB)
- Micron MT8HTF3264HDY (256MB)
- Kingston KVR667D2S5/256

Table 24. DDR2 Interface to SODIMM Sockets

Description	LatticeECP2 I/O Ball	sysIO Bank	J7 (Closer to LatticeECP2)	J3 (Further Away)
DDR2_DQ0	AE12	5	5	5
DDR2_DQ1	AB14	5	7	7
DDR2_DQ2	AA15	5	17	17
DDR2_DQ3	AD14	5	19	19
DDR2_DQ4	W14	5	4	4
DDR2_DQ5	Y14	5	6	6
DDR2_DQ6	AB13	5	14	14
DDR2_DQ7	AF12	5	16	16
DDR2_DM0	**AF10**	**5**	**10**	**10**
DDR2_DQS0_P	**AE11**	**5**	**13**	**13**
DDR2_DQS0_N	**AB11**	**5**	**11**	**11**
DDR2_DQ8	AB15	5	23	23
DDR2_DQ9	Y13	5	25	25
DDR2_DQ10	AF8	5	35	35
DDR2_DQ11	AE8	5	37	37
DDR2_DQ12	AC12	5	20	20
DDR2_DQ13	AD12	5	22	22
DDR2_DQ14	AC14	5	36	36
DDR2_DQ15	AD13	5	38	38
DDR2_DM1	**Y12**	**5**	**26**	**26**
DDR2_DQS1_P	**AC13**	**5**	**31**	**31**

Table 24. DDR2 Interface to SODIMM Sockets (Continued)

Description	LatticeECP2 I/O Ball	sysIO Bank	J7 (Closer to LatticeECP2)	J3 (Further Away)
DDR2_DQS1_N	**AA13**	**5**	**29**	**29**
DDR2_DQ16	AB11	5	43	43
DDR2_DQ17	AD8	5	45	45
DDR2_DQ18	AC9	5	55	55
DDR2_DQ19	AA11	5	57	57
DDR2_DQ20	AB9	5	44	44
DDR2_DQ21	AD9	5	46	46
DDR2_DQ22	AB8	5	56	56
DDR2_DQ23	AB10	5	58	58
DDR2_DM2	**AC8**	**5**	**52**	**52**
DDR2_DQS2_P	**AE6**	**5**	**51**	**51**
DDR2_DQS2_N	**AF6**	**5**	**49**	**49**
DDR2_DQ24	AE5	5	61	61
DDR2_DQ25	AF5	5	63	63
DDR2_DQ26	AC5	5	73	73
DDR2_DQ27	AD5	5	75	75
DDR2_DQ28	AA7	5	62	62
DDR2_DQ29	AB7	5	64	64
DDR2_DQ30	AD4	5	74	74
DDR2_DQ31	AE4	5	76	76
DDR2_DM3	**AF4**	**5**	**67**	**67**
DDR2_DQS3_P	**AA6**	**5**	**70**	**70**
DDR2_DQS3_N	**AB6**	**5**	**68**	**68**
DDR2_DQ32	W8	6	123	123
DDR2_DQ33	AD3	6	125	125
DDR2_DQ34	W7	6	135	135
DDR2_DQ35	AC2	6	137	137
DDR2_DQ36	AE2	6	124	124
DDR2_DQ37	AD2	6	126	126
DDR2_DQ38	Y7	6	134	134
DDR2_DQ39	Y8	6	136	136
DDR2_DM4	**W5**	**6**	**130**	**130**
DDR2_DQS4_P	**AB3**	**6**	**131**	**131**
DDR2_DQS4_N	**AB2**	**6**	**129**	**129**
DDR2_DQ40	U7	6	141	141
DDR2_DQ41	U6	6	143	143
DDR2_DQ42	U8	6	151	151
DDR2_DQ43	V8	6	153	153
DDR2_DQ44	AA1	6	140	140
DDR2_DQ45	AB1	6	142	142
DDR2_DQ46	Y3	6	152	152
DDR2_DQ47	Y4	6	154	154
DDR2_DM5	**U3**	**6**	**147**	**147**
DDR2_DQS5_P	**W3**	**6**	**148**	**148**

Table 24. DDR2 Interface to SODIMM Sockets (Continued)

Description	LatticeECP2 I/O Ball	sysIO Bank	J7 (Closer to LatticeECP2)	J3 (Further Away)
DDR2_DQS5_N	**W4**	**6**	**146**	**146**
DDR2_DQ48	T6	6	157	157
DDR2_DQ49	W1	6	159	159
DDR2_DQ50	R5	6	173	173
DDR2_DQ51	Y2	6	175	175
DDR2_DQ52	V2	6	158	158
DDR2_DQ53	W2	6	160	160
DDR2_DQ54	U2	6	174	174
DDR2_DQ55	R4	6	176	176
DDR2_DM6	**P3**	**6**	**170**	**170**
DDR2_DQS6_P	**R6**	**6**	**169**	**169**
DDR2_DQS6_N	**R7**	**6**	**167**	**167**
DDR2_DQ56	P6	6	179	179
DDR2_DQ57	V1	6	181	181
DDR2_DQ58	P8	6	189	189
DDR2_DQ59	U1	6	191	191
DDR2_DQ60	P5	6	180	180
DDR2_DQ61	P4	6	182	182
DDR2_DQ62	N5	6	192	192
DDR2_DQ63	P7	6	194	194
DDR2_DM7	**N7**	**6**	**185**	**185**
DDR2_DQS7_P	**T1**	**6**	**188**	**188**
DDR2_DQS7_N	**T2**	**6**	**186**	**186**
DDR2_A0	W6	6	102	102
DDR2_A1	Y6	6	101	101
DDR2_A2	W10	5	100	100
DDR2_A3	Y10	5	99	99
DDR2_A4	W11	5	98	98
DDR2_A5	AA10	5	97	97
DDR2_A6	U4	6	94	94
DDR2_A7	AD10	5	92	92
DDR2_A8	AC10	5	93	93
DDR2_A9	AA12	5	91	91
DDR2_A10	V4	6	105	105
DDR2_A11	W12	5	90	90
DDR2_A12	AB12	5	89	89
DDR2_A13	AF9	5	116	116
DDR_BA0	U5	6	107	107
DDR_BA1	V3	6	106	106
DDR_BA2	AE9	5	85	85
DDR2_CK0_P	**V9**	**5**	**30**	**—**
DDR2_CK0_N	**W9**	**5**	**32**	**—**
DDR2_CK1_P	**W13**	**5**	**164**	**—**

Table 24. DDR2 Interface to SODIMM Sockets (Continued)

Description	LatticeECP2 I/O Ball	sysIO Bank	J7 (Closer to LatticeECP2)	J3 (Further Away)
DDR2_CK1_N	**AA14**	**5**	**166**	**—**
DDR2_CK2_P	**N3**	**6**	**—**	**30**
DDR2_CK2_N	**N4**	**6**	**—**	**32**
DDR2_CK3_P	**AC1**	**6**	**—**	**164**
DDR2_CK3_N	**AD1**	**6**	**—**	**166**
DDR2_CKE0	AE10	5	79	79
DDR2_CKE1	T7	6	80	80
DDR2_S0_N	Y1	6	110	—
DDR2_S1_N	AC7	5	115	—
DDR2_S2_N	V5	6	—	110
DDR2_S3_N	Y5	6	—	115
DDR2_RAS_N	AD7	5	108	108
DDR2_CAS_N	R3	6	113	113
DDR2_WE_N	AA2	6	109	109
DDR2_ODT0	M5	6	114	—
DDR2_ODT1	M4	6	119	—
DDR2_ODT2	AE3	5	—	114
DDR2_ODT3	AC4	5	—	119
DDR2_SDA	C8	0	195	195
DDR2_SCL	D8	0	197	197

SPI 4.2

Two 6x10 VHDM backplane connectors, J35 and J36 are provided for SPI4.2 interfaces. Connector J35 includes necessary data pairs and control signals for transmit data, while J36 has been configured for receive data. Standard 100-ohm differential termination is provided for all applicable receive signal pairs of J36. The J35 and J36 connections to the LatticeECP2 are listed in Table 25 and Table 26.

Table 25. SPI4.2 Transmit Connections

J35 Pin	Description	LatticeECP2 I/O Ball	sysIO Bank
A1	SPI4_TDAT_P14	P22	3
A2	SPI4_TDAT_P12	M25	3
A3	SPI4_TDAT_P10	K22	2
A4	SPI4_TDAT_P8	J24	2
A7	SPI4_TDAT_P6	F25	2
A8	SPI4_TDAT_P4	G23	2
A9	SPI4_TDAT_P2	C25	2
A10	SPI4_TDAT_P0	C23	2
B1	SPI4_TDAT_N14	P23	3
B2	SPI4_TDAT_N12	M26	3
B3	SPI4_TDAT_N10	L21	2
B4	SPI4_TDAT_N8	K24	2
B7	SPI4_TDAT_N6	F26	2
B8	SPI4_TDAT_N4	G24	2
B9	SPI4_TDAT_N2	D25	2

Table 25. SPI4.2 Transmit Connections (Continued)

J35 Pin	Description	LatticeECP2 I/O Ball	sysIO Bank
B10	SPI4_TDAT_N0	D23	2
C1	SPI4_TCTL_P	F21	2
C5	SPI4_TSTAT0	M23	2
C6	SPI4_TSCLK	N23	2
D1	SPI4_TCTL_N	E22	2
D5	SPI4_TSTAT1	N24	2
E1	SPI4_TDAT_P15	M22	2
E2	SPI4_TDAT_P13	L25	3
E3	SPI4_TDAT_P11	N25	3
E4	SPI4_TDAT_P9	R19	3
E6	SPI4_TDCLK_P	K25	2
E7	SPI4_TDAT_P7	G22	2
E8	SPI4_TDAT_P5	C26	2
E9	SPI4_TDAT_P3	E25	2
E10	SPI4_TDAT_P1	H25	2
F1	SPI4_TDAT_N15	L22	2
F2	SPI4_TDAT_N13	L26	3
F3	SPI4_TDAT_N11	N26	3
F4	SPI4_TDAT_N9	P20	3
F6	SPI4_TDCLK_N	K26	2
F7	SPI4_TDAT_N7	H21	2
F8	SPI4_TDAT_N5	D26	2
F9	SPI4_TDAT_N3	E26	2
F10	SPI4_TDAT_N1	H26	2

Table 26. SPI4.2 Receive Connections

J36 Pin	Description	LatticeECP2 I/O Ball	sysIO Bank
A1	SPI4_RDAT_P0	R23	3
A2	SPI4_RDAT_P2	T21	3
A3	SPI4_RDAT_P4	R21	3
A4	SPI4_RDAT_P6	T22	3
A7	SPI4_RDAT_P8	U26	3
A8	SPI4_RDAT_P10	Y26	3
A9	SPI4_RDAT_P12	W26	3
A10	SPI4_RDAT_P14	U25	3
B1	SPI4_RDAT_N0	R24	3
B2	SPI4_RDAT_N2	R22	3
B3	SPI4_RDAT_N4	N22	3
B4	SPI4_RDAT_N6	T20	3
B7	SPI4_RDAT_N8	V26	3
B8	SPI4_RDAT_N10	AA26	3
B9	SPI4_RDAT_N12	W25	3
B10	SPI4_RDAT_N14	U24	3
C5	SPI4_RSCLK	M24	2

Table 26. SPI4.2 Receive Connections (Continued)

J36 Pin	Description	LatticeECP2 I/O Ball	sysIO Bank
C6	SPI4_RSTAT0	N21	3
C10	SPI4_RCTL_P	N20	3
D6	SPI4_RSTAT1	N18	3
D10	SPI4_RCTL_N	N19	3
E1	SPI4_RDAT_P1	P19	3
E2	SPI4_RDAT_P3	P25	3
E3	SPI4_RDAT_P5	R25	3
E4	SPI4_RDAT_P7	U20	3
E5	SPI4_RDCLK_P	T26	3
E7	SPI4_RDAT_P9	U23	3
E8	SPI4_RDAT_P11	V25	3
E9	SPI4_RDAT_P13	U19	3
E10	SPI4_RDAT_P15	V23	3
F1	SPI4_RDAT_N1	P21	3
F2	SPI4_RDAT_N3	P26	3
F3	SPI4_RDAT_N5	R26	3
F4	SPI4_RDAT_N7	T19	3
F5	SPI4_RDCLK_N	T25	3
F7	SPI4_RDAT_N9	U22	3
F8	SPI4_RDAT_N11	V24	3
F9	SPI4_RDAT_N13	U21	3
F10	SPI4_RDAT_N15	W24	3

Ethernet PHY

In the upper-left corner of the board is U1, a National Semiconductor Gigabit Ethernet PHY (DP83865). The LatticeECP2 FPGA interacts with the PHY over a Media Independent Interface (MII). The PHY is connected to an RJ45 connector J2 on the Media Dependent Interface (MDI). The RJ45 connector J2 has built in magnetics and spark-gap capacitor.

The PHY is available on the board in order to demonstrate the Lattice Ethernet Media Access (MAC) IP core. However, it is also possible to use the PHY to evaluate a custom MAC solution.

Refer to the schematic and the National Semiconductor DP83865 Data Sheet for detailed information about the operation of the Ethernet PHY interface on this device. Refer to Table 27 for a description of the Ethernet PHY connections.

Table 27. 10/100/1000 Ethernet PHY Connection Summary

Description	LatticeECP2 I/O	sysIO Bank
ETH_CLK_TO_MAC	C4	0
ETH_COL	B3	0
ETH_CRS	B2	0
ETH_EGP0	(low, install R1 to pull high)	—
ETH_EGP2	G5	0
ETH_EGP4	G6	0
ETH_EGP5	B4	0
ETH_EGP6	D5	0

Table 27. 10/100/1000 Ethernet PHY Connection Summary (Continued)

Description	LatticeECP2 I/O	sysIO Bank
ETH_EGP7	C5	0
ETH_GTX_CLK	E9	0
ETH_MAC_CLK_EN	C3	0
ETH_MDC	F11	0
ETH_MDIO	E10	0
ETH_RESET_N	A4	0
ETH_RX_CLK	A3	0
ETH_RX_D0	E5	0
ETH_RX_D1	E6	0
ETH_RX_D2	F7	0
ETH_RX_D3	E7	0
ETH_RX_D4	G7	0
ETH_RX_D5	G8	0
ETH_RX_D6	C1	0
ETH_RX_D7	C2	0
ETH_RX_DV	D4	0
ETH_RX_ER	D3	0
ETH_TX_CLK	D9	0
ETH_TX_D0	H9	0
ETH_TX_D1	F8	0
ETH_TX_D2	F10	0
ETH_TX_D3	E8	0
ETH_TX_D4	D7	0
ETH_TX_D5	C7	0
ETH_TX_D6	B5	0
ETH_TX_D7	A5	0
ETH_TX_EN	G10	0
ETH_TX_ER	H10	0

TI DSP Motherboard Peripheral Connector

The 80-pin Samtec connector TFM-140-31-S-D-LC installed at the upper-left corner on the bottom side of the board is used for connecting to the peripheral connector of Texas Instruments DSP motherboards. With this peripheral connector and proper LatticeECP2 FPGA design, the board can be a daughter card for the DSP motherboards. There are two connectors on the DSP motherboard; a memory connector, and a peripheral connector for attaching daughter cards. The memory connector is an interface (EMIF) used for connecting the DSP to different types of memory devices. Note that only the peripheral connector is implemented on the LatticeECP2 Advanced Engineering board. Refer to Table 28 for a description of the peripheral interface connections based on the "Future Daughtercard Interface" section of the TI's TMS320 Cross-Platform Daughtercard Specification Revision 1.0.

Table 28. TI DSP Motherboard Peripheral Interface Connection

J57 Pin#	Signal	I/O	Description	Connection to LatticeECP2
1	12V	Vcc	12V voltage supply pin	NC (Connected to TP28)
2	-12V	Vcc	-12V voltage supply pin	NC (Connected to TP34)
3	GND	Vss	System ground	GND
4	GND	Vss	System ground	GND

Table 28. TI DSP Motherboard Peripheral Interface Connection (Continued)

J57 Pin#	Signal	I/O	Description	Connection to LatticeECP2
5	5V	Vcc	5V voltage supply pin	VCC_5.0V
6	5V	Vcc	5V voltage supply pin	VCC_5.0V
7	GND	Vss	System ground	GND
8	GND	Vss	System ground	GND
9	5V	Vcc	5V voltage supply pin	VCC_5.0V
10	5V	Vcc	5V voltage supply pin	VCC_5.0V
11	N/C	—	Reserved	NC
12	N/C	—	Reserved	NC
13	N/C	—	Reserved	NC
14	N/C	—	Reserved	NC
15	N/C	—	Reserved	NC
16	N/C	—	Reserved	NC
17	N/C	—	Reserved	NC
18	N/C	—	Reserved	NC
19	3.3V	Vcc	3.3V voltage supply pin	VCC_3.3V
20	3.3V	Vcc	3.3V voltage supply pin	VCC_3.3V
21	DC_CLKXb	I/O	Secondary serial port transmit clock	E12
22	DC_CLKSb	I	Secondary serial port clock source	B6
23	DC_FSXb	I/O	Secondary serial port transmit frame sync	B9
24	DC_DXb	O	Secondary serial port transmit data	A6
25	GND	Vss	System ground	GND
26	GND	Vss	System ground	GND
27	DC_CLKRb	I/O	Secondary serial port receive clock	A9
28	N/C	—	Reserved	NC
29	DC_FSRb	I/O	Secondary serial port receive frame sync	H12
30	DC_DRb	I	Secondary serial port receive data	G11
31	GND	Vss	System ground	GND
32	GND	Vss	System ground	GND
33	DC_CLKXa	I/O	Primary serial port transmit clock	G13
34	DC_CLK_Sa	I	Primary serial port clock source	H11
35	DC_FSXa	I/O	Primary serial port frame sync	C10
36	DC_Dxa	O	Primary serial port transmit data	D10
37	GND	Vss	System ground	GND
38	GND	Vss	System ground	GND
39	DC_CLKRa	I/O	Primary serial port receive clock	C12
40	N/C	—	Reserved	NC
41	DC_FSRa	I/O	Primary serial port receive frame sync	B10
42	DC_DRa	I	Primary serial port receive data	F12
43	GND	Vss	System ground	GND
44	GND	Vss	System ground	GND
45	DC_TOUTa	O	Primary timer output	A10
46	DC_TINPa	I	Primary timer input	B7
47	N/C	—	Reserved	NC
48	DC_INTb	I	Secondary interrupt	A7

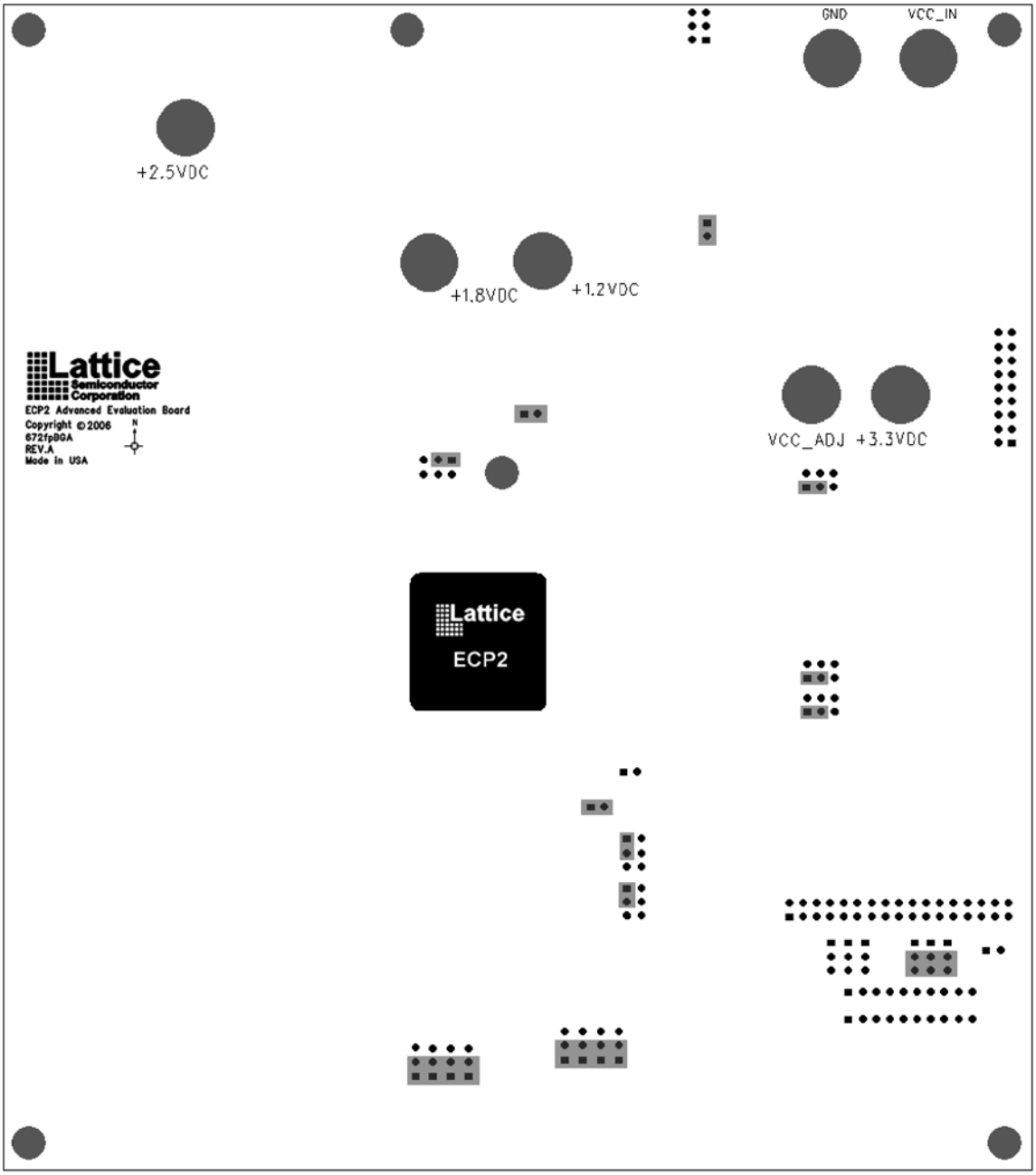
Table 28. TI DSP Motherboard Peripheral Interface Connection (Continued)

J57 Pin#	Signal	I/O	Description	Connection to LatticeECP2
49	DC_TOUTb	O	Secondary timer output	F13
50	DC_TINPb	I	Secondary timer input	C9
51	GND	Vss	System ground	GND
52	GND	Vss	System ground	GND
53	DC_INTa	I	Primary interrupt	D12
54	NC	—	Reserved	NC
55	NC	—	Reserved	NC
56	NC	—	Reserved	NC
57	NC	—	Reserved	NC
58	NC	—	Reserved	NC
59	DC_RESET#	O	System reset	E13
60	NC	—	Reserved	NC
61	GND	Vss	System ground	GND
62	GND	Vss	System ground	GND
63	DC_CNTLb	O	Daughtercard control	C13
64	DC_CNTLa	O	Daughtercard control	E11
65	DC_STATb	I	Daughtercard status	B11
66	DC_STATa	I	Daughtercard status	B8
67	DC_INTc	I	Third interrupt	A11
68	DC_INTd	I	Fourth interrupt	A8
69	NC	—	Reserved	NC
70	NC	—	Reserved	NC
71	NC	—	Reserved	NC
72	NC	—	Reserved	NC
73	NC	—	Reserved	NC
74	NC	—	Reserved	NC
75	GND	Vss	System ground	GND
76	GND	Vss	System ground	GND
77	GND	Vss	System ground	GND
78	DC_CLKOUT	O	Daughtercard clock	G12
79	GND	Vss	System ground	GND
80	GND	Vss	System ground	GND

Default Jumper Settings

The evaluation board is shipped with default jumper positions as shown in Figure 4. Some jumper settings are required for bitstream downloading and display functionality.

Figure 4. Default Jumper Settings



Initial Setup and Handling

The following discussion is recommended reading prior to removing the evaluation board from the static shielding bag and may or may not apply to your particular use of the board.

CAUTION: The devices on the board can be damaged by improper handling.

The devices on the evaluation board contain fairly robust ESD (Electro Static Discharge) protection structures within them, able to withstand typical static discharges (see the "Human Body Model" specification for an example of ESD characterization requirements). Even so, the devices are static sensitive to conditions that exceed their designed in protection. For example: higher static voltages, as well as lower voltages with lower series resistance or larger capacitance than the respective ESD specifications require can potentially damage or degrade the devices on the evaluation board.

As such, it is recommended that you wear an approved and functioning grounded wrist strap at all times while handling the evaluation board when it is removed from the static shielding bag. If you will not be using the board for a while, it's best to put it back in the static shielding bag. Please save the static shielding bag and packing box for future storage of the board when it is not in use.

When reaching for the board, it is recommended that you first touch the outside threaded portion of one of the gold SMA connectors. This will neutralize any static voltage difference between your body and the board prior to any contact with signal I/O.

CAUTION: To minimize the possibility of ESD damage, the first and last electrical connections to the board, should always be from test equipment chassis ground to the J42 GND (black banana jack).

Before connecting signals or power to the board, attach a cable from chassis ground on grounded test equipment to the J42 GND. Connecting the board ground to test equipment chassis ground will decrease the risk of ESD damage to the I/O on the board as the initial connections to the board are made. Likewise, when unplugging cables from the evaluation board, the last connection unplugged, should be the chassis GND connection to J42 GND. If you have signal sources that are floating with respect to chassis GND, attempt to neutralize any static charge on that signal source prior to attaching it to the evaluation board.

If you are holding or carrying the board while it's not in a static shielding bag, please keep one finger on the threaded portion of one of the gold SMA connectors. This will keep the board at the same voltage potential as your body until you can pick up the static shielding bag and put the board back in it.

Configuring/Programming the Board

Requirements

- PC with Lattice's ispVM System version 16.0 (or later) programming software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable). *Note: An option to install these drivers is included as part of the ispVM System setup.*

  ispVM System software can be downloaded from the Lattice web site at www.latticesemi.com/ispvm.

- Any Lattice ispDOWNLOAD Cable (Parallel port or USB) (pDS4102-DL2x, HW7265-DL3x, HW-USB-2x, etc.). See the ispDOWNLOAD Cables Data Sheet for specifications and instructions for the use of these cables.

For a complete discussion of the LatticeECP2's configuration and programming options, refer to TN1108, LatticeECP2 sysCONFIG Usage Guide.

SRAM Configuration Using SPI Flash

The LatticeECP2 device is SRAM-based, so it must remain powered on to retain its configuration when programming the SRAM. The LatticeECP2 SRAM can be configured easily via the on board SPI Flash, which in turn can be programmed using the JTAG port and ispVM. The on-board SPI Flash retains its programmed bitstreams when power is off, and can quickly load programmed bitstreams into the LatticeECP2 device when power is applied. The following steps describe the procedure required to program the SPI Flash device on the board.

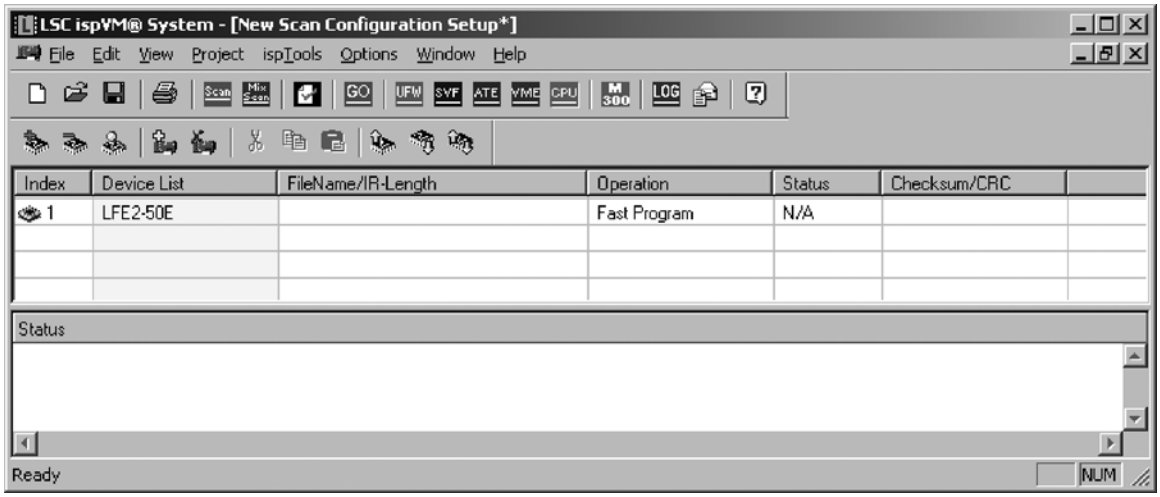
1. Check that the jumpers are installed as shown in Figure 4.

2. Connect the ispDOWNLOAD cable to the PC, and to the header on the board at J46. Note: When using a 1x8 download cable, connect to the 1x10 header by justifying the alignment to pin 1 (Vcc).

Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeECP2 FPGA device and render the board inoperable.*

3. Connect the LatticeECP2 Evaluation Board to an external 5V supply.
4. Start the ispVM System software.
5. Press the **SCAN** button located in the toolbar of the ispVM System software. The LatticeECP2 device should be automatically detected. The resulting screen should be similar to Figure 5.

Figure 5. ispVM System Interface



6. Double-click the device as shown in Figure 5 to open the **Device Information Dialog**, as shown in Figure 6. Select the **Device Access Options** and select **SPI Flash Programming** as shown in Figure 7.

Figure 6. Device Information Dialog

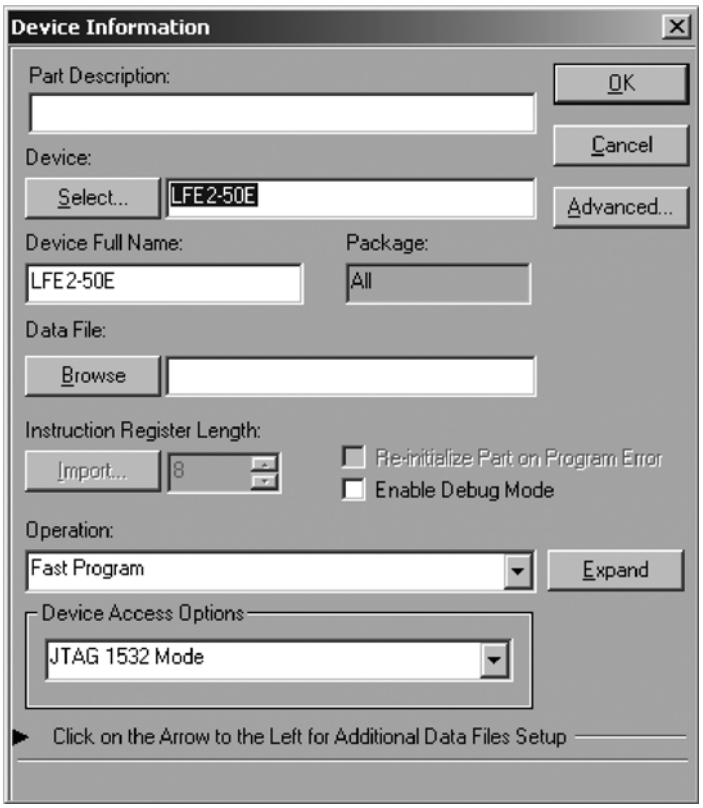
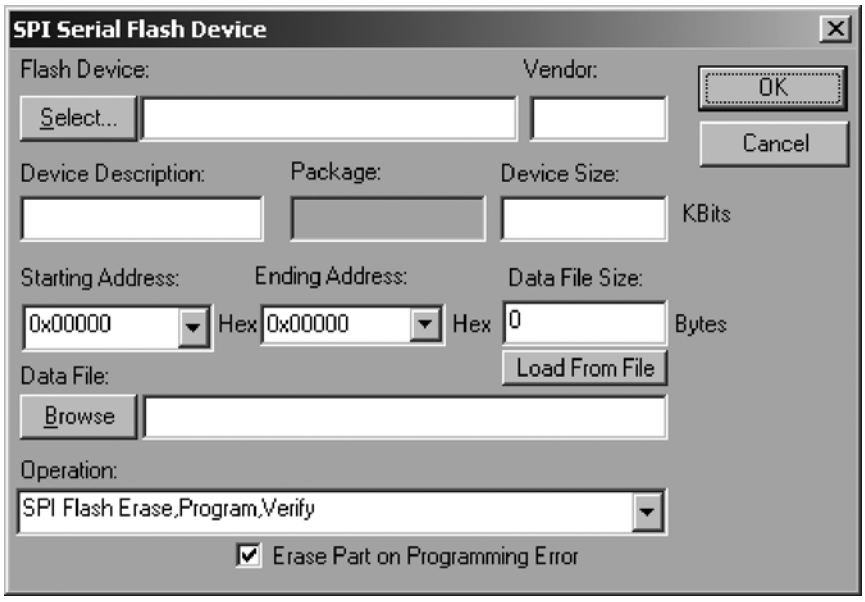


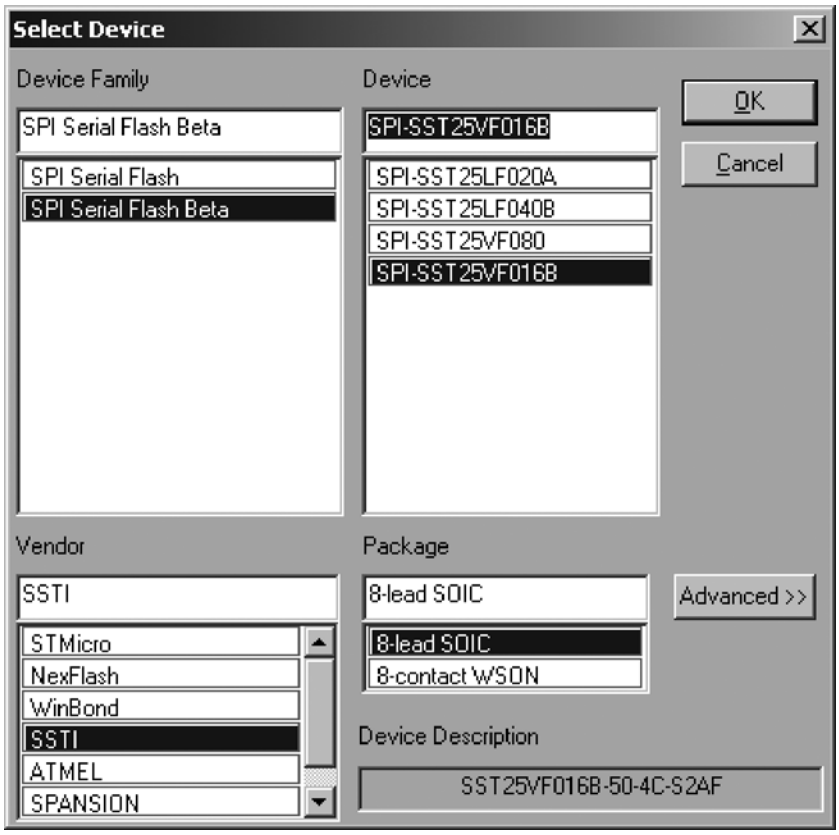
Figure 7. SPI Serial Flash Device Dialog



7. Select **Browse** and point to the location of the bitstream file. This example uses the LatticeECP2 Advanced Evaluation Board sample design bitstream. This is available for download from the Lattice web site at: www.latticesemi.com/products/developmenthardware/fpgafspcboards/ecp2advancedevaluationboa.cfm.

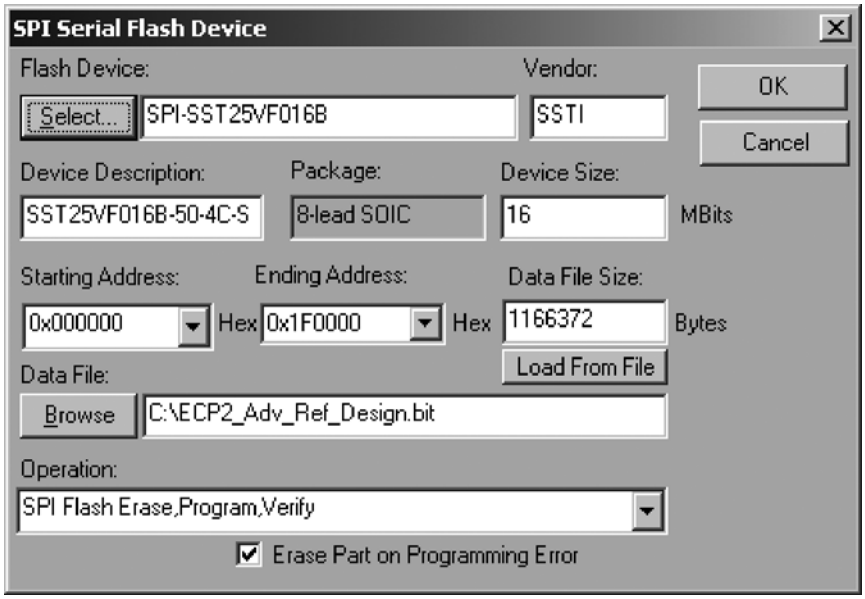
   Select **Flash Device** and in the Select Device window, change the selections as shown in Figure 8. Press **OK** to close the "Select Device" window.

Figure 8. Select Device Dialog



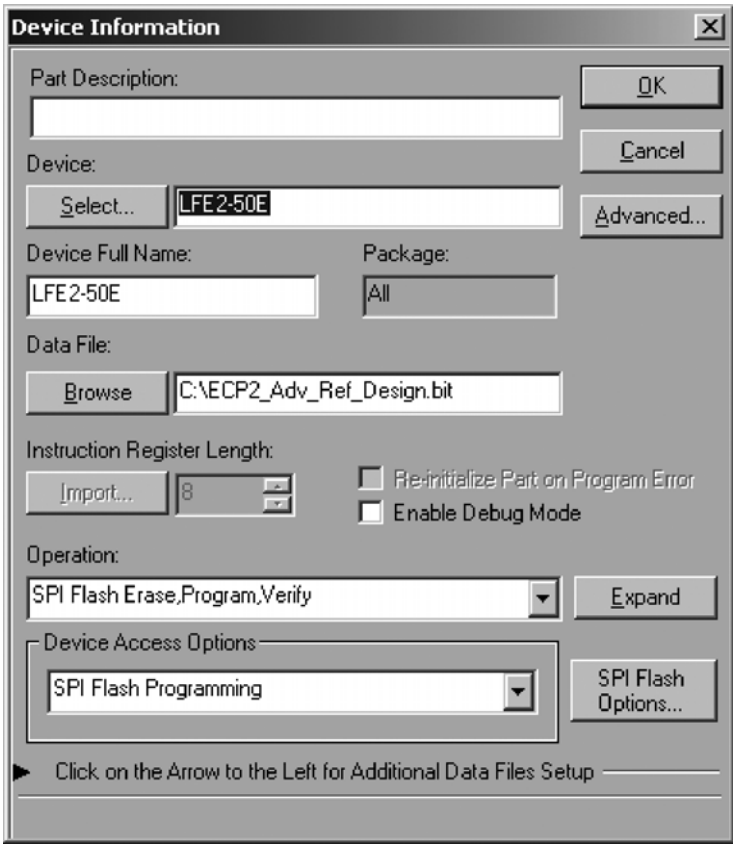
8. Check that the SPI Serial Flash Device window now appears as shown in Figure 9 and press **OK** to close the SPI Serial Flash Device window.

Figure 9. SPI Serial Flash Device Dialog



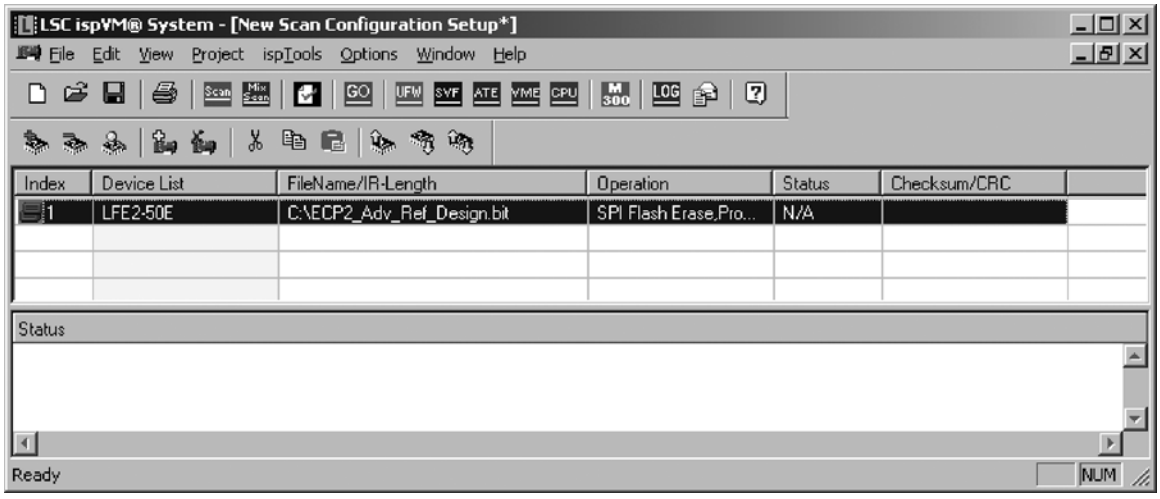
9. Check that the Device Information window appears as shown in Figure 10 and press **OK** to close the Device Information window.

Figure 10. Device Information Dialog



10. Check that the LSC ispVM System window appears as it does in Figure 11.

Figure 11. ispVM System Interface



11. To begin the download of the bitstream into the SPI Flash, press the **GO** menu button. You will see a small counter display window start up and then that window will change to a Processing address window. A blue section of that Processing window will start to fill in from the left side until it reaches the right side of the window. When downloading to SPI Flash is complete, ispVM will then begin to verify the downloaded bitstream loaded into the SPI Flash with another small processing window and blue bar moving across it.

12. Upon successful verification of the downloaded bitstream to SPI Flash, the LatticeECP2 device can then be programmed by pressing the **PROGRAMN** button (SW3) on the evaluation board.

13. If you have loaded the LatticeECP2 Advanced Evaluation Board sample program, you should now see the LatticeECP2 evaluation board's LED digit display incrementing from 0 to 9 and a to f, the digit decimal point should be blinking, and the LEDs below the digit should show the internal counter state while the digit count is incrementing.

14. If you cycle the power to the evaluation board, you will need to push the **PROGRAMN** (SW3) button again to reload the bitstream from the SPI Flash into the LatticeECP2 device.

Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
LatticeECP2 Advanced Evaluation Board (RoHS Compliant)	LFE2-50E-H-EVN	
LatticeECP2 Advanced Evaluation Board (Non-RoHS, Obsolete)	LFE2-50E-H-EV	

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
October 2006	01.0	Initial release.
February 2007	01.1	Updated DDR2 section.
March 2007	01.2	Added Ordering Information section.
April 2007	01.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.
June 2007	01.4	Updated DDR2 text section.
October 2007	01.5	Updated Placement and Dimensions schematic in Appendix A.
January 2009	01.6	Updated ordering information.

Appendix A. Schematics

Figure 12.

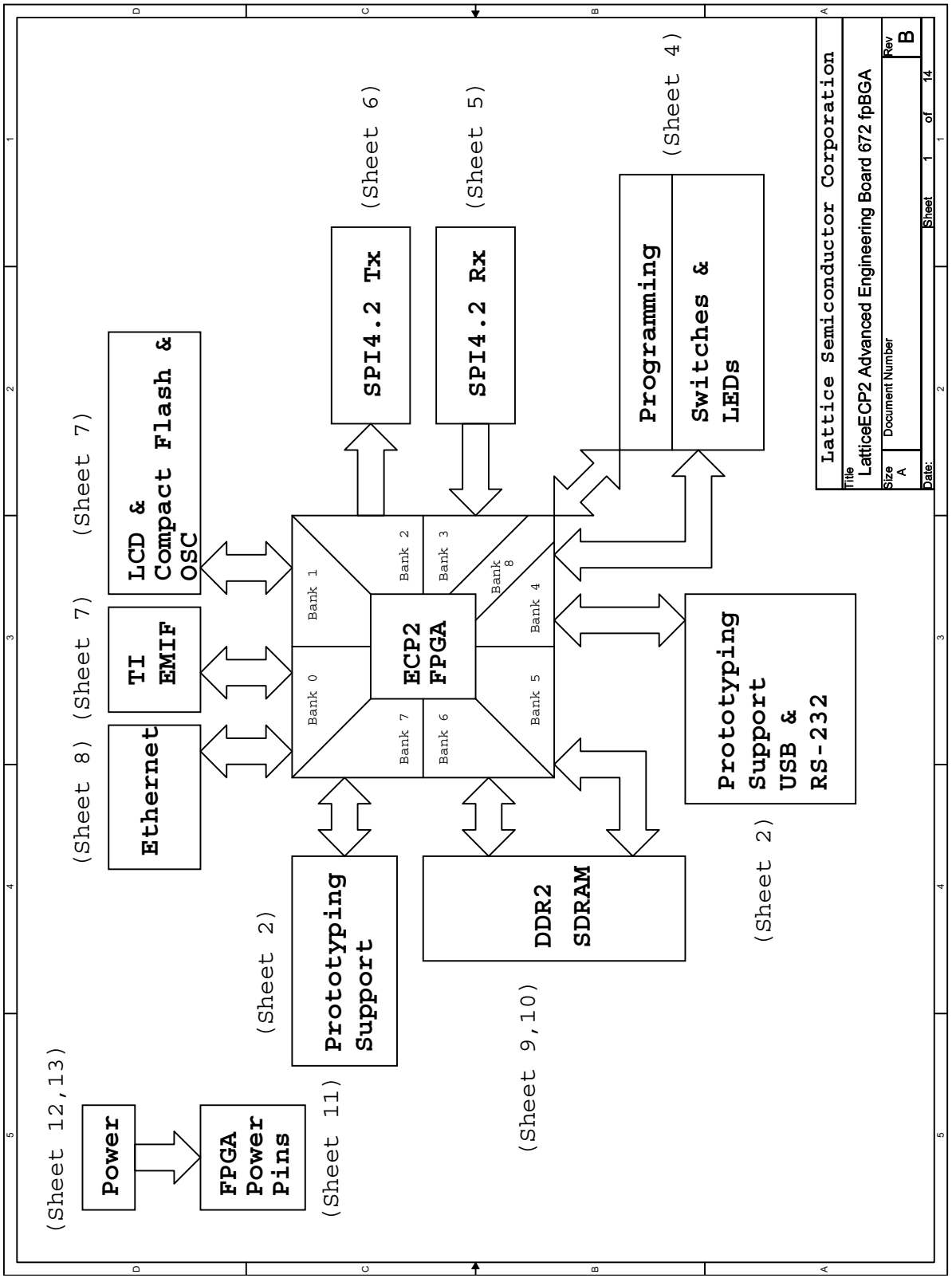


Figure 13. Prototyping Support

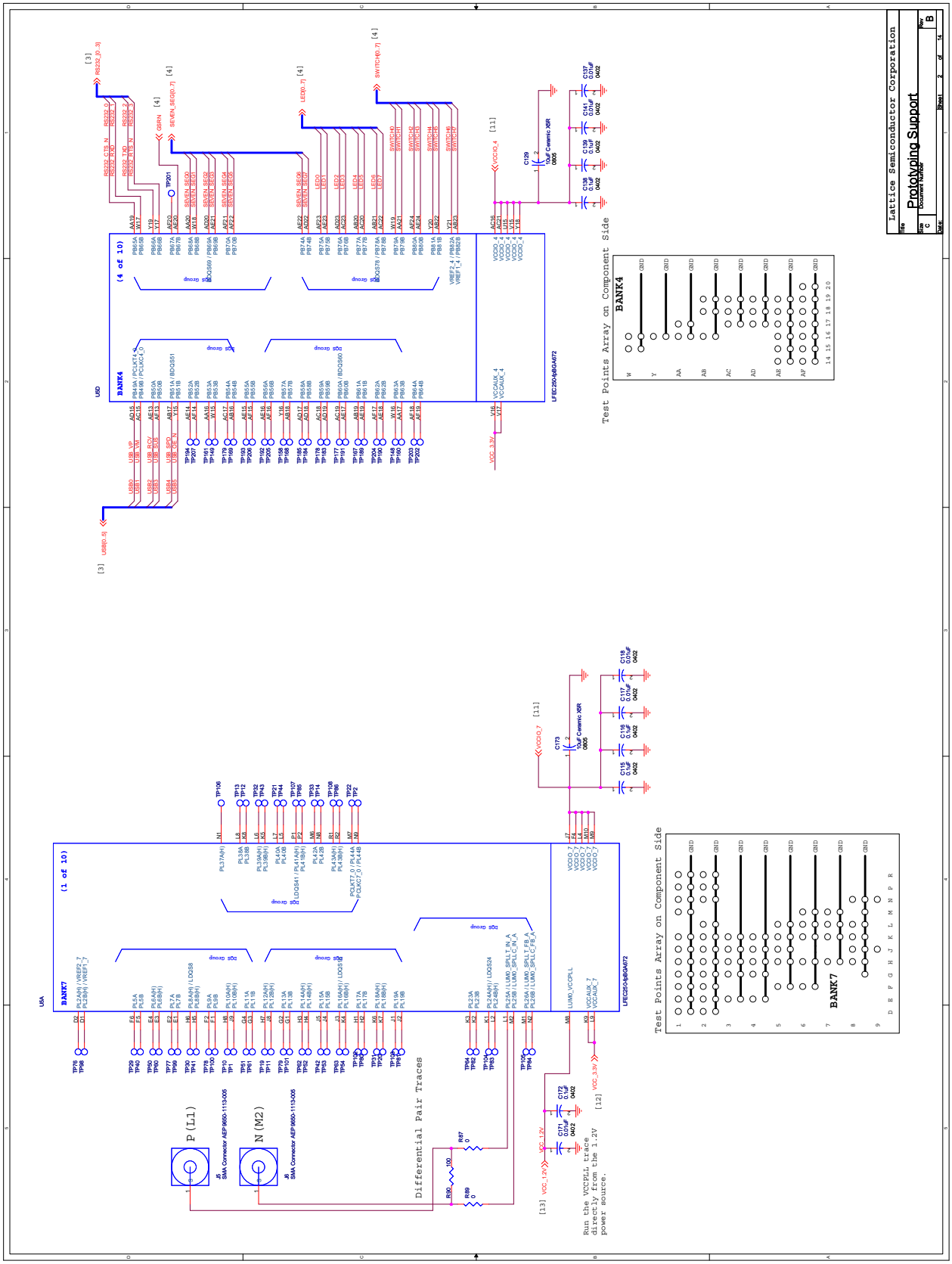


Figure 14. USB 1.1 and RS-232

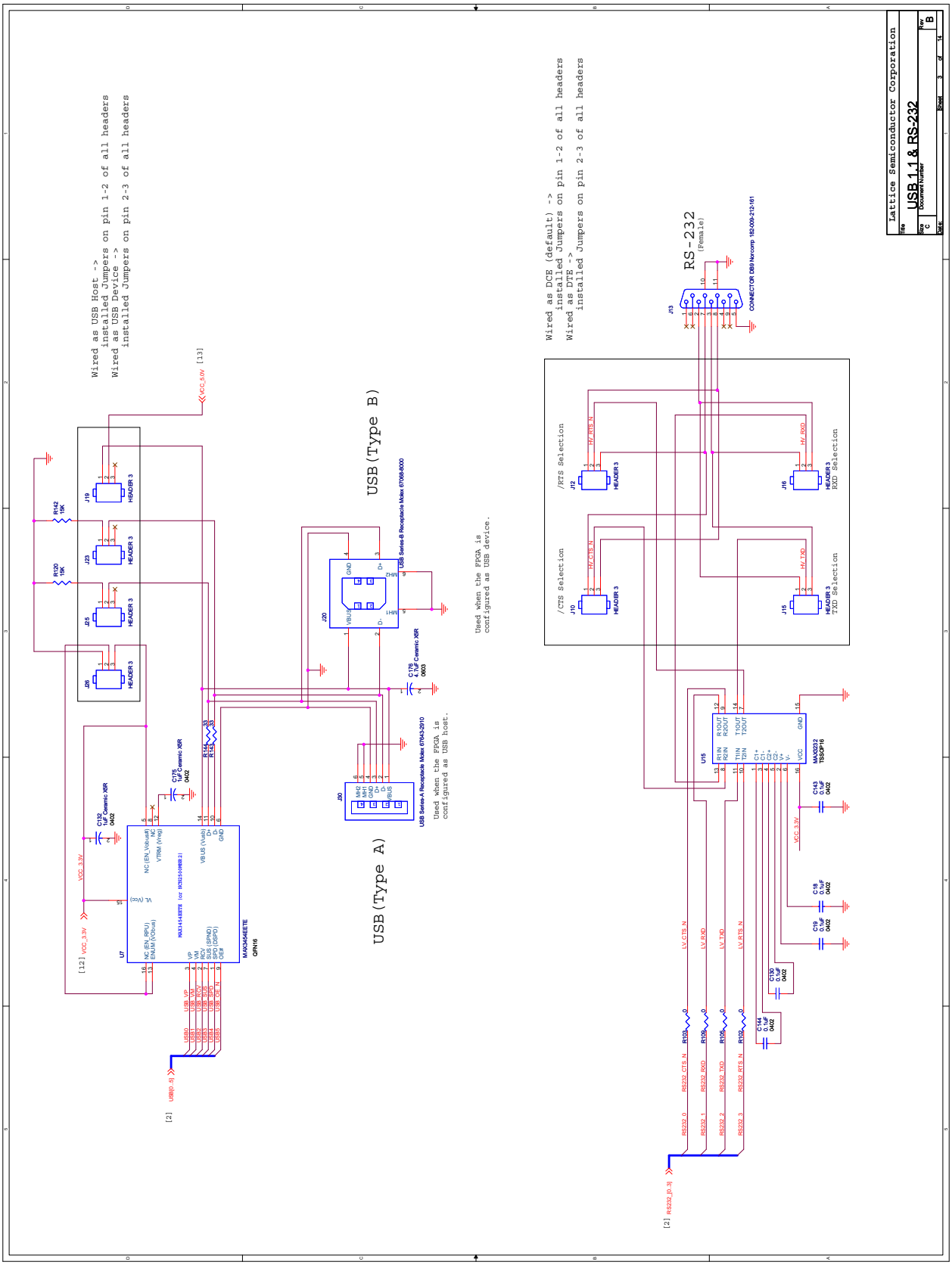


Figure 15. Program, Switches and LEDs

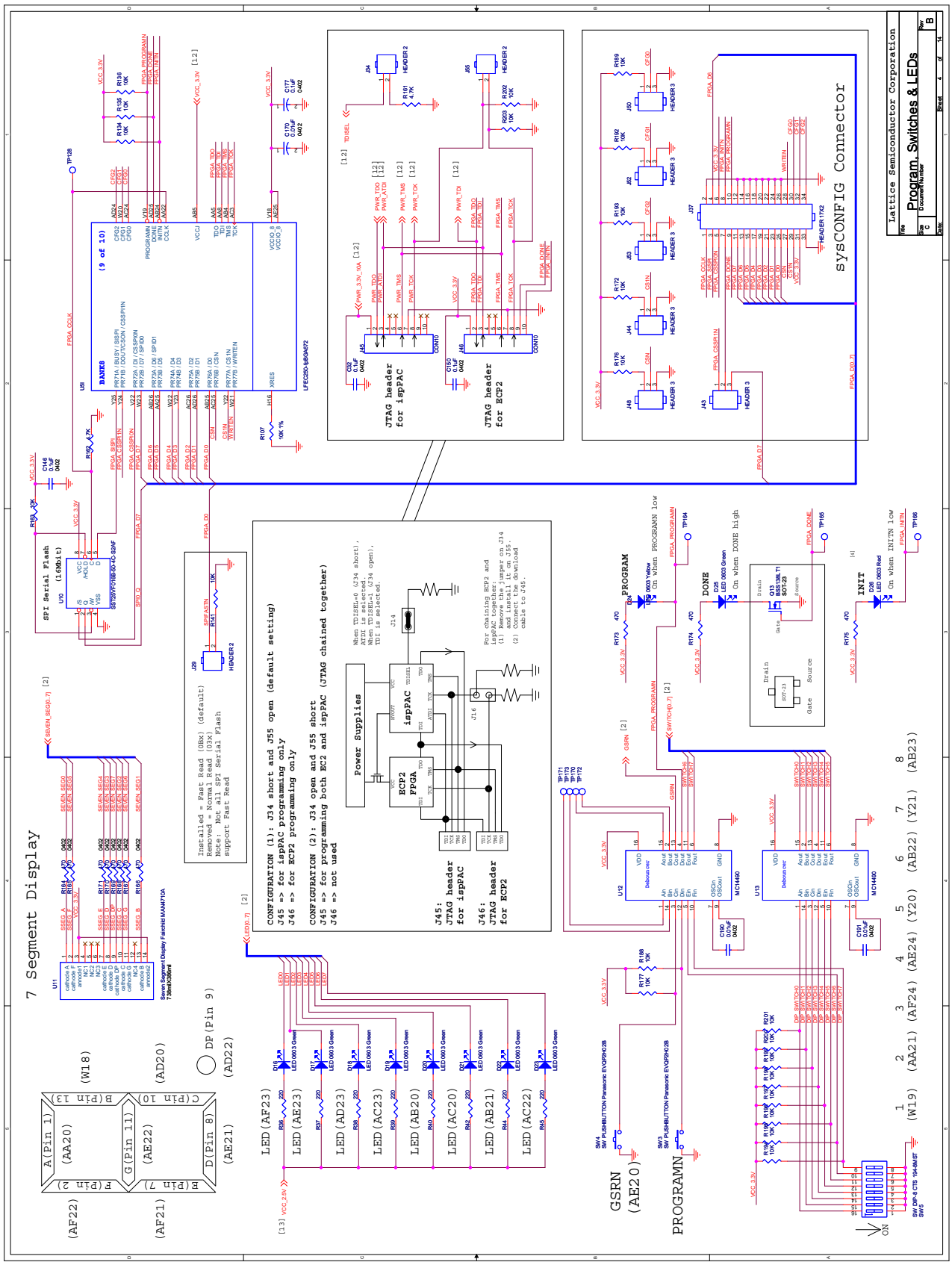


Figure 16. SPI4.2 Rx

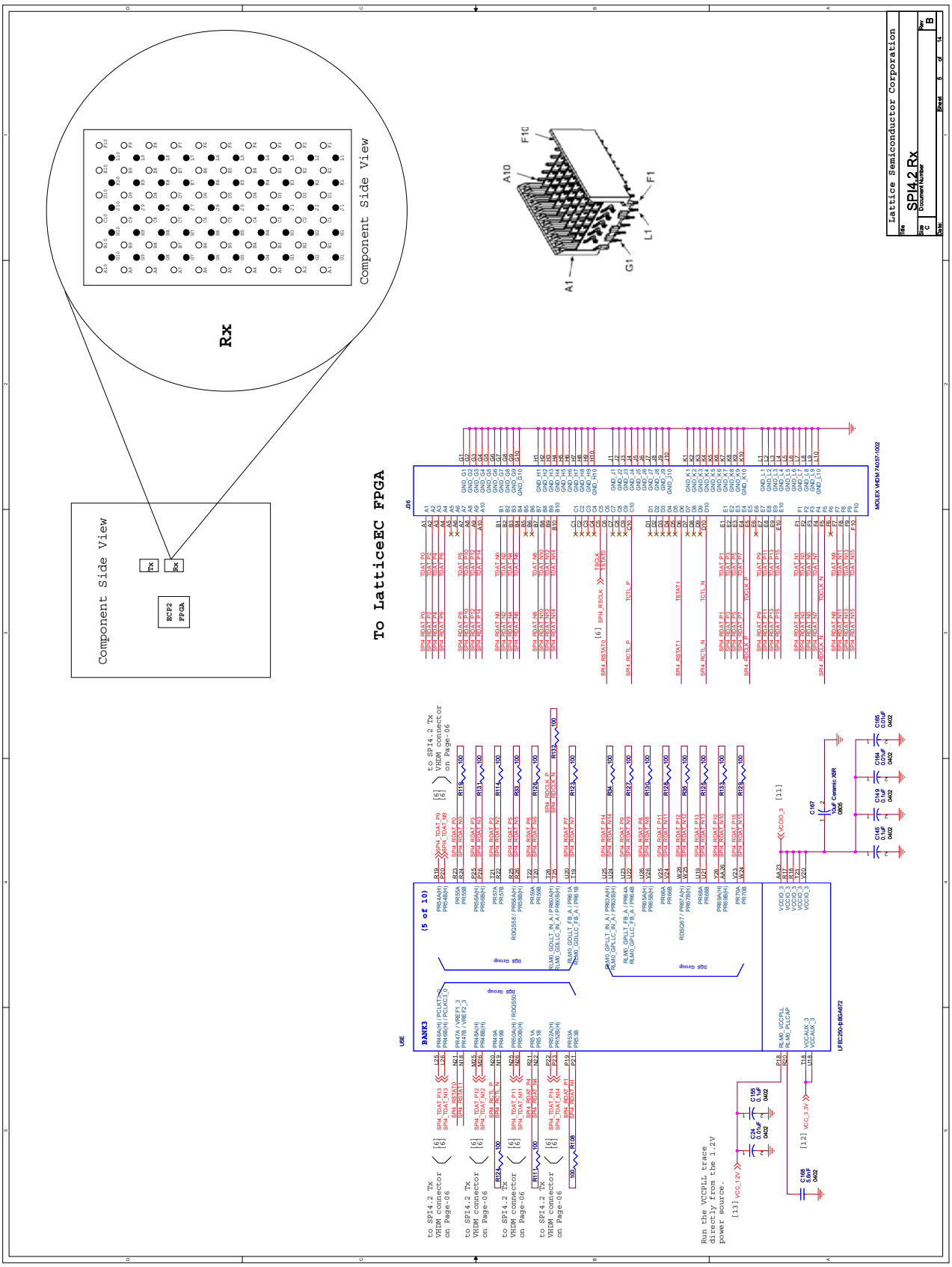


Figure 17. SPI4.2 Tx

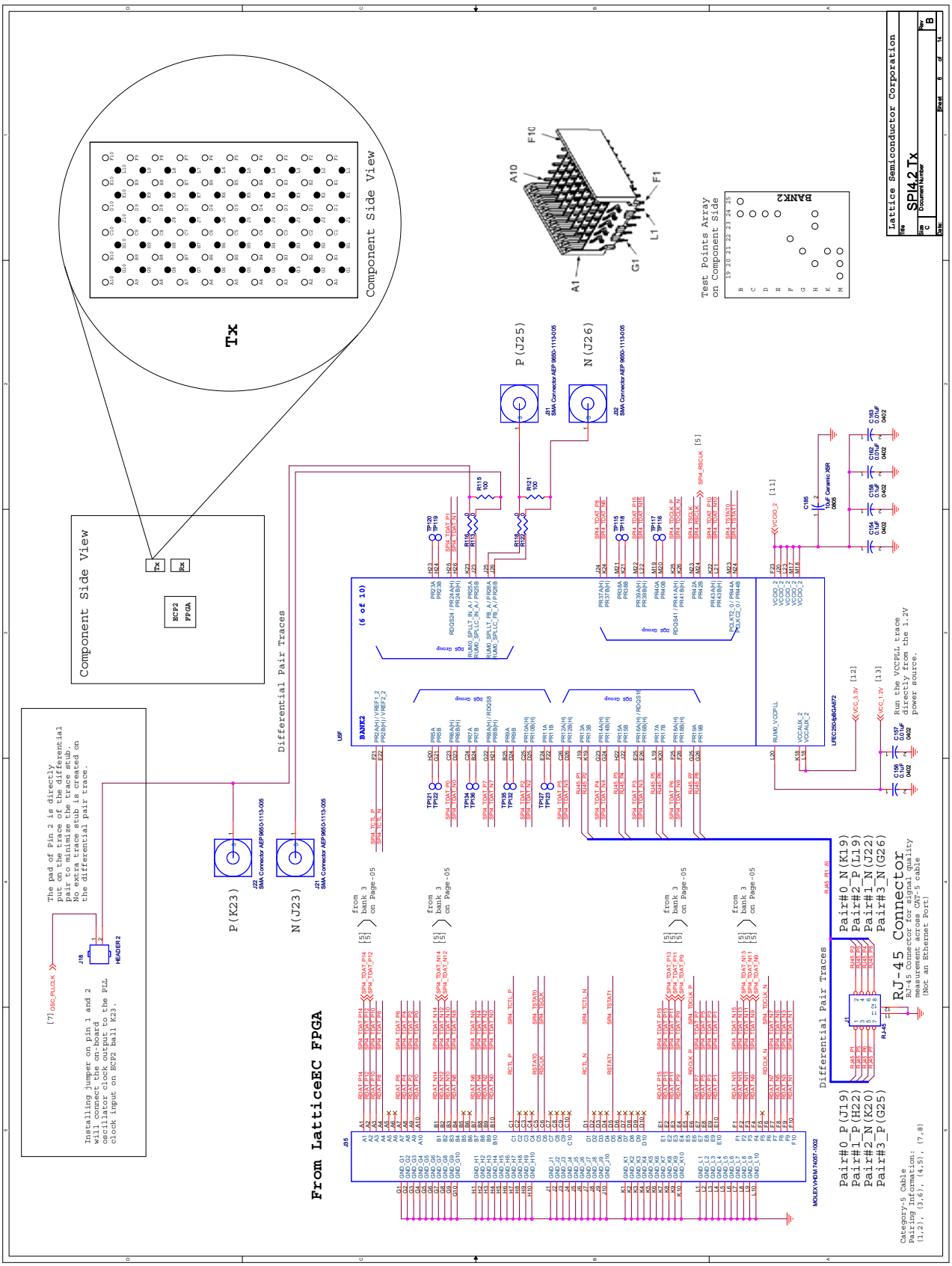


Figure 18. LCD, CF, IT EMF and OSC

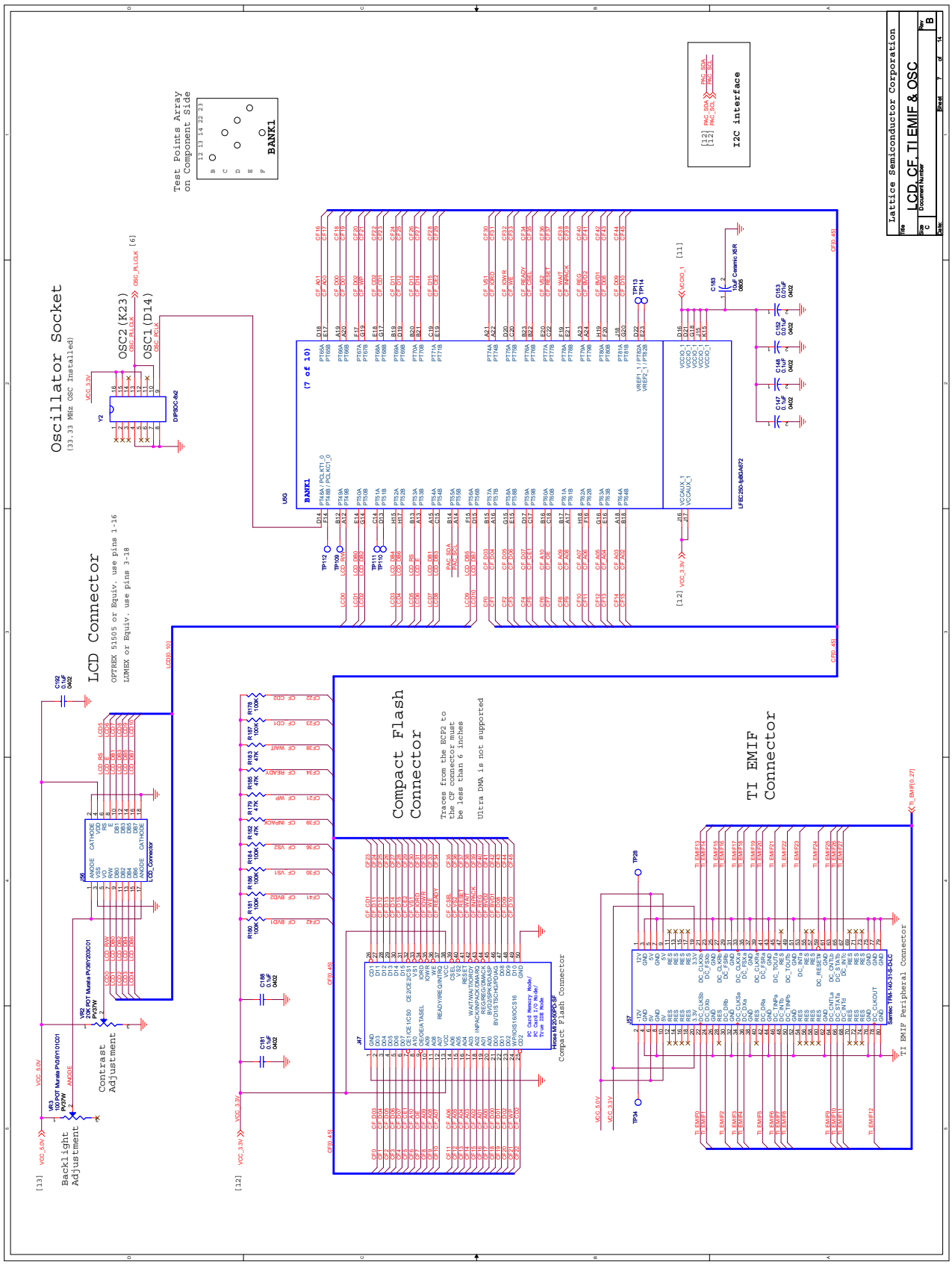


Figure 19. Ethernet

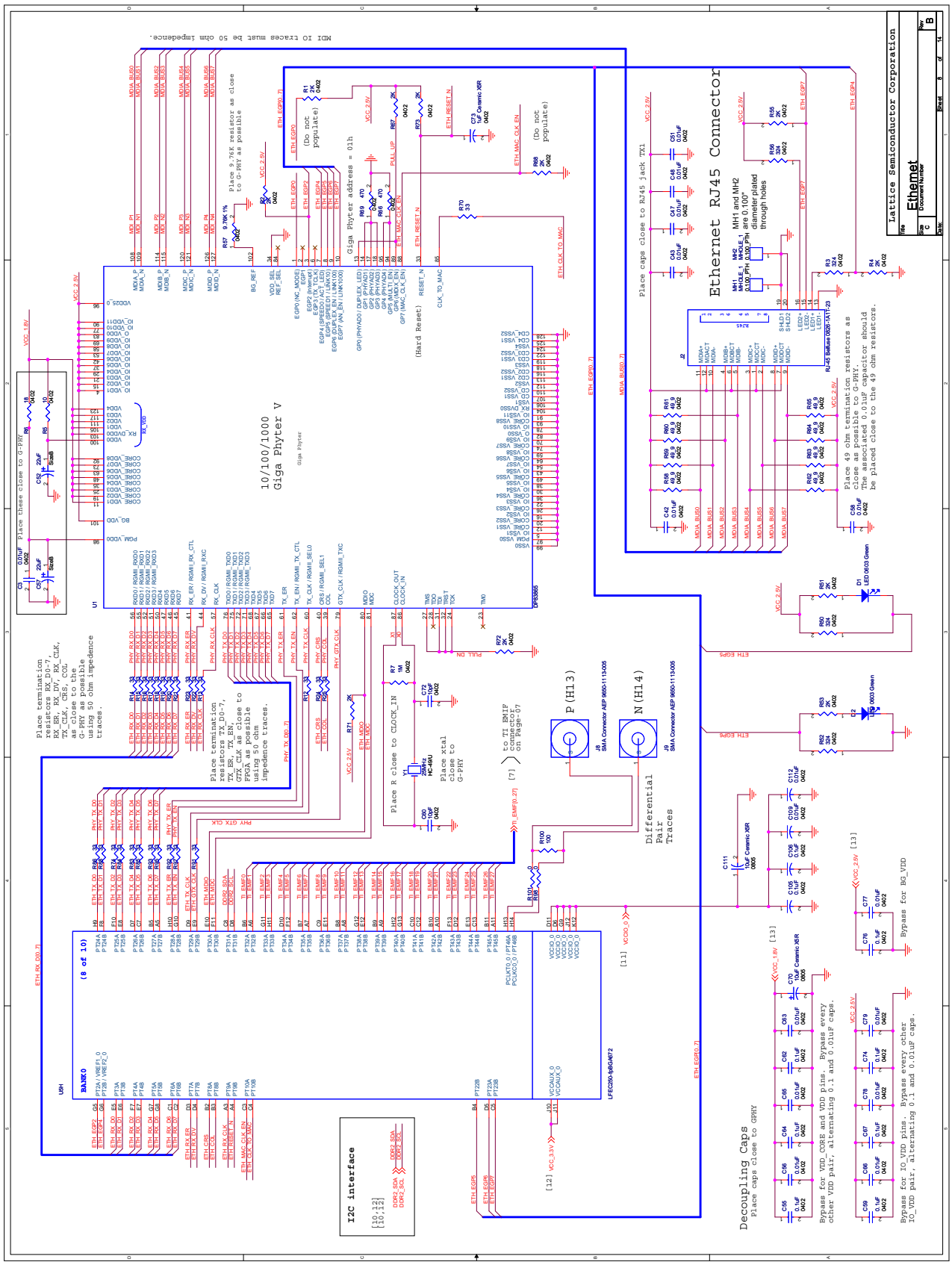


Figure 20. DDR2 SDRAM FPGA

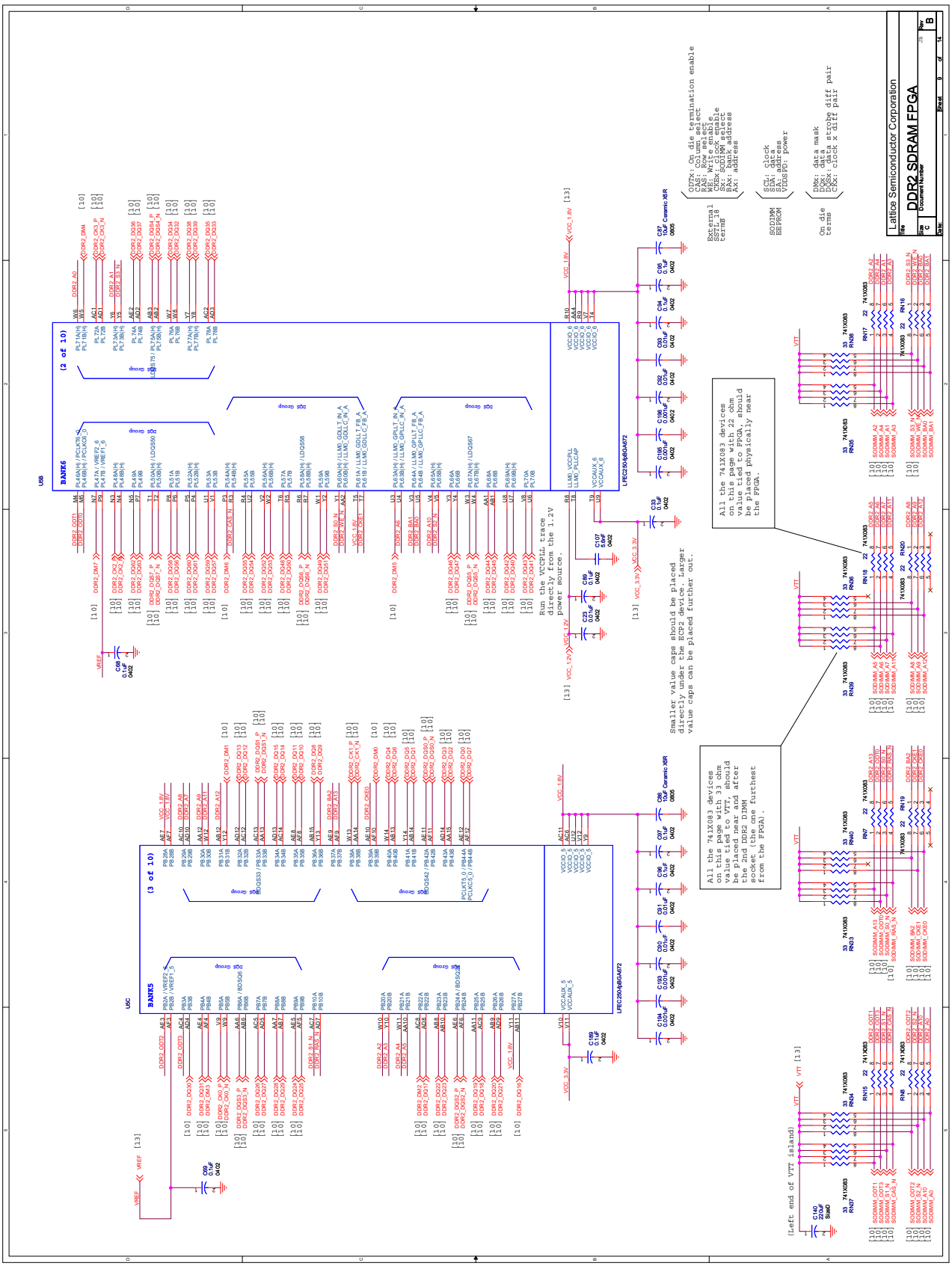


Figure 21. DDR2 SDRAM SO-DIMM

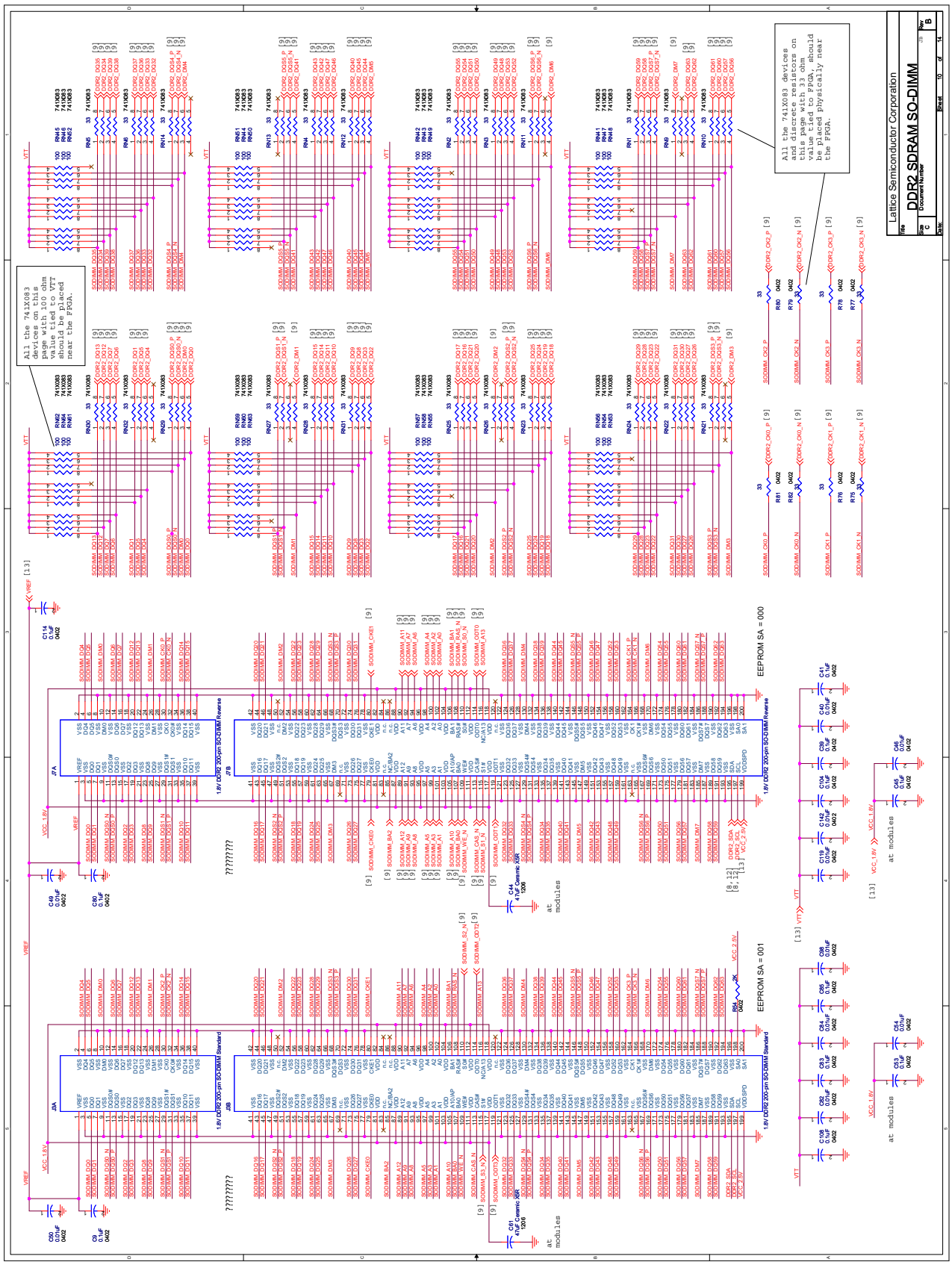


Figure 22. FPGA Power Pins

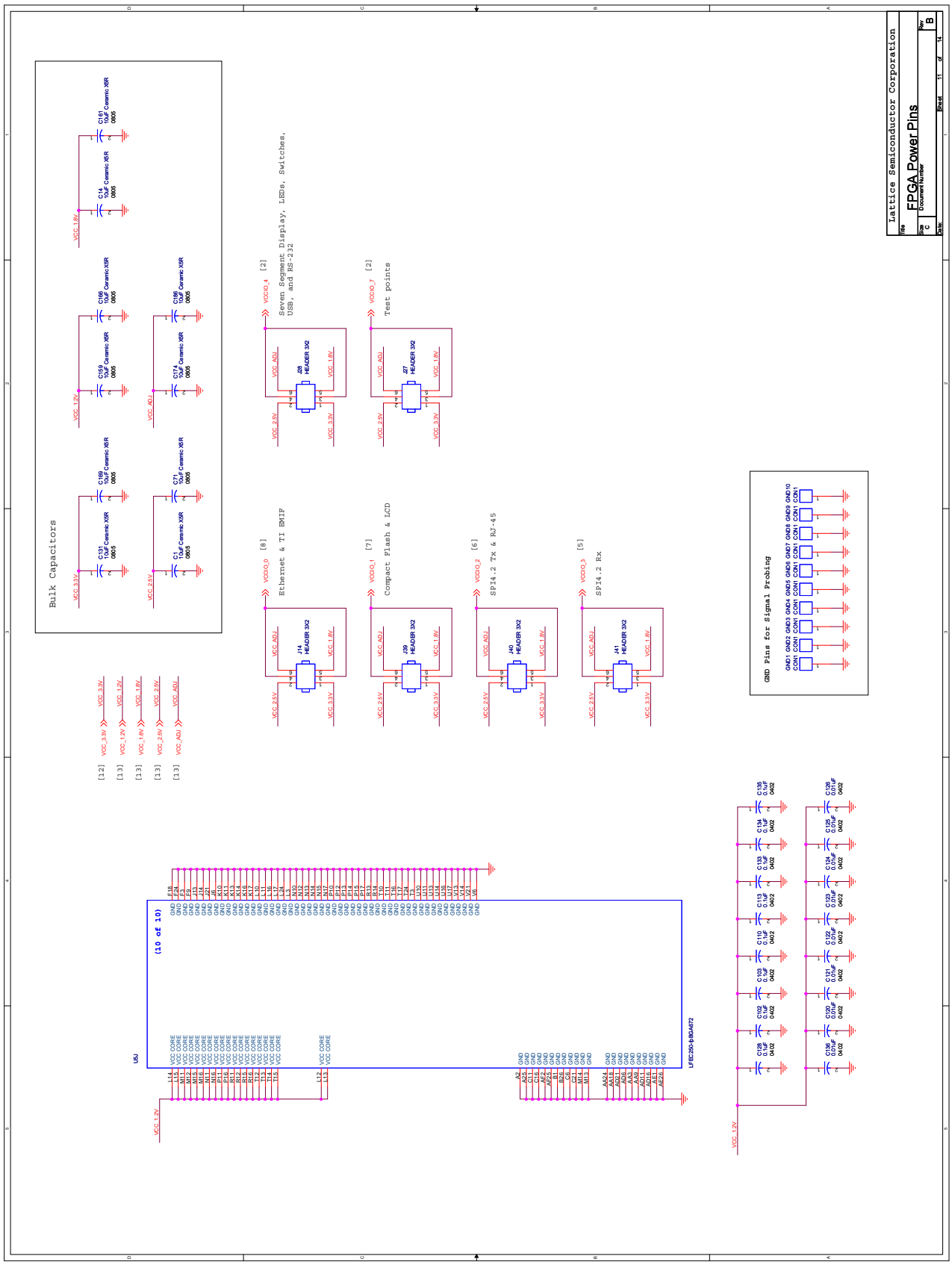


Figure 23. Power 1

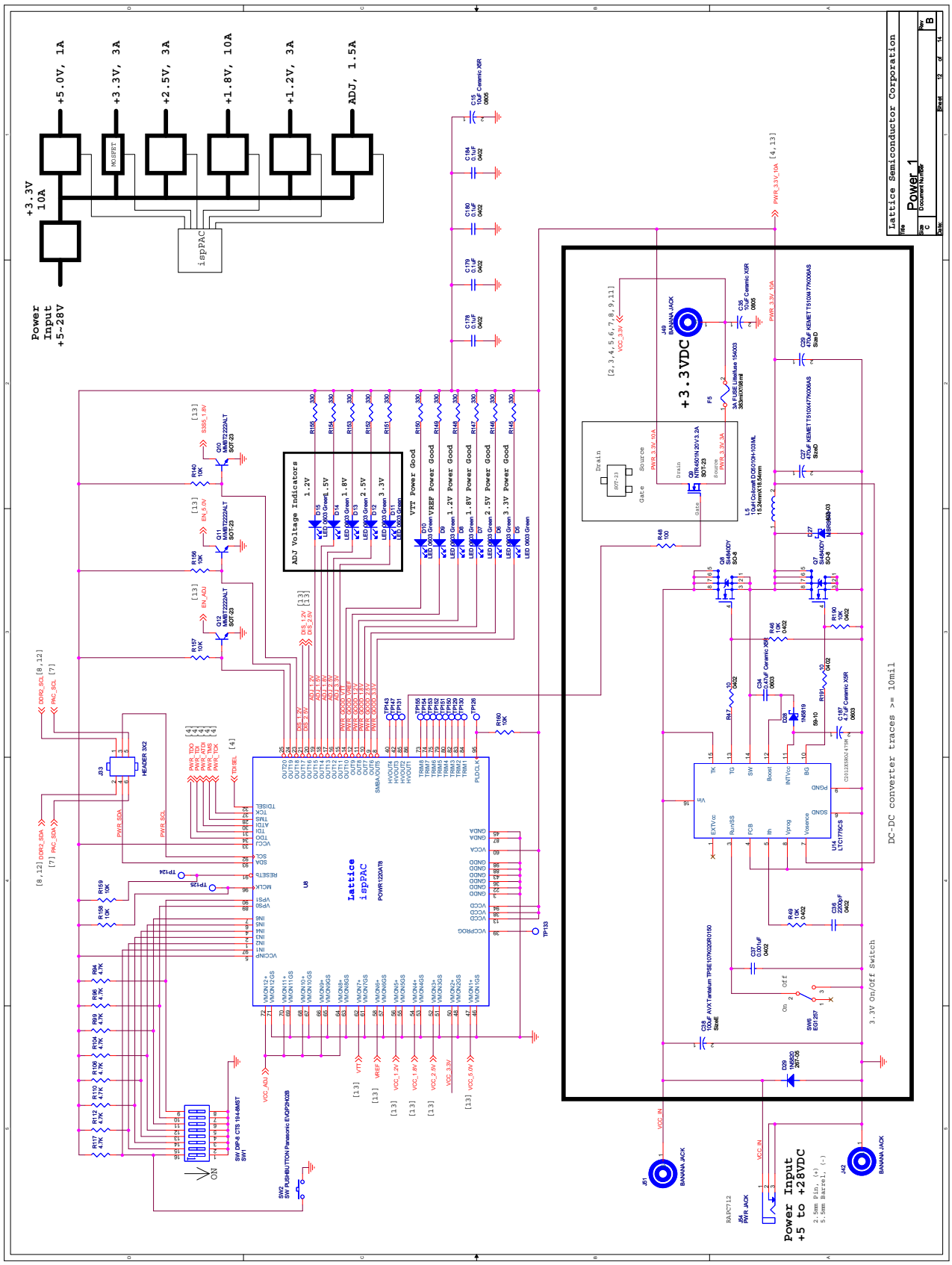


Figure 24. Power 2

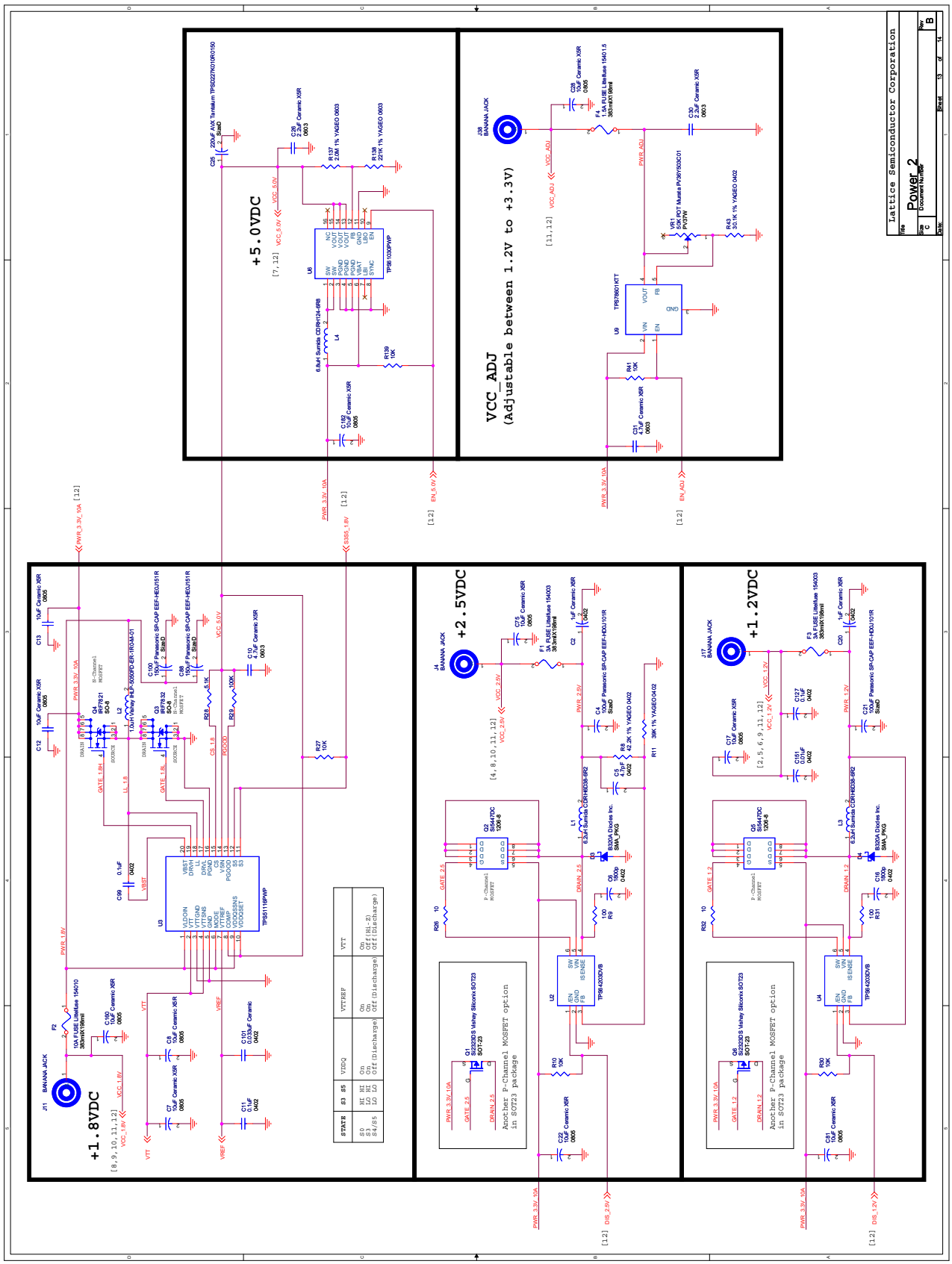


Figure 25. Placement and Dimensions (7.5" x 8.5")