Powering Up and Programming the ispPAC-POWR1014/A

April 2011 Application Note AN6075

Introduction

This application note discusses the states of the Power Manager II ispPAC®-POWR1014/A device's output pins — Open drain logic outputs (OUT3-OUT14) and HVOUT — during power-up, reset, and JTAG programming, as well as the states of these pins on a device that has not yet been programmed by the user. An understanding of this aspect of the device's operation is the key to designing systems that sequence supplies on in a dependable fashion. Suggested methods for interfacing to the enable pin of DC/DC converters and for performing in-system programming are also covered in this application note.

Power-on Reset

The ispPAC-POWR1014/A contains on-chip power-on reset circuitry to ensure that all parts of the device start up reliably, regardless of the VCC ramp rate. The device enters power-on reset when VCC is approximately 0.8V. VCC must reach a voltage greater than 2.5V for the device to exit power-on reset. During power-on reset, the output pins will go to the states shown in Table 23-1. After the device exits power-on reset, any brownouts that cause the VCC supply to dip below 2.5V will cause another power-on reset event to occur.

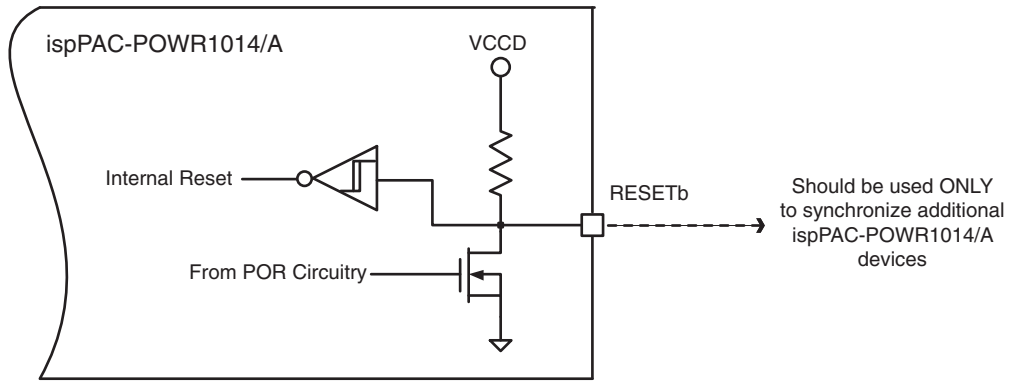
Table 23-1. Output States During Power-On Reset

Output Type	Power-on Reset State
OUT3-OUT14	High Impedance
HVOUT, Charge Pump Mode (as-shipped)	Pull-down
HVOUT, Open Drain Logic Output Mode	High Impedance

The ispPAC-POWR1014/A has a bi-directional reset pin (RESETb) whose only purpose is to synchronize the startup of multiple Power Manager II devices. Figure 23-1 shows an equivalent circuit for this pin; it is an open-drain output with a built-in pullup resistance to VCCD. If this pin is not being used to cascade multiple Power Manager II devices, it should be left unconnected.

Figures 23-2-23-5 illustrate the power-on reset behavior associated with logic outputs OUT3-14 and HVOUT pins that have been programmed to operate as open drain logic outputs. 2k Ohm pullup resistors to the VCCD pin were used on the logic output pins in all of the plots.

Figure 23-1. RESETb Pin Equivalent Circuit



Figures 23-2 and 23-3 show an open drain logic output pin that has been programmed to behave as a registered output. The difference between these two plots is that in Figure 23-2, the output has been programmed to reset to

a low level, whereas in Figure 23-3, it has been programmed to reset high. The power supply goes from zero to 3.3V in 20 milliseconds. The waveforms in Figures 23-2 and 23-3 are typical of VCC supplies that take more than a millisecond to reach 3.3V.

Figure 23-2. Startup with Slow Supply; Output Resets Low

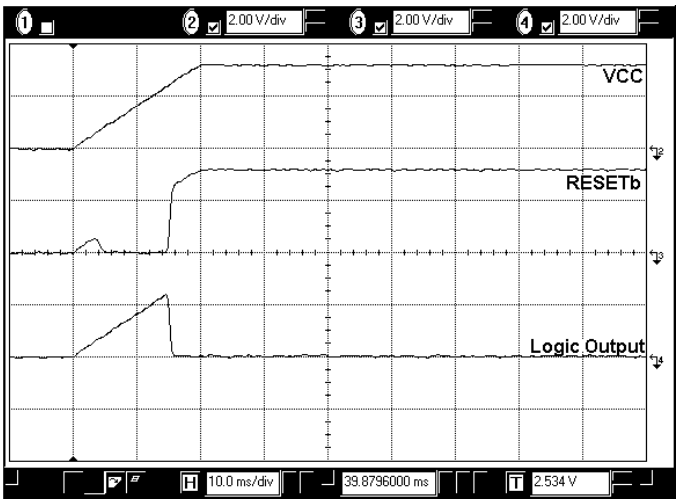
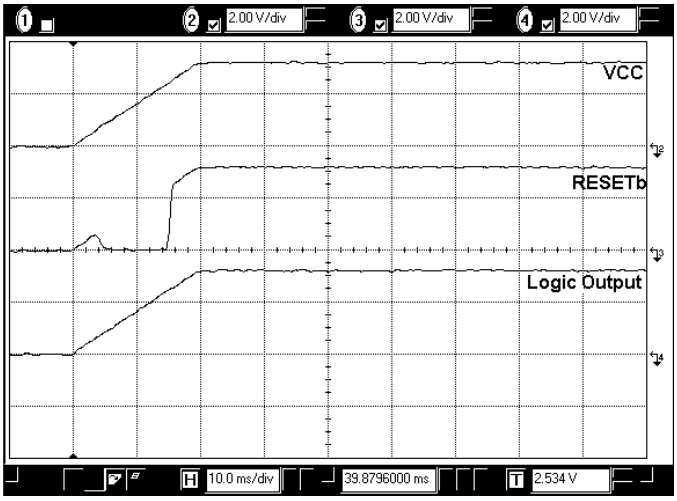


Figure 23-3. Startup with Slow Supply; Output Resets High



The behavior in both cases is identical until the time that VCC reaches 2.5V. RESETb pulls down starting at a VCC voltage of 0.8V; the RESETb output thus follows VCC up until this point. The open drain logic output retains its high impedance state until VCC reaches 2.5V; the voltage observed at the open drain logic output thus follows VCC to 2.5V. When VCC reaches 2.5V, power-on reset ends. From that point on, RESETb goes to a high level, and the logic outputs assume their programmed macrocell reset levels.

Figures 23-4 and 23-5 show the waveforms observed when the same device and setup that were examined in Figures 23-2 and 23-3 are powered from a supply that goes from 0 to 3.3V in 100 microseconds. Despite the faster power-up rate, RESETb still indicates that power-on reset starts when VCC reaches 0.8V. At this faster power-up rate, however, the time at which power-on reset ends is dominated by the time that it takes for the logic circuitry inside the ispPAC-POWR1014/A device to initialize, rather than occurring when VCC crosses 2.5V. Regardless of the VCC supply ramp rate, the low-to-high transition of RESETb indicates that the logic circuitry is ready to operate, and the outputs can be observed going to their programmed states.

Figure 23-4. Startup with Fast Supply; Output Resets Low

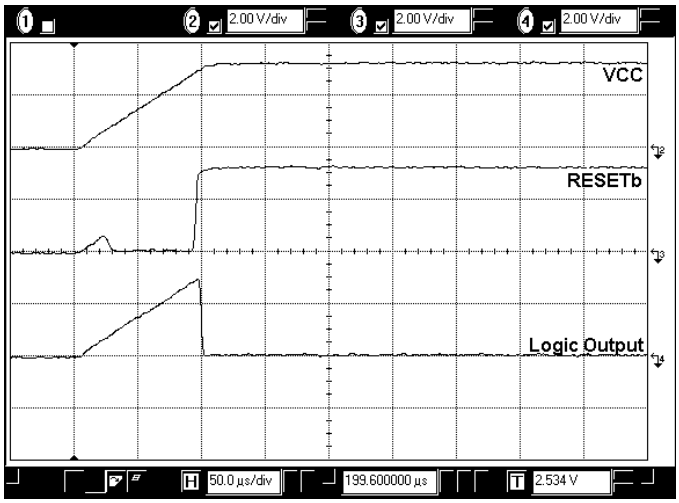
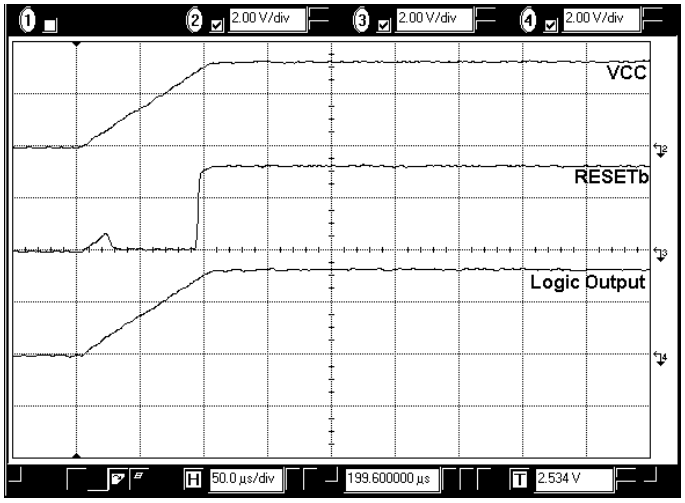


Figure 23-5. Startup with Fast Supply; Output Resets High



HVOUT pins that have been programmed for charge pump operation pull down during power-on reset regardless of the reset levels programmed into their associated macrocells. This is a safety feature that ensures that the external MOSFETs that these pins control will be off when the ispPAC-POWR1014/A begins its power supply sequencing operations.

An internal delayed reset signal, called AGOOD in PAC-Designer®, becomes true approximately 220 microseconds after RESETb goes high. AGOOD is an indication that all analog circuitry in the device is ready. Since the logic circuitry becomes available before the analog circuitry, PAC-Designer's LogiBuilder interface automatically inserts a "Wait for AGOOD" instruction at the beginning of each new sequence as a convenience. The user is given the freedom to insert new steps before the "Wait for AGOOD" instruction because sequencing tasks that depend purely on digital inputs can be performed before AGOOD becomes true.

Because all VMON comparator outputs will be low, regardless of the voltage at the VMON input pin, before the analog circuitry is ready, any supervisory logic window equations in which a low VMON comparator output indicates a failure condition will need to use AGOOD to block the comparator signal. For example, assume that two VMON inputs (Vin_5v and Vin_3v3) are being used to monitor rails not sequenced by this Power Manager device for brownout conditions and that if either of these rails browns out, the signal BROWN_OUT is to be driven low. If we program the supervisory logic equation

BROWN_OUT = Vin_5v AND Vin_3v3

the result will be that BROWN_OUT will pull low for about 220 microseconds following the release of RESETb, even if these voltage rails are within acceptable limits during that time. Modifying the above equation to

BROWN_OUT = (NOT AGOOD) OR (Vin_5v AND Vin_3v3)

prevents an indication of failure from being generated due to the analog circuitry not being ready. During that time, the expression NOT AGOOD will be true, forcing the output BROWN_OUT to be high.

User-initiated Resets

The ispPAC-POWR1014/A may be reset via I^2C or JTAG. **CAUTION:** The output pins will go to the states defined in Table 23-2 during a reset event, irrespective of the logic implemented.

Table 23-2. Output States During Reset

Output Pin	Reset State
OUT3 to OUT14	High-Z
HVOUT 1-2, FET Driver (as-shipped)	Discharge
HVOUT 1-2, Open-Drain	High-Z

At the conclusion of the reset event, the RESETb pin goes high. The OUT3 to OUT14 pins, as well the HVOUT pins go to their programmed levels at this time. AGOOD becomes true approximately 220 microseconds after RESETb goes high. The VMON comparators become operational when AGOOD becomes true.

Behavior During JTAG Programming

During JTAG programming, the RESETb pin goes to a low value, and the output pins go to the states defined in Table 23-3.

Table 23-3. Output States During JTAG Programming

Output Type	State During JTAG Programming
OUT3 to OUT14	High Impedance
HVOUT	Pull-down

HVOUT pins that were programmed for open drain logic operation temporarily change to FET driver mode during programming and pull down. This behavior ensures that any MOSFETs driven by these pins will stay off during programming. If the HVOUT pins are being used as open drain logic outputs, then it is recommended that power be supplied only to the ispPAC-POWR1014/A through VCCJ and VCCPROG during in-system programming. Strategies for doing this are covered in a later section of this application note.

Shipped State of New Parts

ispPAC-POWR1014/A devices are programmed during factory testing with a sequence known as the “as-shipped” state. The output pins of devices in the as-shipped state will assume the states defined in Table 23-4 once power-on reset is completed. The I^2C address of devices in the as-shipped state is 0.

Table 23-4. Output Functions of Device As-Shipped from Lattice Semiconductor

Output Pin	As-Shipped State
OUT3-14	High-Z
HVOUT 1&2	Discharge (FET driver mode)
MCLK	High-Z (Standalone clocking mode)
PLDCLK	Enabled

Ensuring Reliable Operation at Power-up

Power supply systems using the ispPAC-POWR1014/A should be designed such that a high impedance state on a given logic output disables the supply controlled by that pin. Supplies with negative enable logic – that is, ones in which pulling the enable pin to ground turns the supply on – can often be connected directly to the open drain output pins without any additional components. For supplies with positive enable logic, the circuit in Figure 23-6 should be used. In both cases, the DC/DC converter data sheet should be checked to see whether its enable input has a built-in pullup resistor or whether an external resistor must be used. Tables 23-5 and 23-6 list the values that should be used in the LogiBuilder OUTPUT instructions and the reset levels that should be selected in the "PINS" window for supplies with positive and negative enable logic, respectively.

Figure 23-6. Interfacing to Supplies with Positive Enable Logic

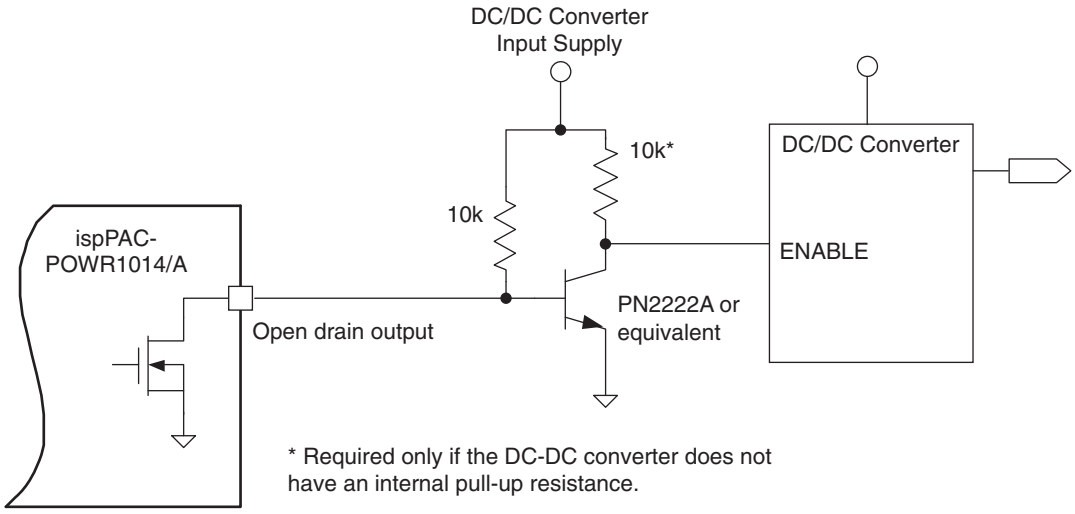


Table 23-5. Controlling Positive Logic Supplies

Interface Method	"PINS" Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Use Inverter Circuit (Figure 23-6)	HIGH	0 (Deassert)	1 (Assert)

Table 23-6. Controlling Negative Logic Supplies

Interface Method	"PINS" Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Connect Directly to Open-Drain Output	HIGH	0 (Deassert)	1 (Assert)

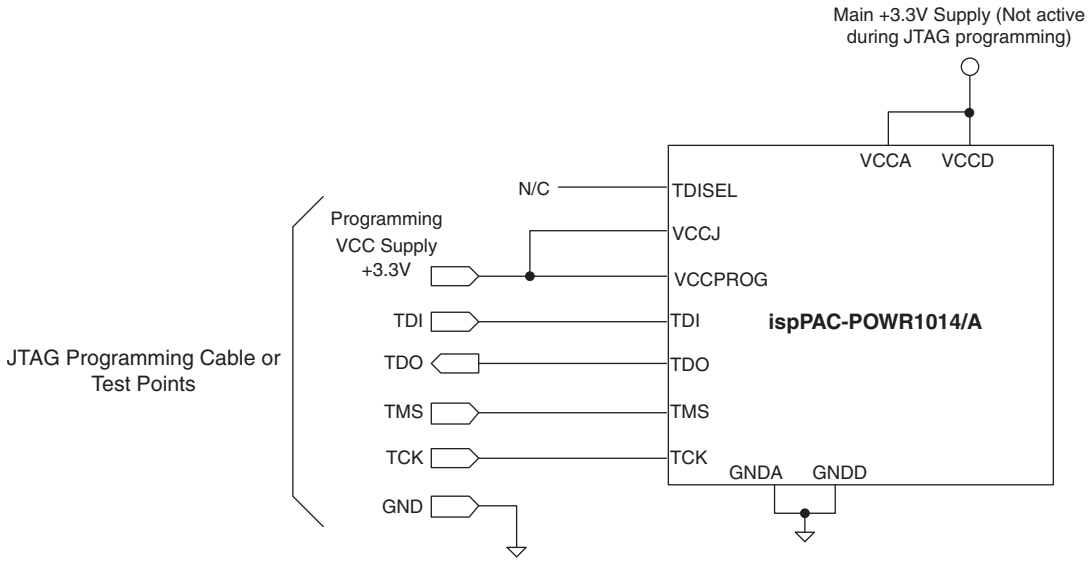
In-System Programming with the ispPAC-POWR1014/A

The ispPAC-POWR1014/A provides several different modes of programming, in relation to how it is powered. Using the standard method of powering VCCD, VCCA and VCCJ, the device can be programmed as powered up normally and the device output pins will respond to the programming as noted in Table 23-3. After the program is complete, the device is ready to start its sequence.

The second method is for programming just the ispPAC-POWR1014/A, without powering up the PLD macrocells, I/O or I^2C circuitry. This method allows the user to power up just a portion of the device for programming without powering up the whole board or affecting other devices and supplies in the system. This is achieved by powering VCCPROG and VCCJ only. A simple low power external 3.3V supply is needed to supply power to VCCPROG and VCCJ as shown in Figure 23-7. In this mode the HVOUT pins will be low and the OUT3-OUT14 will be in a high

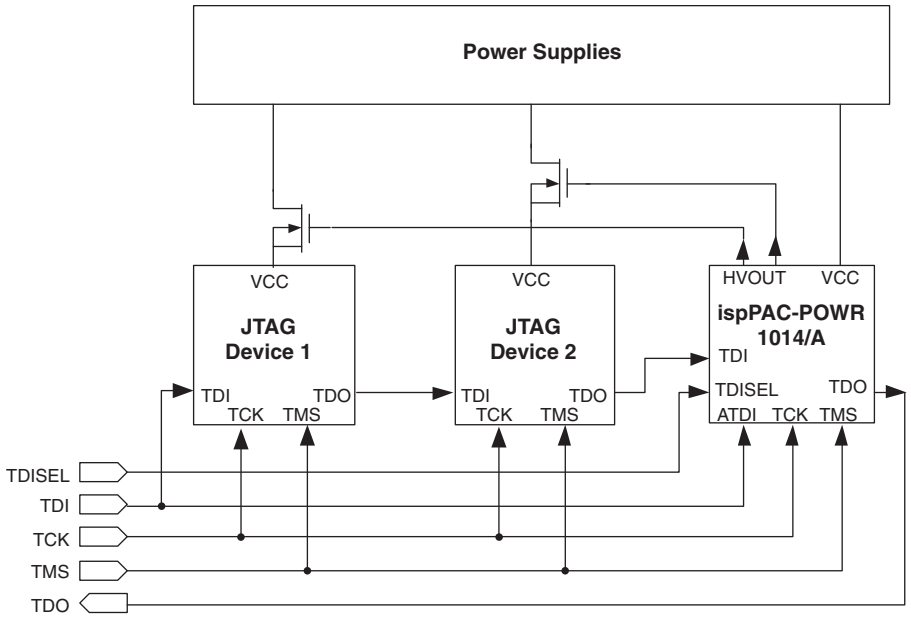
impedance state. Once programming is complete, remove the VCCPROG supply and power up with VCCA, VCCD, and VCCINP. To enable normal JTAG operations, power should be applied to VCCJ and can be separated from VCCPROG with a jumper or Schottky diode.

Figure 23-7. Powering Through VCCPROG and VCCJ During Programming



To have the device fully powered up during programming, power should be applied to VCCJ, VCCD, and VCCA, but not VCCPROG. This is the strategy that must be used if it is desired to initiate a test sequence via JTAG (by writing to the register associated with IN1) after programming is complete. Frequently, other JTAG devices on the board, such as FPGAs, have their power sequenced on by the ispPAC-POWR1014/A. Ideally, the design should be achievable using only one JTAG chain. The ispPAC-POWR1014/A provides an alternate TDI JTAG input feature that makes this goal achievable. By using the ATDI pin, as shown in Figure 8, the unpowered devices in the chain can be bypassed while the ispPAC-POWR1014/A is being programmed. TDISEL should be pulled to ground during programming of the Power Manager II device in order to select the ATDI input. All JTAG devices in the chain must be hot-socket compatible to guarantee that the TMS and TCK signals are not clamped. For a more detailed treatment on programming using the ATDI input, please refer to AN6068, Programming the ispPAC-POWR1220AT8 in a JTAG Chain Using the ATDI Pin. The operation of the ATDI feature on the ispPAC-POWR1014/A is identical to that on the ispPAC-POWR1220AT8.

Figure 23-8. Using ATDI to Bypass Unpowered Devices



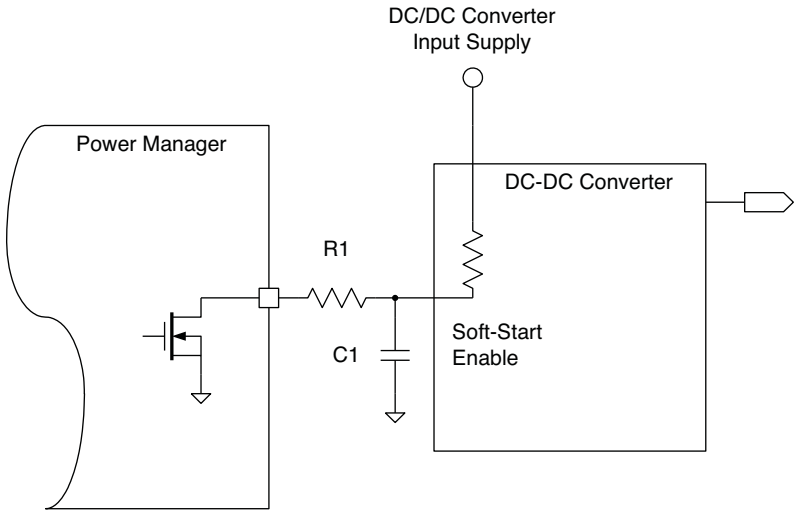
Non hot-socket compliant devices may share a JTAG chain with the ispPAC-POWR1014/A if these devices have a separate VCCJ power supply pin. Power must be applied to the VCCJ pins on these devices while programming the ispPAC-POWR1014/A in order to prevent clamping of the TMS and TCK signals. These devices can be bypassed by using the ATDI feature.

Capacitive Loading on Outputs

In certain applications, the outputs of the Power Manager device are used to enable the soft-start feature of a DC-DC converter. This presents a capacitive load to the outputs of the Power Manager. During the power-up cycle of the Power Manager, the open-drain outputs will transition from active low to high-z. Likewise, the HVOUT pins will transition from active low to discharge (or high-z depending on the configuration) during the power-up cycle. If the soft-start capacitors have any charge stored during this time, excessive currents will flow through the open-drain outputs to ground. These currents can result in an unreliable start-up of the Power Manager. Furthermore, during normal operation setting an output low can also result in a discharge current that exceeds the maximum current limits in the data sheet.

To ensure reliable Power Manager start-up and to limit the current surge it is required to add a series resistor when a capacitive load is connected to an output as shown in Figure 23-9. The value of R1 should be such that when C1 is discharged by the open-drain output the current is less than the $I_{SINKMAXTOTAL}$ limit in the data sheet. The $I_{SINKMAX-TOTAL}$ is for any single output and is found in the Absolute Maximum Ratings Table of the data sheet. If multiple outputs have capacitive loads the $I_{SINKTOTAL}$ Max should also be considered in setting a value for the series resistors. The $I_{SINKTOTAL}$ number is found in the Digital Specifications table of the data sheet and applies to all outputs combined.

Figure 23-9. Limiting Capacitive Load Currents to Less than $I_{SINKMAXTOTAL}$



Summary

The startup characteristics of the open drain logic outputs (OUT3 to OUT14) and the HVOUT pins as a function of the power-on reset condition have been described. The behavior of these outputs has also been defined during user-issued resets and during JTAG programming. The programmed state in which new devices are shipped from the factory (the “as-shipped” state) has been described.

To ensure reliable startup of power supplies, the ispPAC-POWR1014/A’s logic outputs should be set up so that a logic low activates the supplies. Supplies that use positive enable logic require a simple one-transistor inverter to interface to the ispPAC-POWR1014/A’s open drain logic outputs.

Strategies to perform in-system programming by applying power only to VCCJ and VCCPROG are strongly suggested. An example was presented showing a system in which the ispPAC-POWR1014/As JTAG interface is shared between a JTAG programmer and an on-board JTAG chain that uses the device’s non-programming JTAG capabilities.

When outputs are driving a capacitive load a series resistor is required to insure the discharge current is below the current limits in the data sheet.

Related Literature

- ispPAC-POWR1014/A Data Sheet
- AN6068, Programming the ispPAC-POWR1220AT8 in a JTAG Chain Using the ATDI Pin

Technical Support Assistance

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Revision History

Date	Version	Change Summary
March 2006	01.0	Initial release.
April 2011	01.1	Updated to address capacitive loading on the outputs.