BSCAN2 – Multiple Scan Port Linker

Reference Design

FPGA-RD-02106-4.9

December 2019

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1. Introduction

According to the IEEE 1149.1 Boundary Scan System, every complex system can have more than one boundary scan compliant scan port. This design adds the capability of linking these multiple scan ports dynamically. The Multiple Scan Port (MSP) device can be used to link the Local Scan Paths (LSP) or it can be completely bypassed. The four local scan ports, or any combination of these four ports, can be selected by entering the necessary data into the instruction and data registers.

2. Functional Description

The MSP is comprised of four major logic blocks (Figure 2.1.). The Port Control block is responsible for controlling the operation of the instruction register and data register. The Instruction Register and Data Register blocks shift and load one instruction register and three data registers. The Scan Port Configuration block links any combination of the four secondary scan ports.

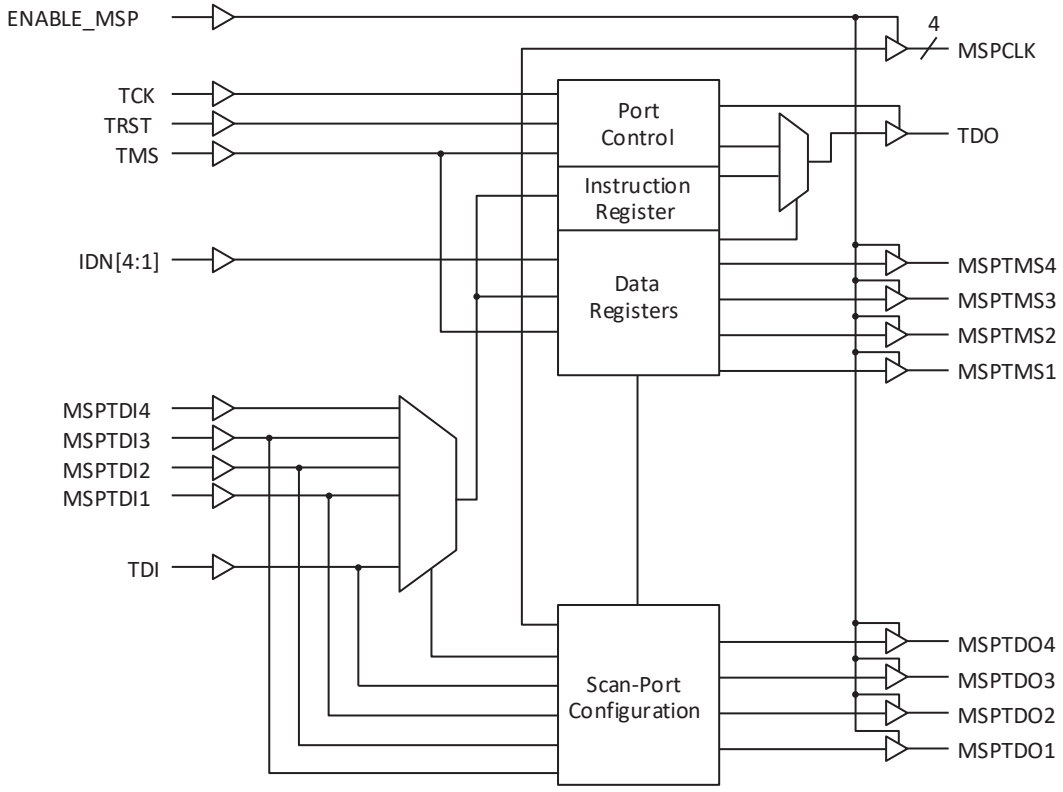

Figure 2.1. BSCAN2 Block Diagram

The value in any of the registers is loaded in such a way that the least significant bit (LSB) is the first to be shifted in closest to the TDO and the most significant one (MSB) is the last and closest to TDI.

Table 2.1. Pin List

Pin	I/O	Description
TCK	I	Test Clock – All operations are synchronous to TCK. Input values are captured on the rising edge, while outputs are updated on the falling edge.
TMS	I	Test Mode Select – TMS values determine the next state for the TAP controller state machine.
TDI	I	Test Data Input – Serial input to shift data into the data and instruction registers.
TRST	I	Test Reset – Active low signal, asynchronously resetting the TAP controller to the Test-Logic Reset state.
TDO	O	Test Data Output – Serial output from the data and instruction registers. Active during the Shift-IR and Shift-DR states.
IDN 1:4	I	Identification – Port to allow definition of a user-defined ID, which can be read using the appropriate instruction. In case of chaining BSCAN2 top_linker modules, each instance should have a unique IDN.
MSPTCK 1:N	O	Multiple Scan Port TCK – TCK buffered output driven to each local scan chain.
MSPTMS 1:N	O	Multiple Scan Port TMS – The value of TMS is driven to each local scan chain when enabled.
MSPTDI 1:N	I	Multiple Scan Port TDI – Serial data received from the local scan chain.
MSPTRST 1:N	O	Multiple Scan Port TRST – TRST buffered output to reset all local scan ports.
MSPTDO 1:N	O	Multiple Scan Port TDO – Serial data output to the local scan chain.
Enable_MSP	I	Global Output Enable for all local scan chains – When low, the device outputs are tri-stated, allowing independent control from a source such as a Lattice ispDOWNLOAD™ Cable.

Note: Supported values for N are currently 4 and 8.

The test port consists of three signals: TMS, TCK and TRST and includes a TAP controller that adheres to the IEEE Standard 1149.1 protocol. This port controls the operation of the circuit by issuing the proper control instructions to the data registers. The state diagram for the TAP controller is shown in Figure 2.2.

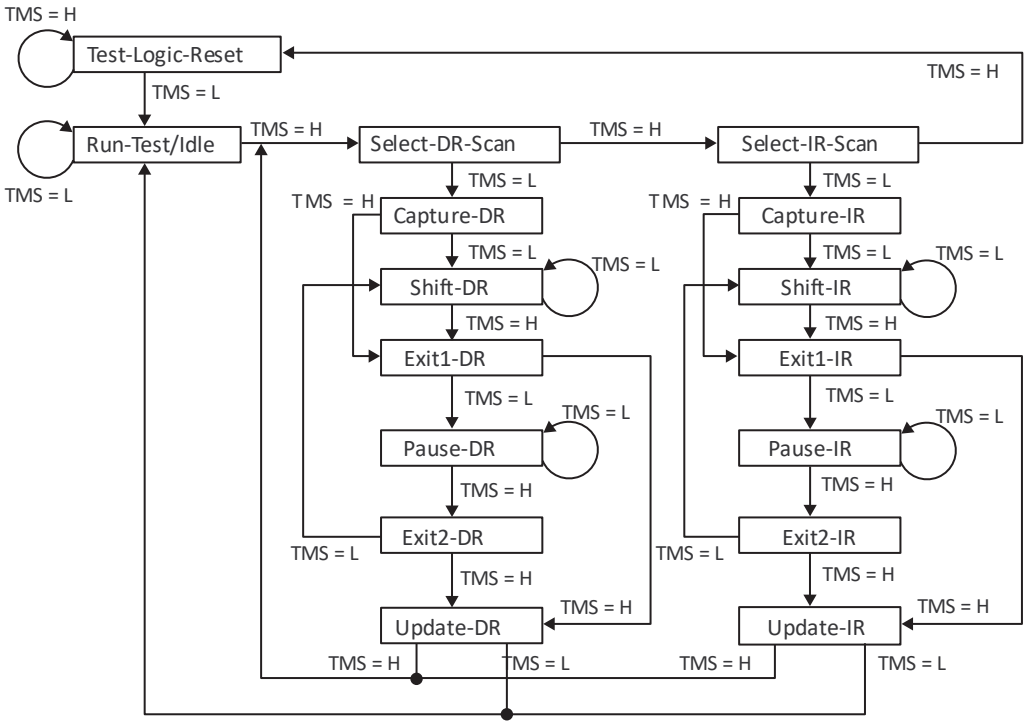

Figure 2.2. TAP Controller State Machine

The device is controlled by instructions loaded into one 8-bit-wide serial shift register known as the Instruction Register. Data is shifted in via the TDI pin and out through the TDO pin.

Table 2.2. BSCAN2 Registers

Register Name	Type	Size
INSTRUCTION	IR	8
SELECT	DR	8
ID BUS	DR	4
BYPASS	DR	1

Table 2.3. lists the instructions implemented in the MSP and the data register selected by each instruction.

Table 2.3. BSCAN2 Instructions

Instruction	Data Register	Instruction
11111100 (FC)	ID Bus	SCANIDB
01111101 (7D)	ID Bus	READIDB
01111110 (7E)	Select	SCANSEL
All Others	Bypass	BYPASS

2.1. Select Register

The Select Register (SR) is an 8-bit serial register that determines which, if any, of the local scan paths (LSPs) will be active. Assertion of TRST or entry into the Test-Logic-Reset TAP controller state forces all bits to zero. The register is divided into four 2-bit sections, each controlling one LSP. Table 2.4. shows the SR bits controlling the operation of MSPTMS and MSPTDO.

Table 2.4. Select Register Mapping

Bit	7	6	5	4	3	2	1	0
Function	EN	MS	EN	MS	EN	MS	EN	MS
Port	LSP4		LSP3		LSP2		LSP1	

Table 2.5. Port Control via the Select Register

EN	MS	MSPTMS	MSPTDO
0	0	H	Z
0	1	L	Z
1	X	TMS	Active

2.2. ID Bus Register

During the SCANIDB IR operation, the ID register is placed in the scan path and preloaded with data from the IDN[1:4] pin during the rising edge of TCK in the Capture-DR state.

During the READIDB IR operation, the ID register is placed in the scan path but is not preloaded in the Capture-DR TAP state.

2.3. Bypass Register (BR)

The Bypass Register is a 1-bit serial register used to reduce the length of the scan path. When the Instruction Register is loaded with the Bypass instruction, data passes to the scan port unmodified during the Shift-DR TAP state.

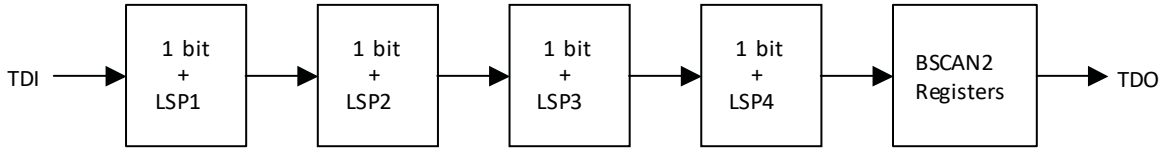

Figure 2.3. LSP Order (All Ports Selected)

Note: Any local scan port (LSP) may be bypassed. However, the BSCAN2 register is always active.

3. Larger BSCAN2 Implementations

For compatibility with multiple test system platforms, two distinct models are created to implement the BSCAN2 Linker with more than four ports. These models are similar in operation, with a few notable exceptions.

The first 8-port BSCAN2 is implemented by daisy chaining two BSCAN2 blocks. The logical representation of this is shown in Figure 3.1.

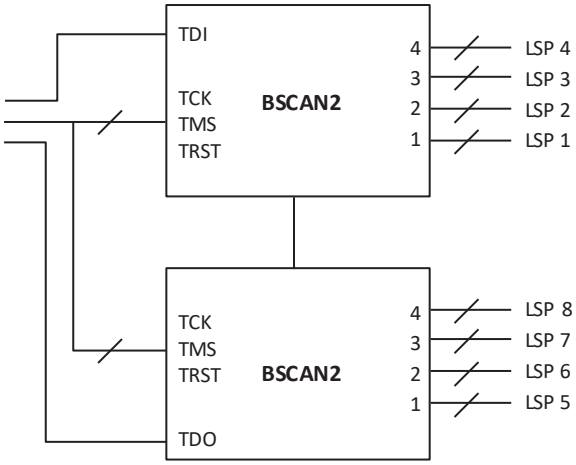

Figure 3.1. 8-port BSCAN2 Implementation via Daisy Chaining

This model is used for compatibility with boundary scan test tools from JTAG Technologies®.

The key difference in this model is the existence of two sets of data and instruction registers. Each BSCAN2 block also contains the 4-bit identification register, which are both connected to the external IDN[4:1] bus.

The Select register mapping for this model is shown in Table 3.1.

Table 3.1. 8-Port BSCAN2 Select Register Mapping (JTAG Technologies Model)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS
Port	LSP4		LSP3		LSP2		LSP1		LSP8		LSP7		LSP6		LSP5	

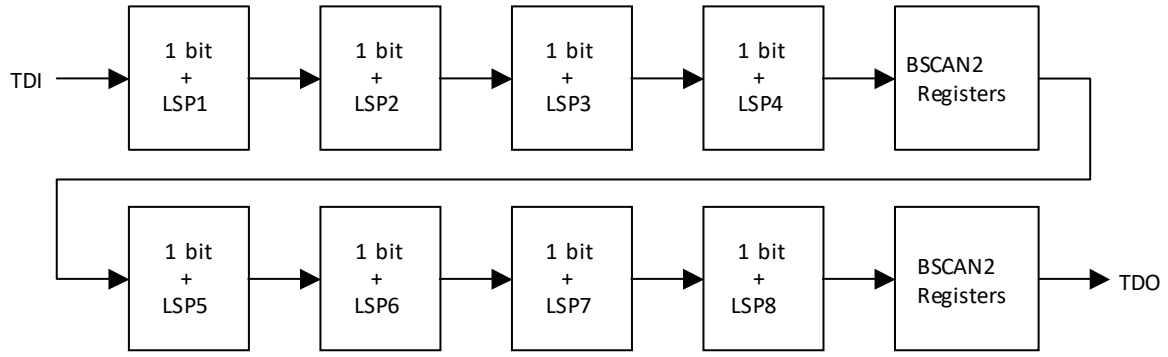

Figure 3.2. BSCAN2 x 8-Port (JTAG Technologies Model) LSP Order (All Ports Selected)

Note: Any local scan port (LSP) may be bypassed. However, the BSCAN2 registers are always active.

The second and final 8-port BSCAN2 is implemented by integrating the additional ports into the existing BSCAN2 register structure. Only the size of the Select register is increased. The logical representation of this model is shown in Figure 3.3.

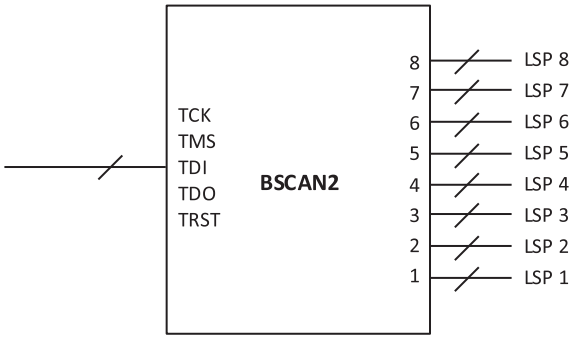

Figure 3.3. Integrated 8-Port BSCAN2 Implementation

This model is implemented in Asset Intertech® boundary scan tools.

Table 3.2. 8-port BSCAN2 Select Register Mapping (Asset Model)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Function	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS	EN	MS
Port	LSP8		LSP7		LSP6		LSP5		LSP4		LSP3		LSP2		LSP1	

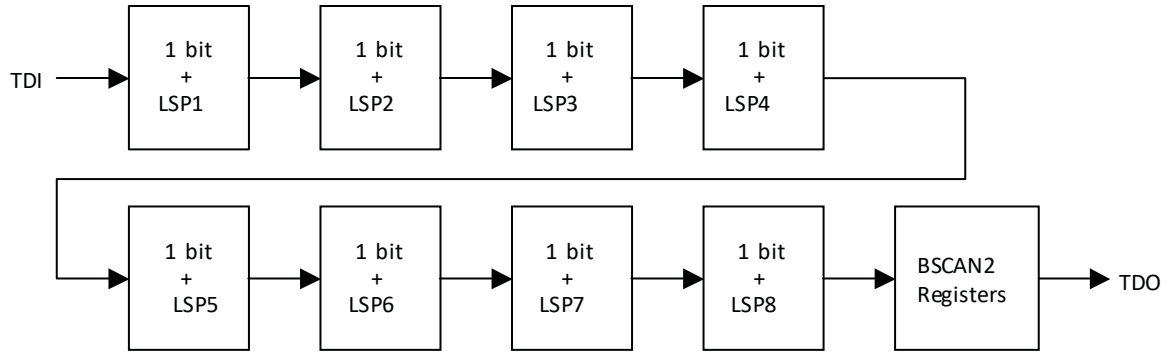

Figure 3.4. BSCAN2 x 8-Port (Asset Model) LSP Order (All Ports Selected)

Note: Any local scan port (LSP) may be bypassed. However, the BSCAN2 register is always active.

3.1. BSCAN2 Operation Using ispVM™ System Software

ispVM System can be used in conjunction with BSCAN2 to program Lattice devices within any of the local scan ports.

Note: The following procedures assume familiarity with ispVM System. For more information on using ispVM System, please refer to the tutorials included within the Help system.

ispVM System (14.3.2 and later) includes a BSCAN2 utility to configure the Select register to activate specified local scan ports.

1. Connect an ispDOWNLOAD cable to the BSCAN2 device JTAG signals and apply power to all applicable devices.
2. Open the utility, found in the ispTools menu (**ispTools > BSCAN Config**). Choose the appropriate implementation. The resulting dialog will look similar to Figure 3.5.

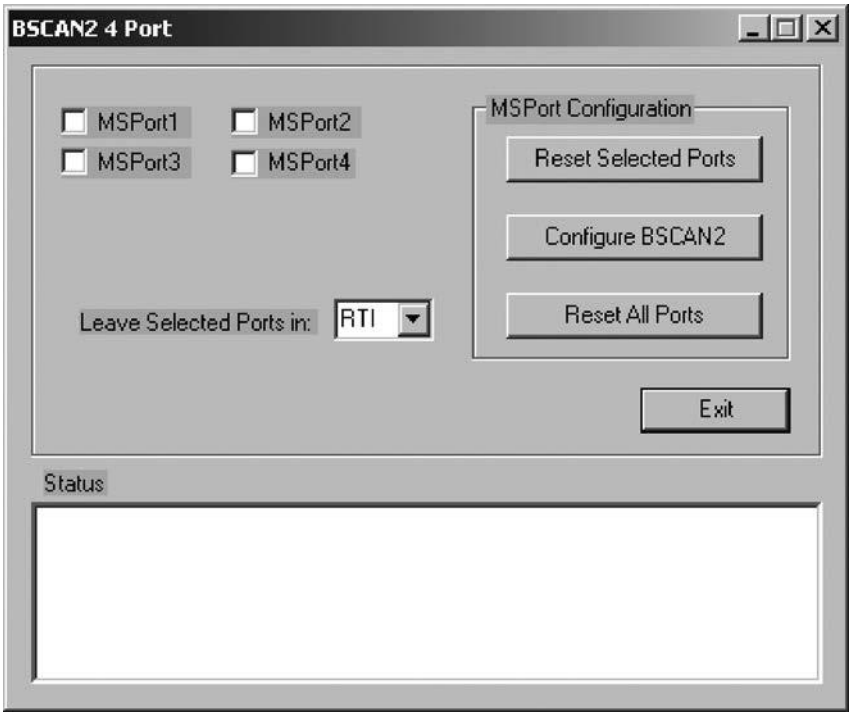

Figure 3.5. BSCAN2 Configuration Dialog (4-Port Implementation)

3. Press the Reset All Ports button to initialize all devices into the same state.
4. Select the desired local ports by placing a check mark in the corresponding check boxes.
5. Press the Configure BSCAN2 button. The command is then sent to the BSCAN2 device and the Select register is loaded with the corresponding values.

Chain Setup

- Create a new chain file and insert the devices that represent the entire chain you wish to access.

Note: The SCAN function cannot be used, since it would force a Test-Logic Reset of the BSCAN2 device, clearing the Select register.

- Active ports always have a one-bit synchronization register at the beginning of the local port. This should be represented with a JTAG-NOP device with an instruction register length of '1', as shown in Figure 3.6.

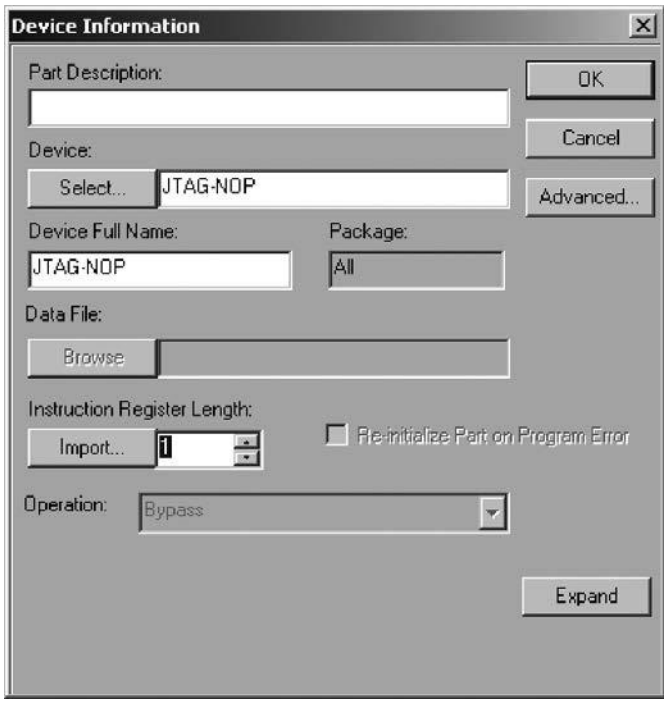

Figure 3.6. Representation of the Synchronization Bit

- The BSCAN2 Bypass register is always the last device in the entire chain. It should be represented as a JTAG-NOP device with an instruction register length of '8'.
- For the daisy chained 8-port BSCAN2 implementation (JTAG Technologies model), two Bypass registers are present in the complete chain. They should be positioned after LSPs 4 and 8.
- ispVM System must be configured to avoid the Test-Logic Reset (TLR) state. When the TLR state is reached, the Select register is cleared, deactivating all ports. Two options under the **Projects -> Project Settings** dialog must be set: **Disable Board Setup Checking** and **Avoid Test Logic Reset**, as shown in Figure 3.7.

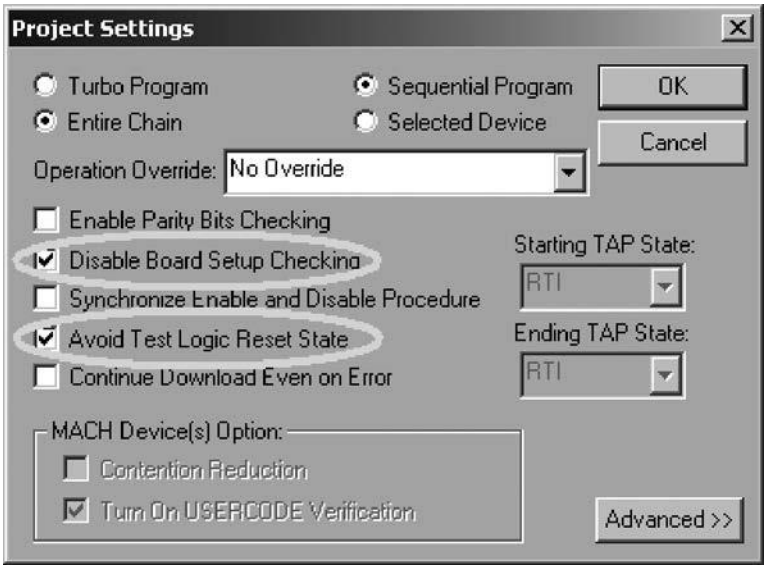

Figure 3.7. Project Settings for BSCAN2 Compatibility

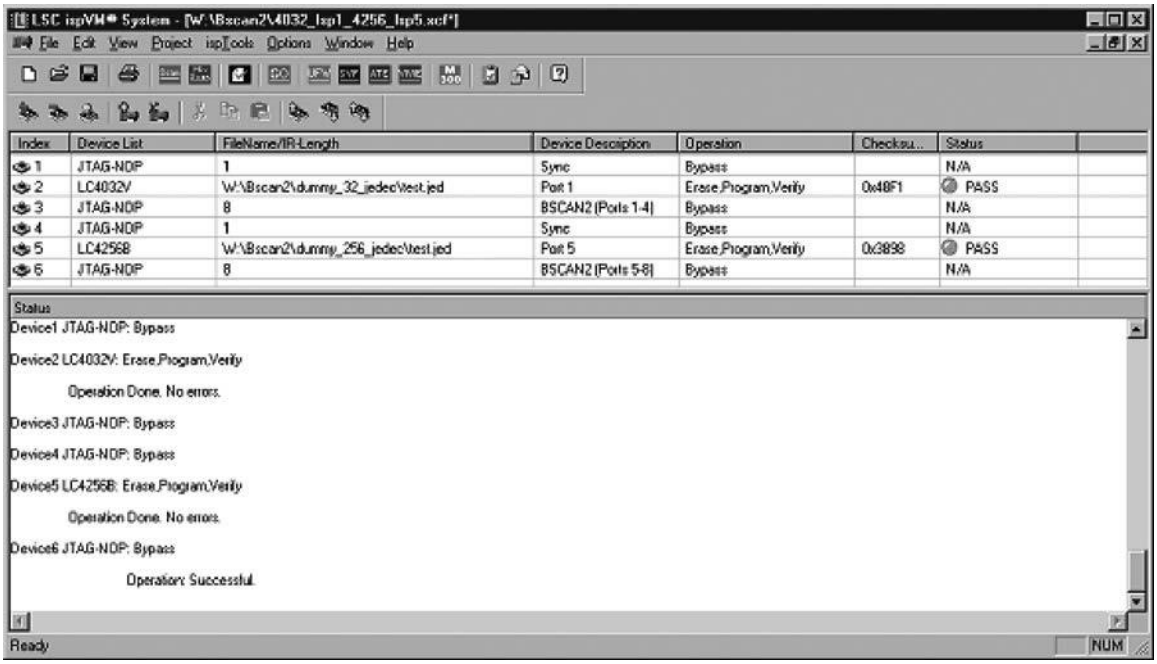

Figure 3.8. Example Chain Configuration for 8-Port BSCAN2 (JTAG Model) with Ports 1 and 5 Activated

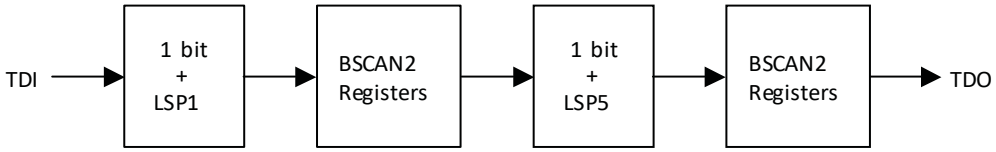

Figure 3.9. Logical Representation of ispVM Chain Configuration

4. Implementation

This design is implemented in Verilog and VHDL. When using this design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 4.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
4-Port Implementation						
MachXO2™ [1]	Verilog	–4	88 LUTs	>30	30	N/A
	VHDL	–4	85 LUTs	>30	30	N/A
MachXO™ [2]	Verilog	–5	88 LUTs	>30	30	N/A
	VHDL	–5	85 LUTs	>30	30	N/A
LatticeXP2™ [3]	Verilog	–5	83 LUTs	>30	30	N/A
	VHDL	–5	84 LUTs	>30	30	N/A
ispMACH® 4000ZE[4]	Verilog	–5 (ns)	60 Macrocells	>30	30	N/A
	VHDL	–5 (ns)	60 Macrocells	>30	30	N/A
ispMACH 4000V/B/C/Z[5]	Verilog	–2.7 (ns)	60 Macrocells	>30	30	N/A
	VHDL	–2.7 (ns)	60 Macrocells	>30	30	N/A
Platform Manager™ [6]	Verilog	–3	88 LUTs	>30	30	N/A
	VHDL	–3	85 LUTs	>30	30	N/A
ECP5™ [10]	Verilog	6	88 LUTs	>30	30	N/A
	VHDL	6	85 LUTs	>30	30	N/A

8-Port Assert Implementation						
MachXO2[1]	Verilog	–4	129 LUTs	>30	50	N/A
	VHDL	–4	122 LUTs	>30	50	N/A
MachXO[2]	Verilog	–5	219 LUTs	>30	50	N/A
	VHDL	–5	212 LUTs	>30	50	N/A
LatticeXP2[3]	Verilog	–5	108 LUTs	>30	50	N/A
	VHDL	–5	122 LUTs	>30	50	N/A
ispMACH 4000ZE[4]	Verilog	–5 (ns)	108 Macrocells	>30	50	N/A
	VHDL	–5 (ns)	108 Macrocells	>30	50	N/A
ispMACH 4000V/B/C/Z[5]	Verilog	–2.7 (ns)	108 Macrocells	>30	50	N/A
	VHDL	–2.7 (ns)	108 Macrocells	>30	50	N/A
Platform Manager[8]	Verilog	–3	129 LUTs	>30	50	N/A
	VHDL	–3	122 LUTs	>30	50	N/A
ECP5 ™ [10]	Verilog	6	129 LUTs	>30	50	N/A
	VHDL	6	122 LUTs	>30	50	N/A
8-Port JTAG Implementation						
MachXO2[1]	Verilog	–4	154 LUTs	>30	50	N/A
	VHDL	–4	147 LUTs	>30	50	N/A
MachXO[2]	Verilog	–5	271 LUTs	>30	50	N/A
	VHDL	–5	147 LUTs	>30	50	N/A
LatticeXP2[3]	Verilog	–5	148 LUTs	>30	50	N/A
	VHDL	–5	149 LUTs	>30	50	N/A
ispMACH 4000ZE[4]	Verilog	–5 (ns)	127 Macrocells	>30	50	N/A
	VHDL	–5 (ns)	127 Macrocells	>30	50	N/A
ispMACH 4000V/B/C/Z[5]	Verilog	–2.7 (ns)	127 Macrocells	>30	50	N/A
	VHDL	–2.7 (ns)	127 Macrocells	>30	50	N/A
ECP5™ [7]	Verilog	154	193 LUTs	>30	50	N/A
	VHDL	147	195 LUTs	>30	50	N/A

Table 4.2. Performance and Resource Utilization (Continued)

Device Family	Language	Speed Grade	Utilization	f_{MAX} (MHz)	I/Os	Architecture Resources
Platform Manager[6]	Verilog	–3	154 LUTs	>30	50	N/A
	VHDL	–3	147 LUTs	>30	50	N/A

Notes:

1. Performance and utilization characteristics are generated using LCMX02-640HC-4TG100C with Lattice Diamond® 3.1 design software with LSE (Lattice Synthesis Engine).
2. Performance and utilization characteristics are generated using LCMXO2640C-5T100C with Diamond 3.1 design software.
3. Performance and utilization characteristics are generated using LFXP2-5E-5M132C with Lattice Diamond 3.1 design software.
4. Performance and utilization characteristics are generated using LC4128ZE-5TN100C with ispLEVER® Classic 1.4 software.
5. Performance and utilization characteristics are generated using LC4128V-27T100C with ispLEVER Classic 1.4 software.
6. Performance and utilization characteristics are generated using LPTM10-12107-3FTG208CES with ispLEVER 8.1 SP1 software.
7. Performance and utilization characteristics are generated using LFE5UM-85F-CABGA756 with Lattice Diamond 3.1 design software with LSE.

Appendix A. BSCAN2 Configuration in SVF Format

```
ENDIR idle;
ENDDR idle;
HDR 0;
HIR 0;
TDR 0;
TIR 0;
STATE RESET;      ! Go to TLR, clearing the
                  ! scan select register

SIR 8 TDI  (7E);  ! Load the SCANSEL instruction

SDR 8 TDI  (NN);  ! Load the Select Register
                  !where NN = Desired value from
                  !Select register mapping (HEX)
```

Figure A.1. SVF Configuration Template for BSCAN2 x 4 Port

```
ENDIR idle;
ENDDR idle;
HDR 0;
HIR 0;
TDR 0;
TIR 0;
STATE RESET;      ! Go to TLR, clearing the
                  ! scan select register

SIR 8 TDI  (7E);  ! Load the SCANSEL instruction

SDR 16 TDI  (NNNN); ! Load the Select Register
                    !where NNNN = Desired value from
                    !Select register mapping (HEX)
```

Figure A.2. SVF Configuration Template for BSCAN2 x 8 Port (Asset Model)

```
ENDIR idle;
ENDDR idle;
HDR 0;
HIR 0;
TDR 0;
TIR 0;
STATE RESET;      ! Go to TLR, clearing the
                  ! scan select register

SIR 16 TDI  (7E7E); ! Load the SCANSEL instruction

SDR 16 TDI  (NNNN); ! Load the Select Register
                    !where NNNN = Desired value from
                    !Select register mapping (HEX)
```

Figure A.3. SVF Configuration Template for BSCAN2 x 8 Port (JTAG Model)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 4.9, December 2019

Section	Change Summary
All	• Changed document number from RD1002 to FPGA-RD-02106. • Updated document template.
Disclaimers	Added this section.

Revision 4.8, January 2017

Section	Change Summary
Functional Description	Updated this section. In Figure 2.2., TAP Controller State Machine, corrected the Exit1-DR to Update-DR arrow from TMS-L to TMS=H.
Technical Support Assistance	Updated this section.

Revision 4.7, March 2015

Section	Change Summary
Functional Description	Updated this section. In Table 2.1., Pin List, added details to the description of IDN 1:4 pin.
Implementation	• Added support for ECP5 device family. • Added support for Lattice Diamond 3.1 design software.

Revision 4.6, March 2014

Section	Change Summary
Implementation	• Updated Table 4.1., Performance and Resource Utilization. • Added support for ECP5 device family. • Added support for Lattice Diamond 3.1 design software.

Revision 4.5, December 2011

Section	Change Summary
All	• Added support for all device families. • Removed explicit GSR instance.

Revision 4.4, April 2011

Section	Change Summary
Implementation	• Added support for MachXO2 device family. • Added support for Lattice Diamond 1.2 design software.

Revision 4.3, December 2010

Section	Change Summary
Implementation	• Added support for Platform Manager device family. • Added support for Lattice Diamond 1.1 and ispLEVER 8.1 SP1 design software.

Revision 4.2, January 2010

Section	Change Summary
Implementation	• Added support for LatticeXP2 device family • Added VHDL support for all families. • Added support for ispLEVER 8.0.

Revision 4.1, February 2009

Section	Change Summary
All	• Added performance and resource utilization information. • Removed legacy device pinout information.

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