BSCAN1 – Multiple Scan Port Addressable Buffer

Reference Design

FPGA-RD-02105-7.4

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1. Introduction

BSCAN1 is a multiple boundary scan test access port (TAP) addressable buffer function that can be accessed through a standard IEEE 1149.1 interface. With three Local Scan Ports (LSP), the BSCAN1 function can be structured as hierarchical ports with the ability to add and remove local scan chains to improve test throughput. The LSP can also be accessed individually or in combination of two or three ports at a time to streamline the test flow of similar devices.

The LSPs are configured by accessing the Mode Register from the master TAP interface. In addition to the standard TAP interface signals TDI, TMS, TCK, TDO and TRST, the BSCAN1 interface also includes six static ID inputs and a TOE input. The Mode Register is used to configure the local scan ports. It allows daisy chaining and/or bypassing of the local scan ports. The static ID inputs are capable of supporting up to 64 unique addresses. The TOE signal is used to enable or disable all the local scan ports.

The major functional blocks and general architecture of BSCAN1 are illustrated in Figure 1.1. As defined in IEEE 1149.1, the instruction register and various test data registers can be scanned to exercise the functions of BSCAN1. The 16-state state machine TAP Controller, hereafter called the Master TAP Controller, provides the main control for the device.

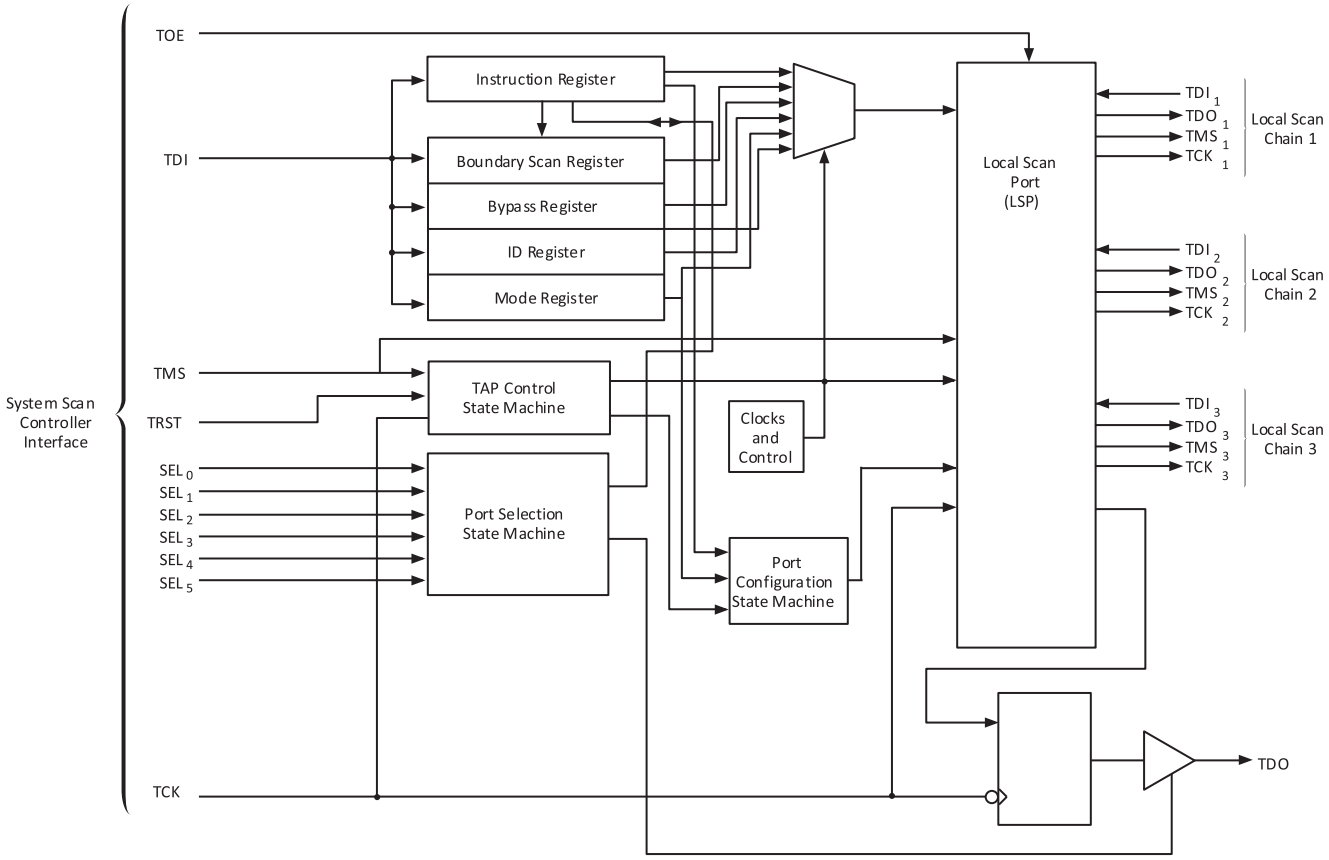

Figure 1.1. BSCAN1 Block Diagram

The primary function of the Port Selection Controller is to compare the address shifted into the Instruction Register to the static identification inputs, allowing the 1149.1 protocol to be used within a multidrop environment. It then enables BSCAN1, as appropriate, for other operations. Multiplexing logic for selecting different port configurations is contained in the Local Scan Port (LSP).

The BSCAN1 instruction register, mode register and the TAP Controller all provide input into the Local Scan Controller block. All four TAP boundary scan signals are then fed by the Local Scan Controller from their respective ports to the local scan ports.

2. Functional Description

In a multidrop scan system, the scan tester has the ability to select individual BSCAN1 devices as needed for scan operations. Scan chains are selected when a particular device address is sent to all BSCAN1 devices. The device with the corresponding, hardcoded address is enabled to receive instructions from the scan tester. This selection is done using a "Level 1" protocol (see Glossary) and subsequent instructions are sent to the appropriate BSCAN1 by using a "Level 2" protocol.

As is described in Figure 2.1., BSCAN1 contains an 1149.1 TAP Control State Machine (Figure 2.2.), a Selection State Machine (Figure 2.3.) and a Port Configuration State Machine (identical for each local port, see Figure 2.4.).

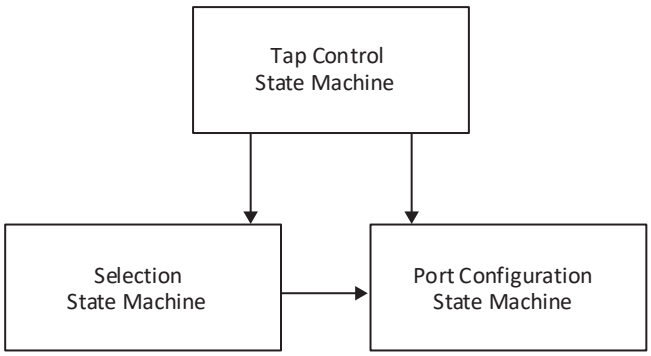

Figure 2.1. Internal State Machines

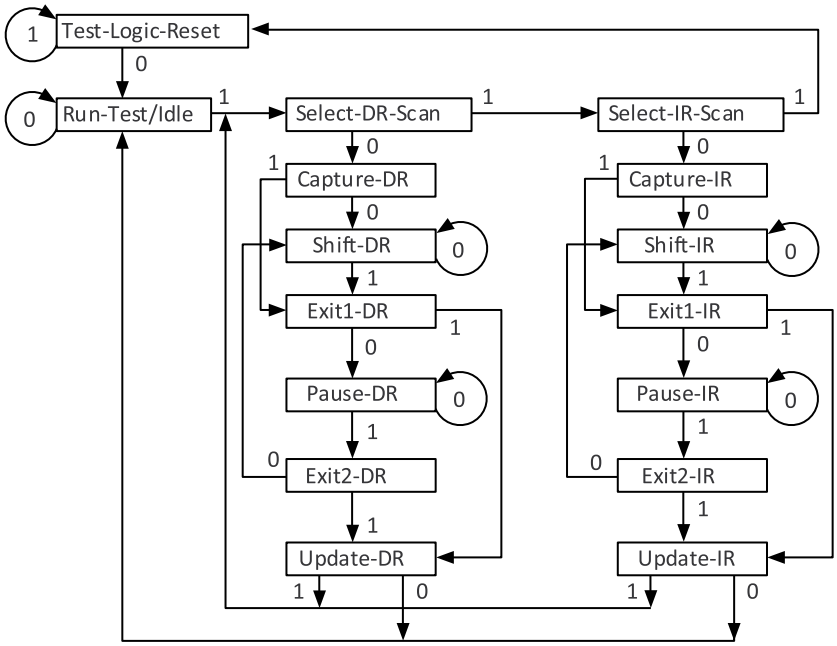

Figure 2.2. IEEE 1149.1 State Machine

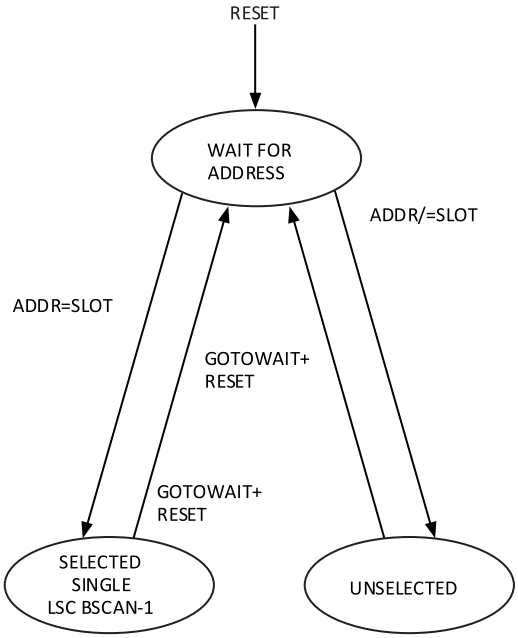

Figure 2.3. Selection Controller State Machine

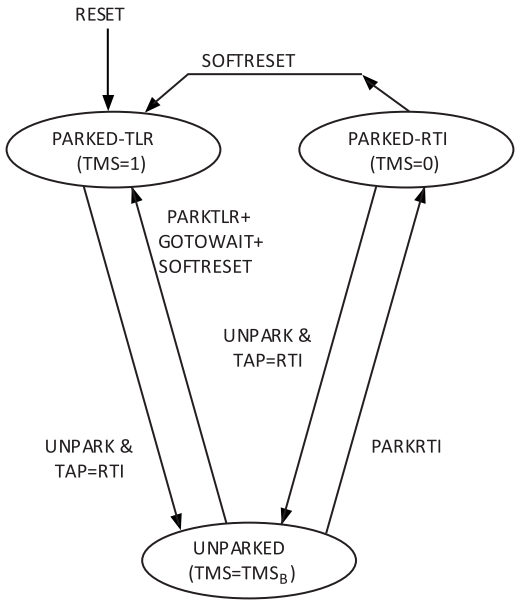

Figure 2.4. Local Port Configuration State Machine

The Selection State Machine is responsible for the addressing and multidrop capability. It also supports functionality for single access and the chip's Level 1 protocol. The Port Configuration State Machine allows the individual enabling and disabling of the LSPs from the overall scan chain.

The Port Configuration State Machine controls which local scan ports are included in, and which ports are isolated from, the overall scan chain. Therefore, to the system scan controller, each BSCAN1 represents only a single scan chain. Internal to BSCAN1 is the logic that controls which or how many of the LSPs are included in the chain presented to the system scan controller. There are two stable states in which a local port can be parked: Parked-TLR and Parked-RTI. Once a chain is parked, it is removed from the active scan chain indefinitely, or until "unparked." Unparking a chain moves it into the active chain. As is shown in Figure 2.4., the state of each of the local ports is independent of the states of other local ports on BSCAN1. It is important to understand that some states depend on the current state of the TAP Controller State Machine, while in others the state of BSCAN1's TAP Control State Machine can be forced by transitions of the Port Configuration State Machine. BSCAN1's Port Configuration State Machine provides part of the Level 2 protocol and has a number of Level 2 instructions other than local scan port configuration that provide access to and control of various registers within BSCAN1. The instructions include:

- BYPASS
- EXTEST
- SAMPLE/PRELOAD
- IDCODE
- MODESEL
- GOTOWAIT

Each BSCAN1 can be selected individually. Level 2 protocol commands are used to park or unpark. After a reset, BSCAN1 is ready for Level 1 protocol and Level 2 protocol instructions, in that order. The TAP controller state machine is reset to the TLR (Test-Logic-Reset) state, the Port Selection State Machine is in the Wait-for-Address state and the three local scan ports are in the Parked-TLR state.

3. Signal Descriptions

Table 3.1. Signal Descriptions

Pin	I/O	Description
TCK	I	Test clock input from the backplane. This is the master clock signal that controls all scan operations of BSCAN1 and of the three local scan ports.
TMS	I	Test mode select input from the backplane. Controls sequencing through the TAP controller of BSCAN1. Also controls sequencing of the TAPs on the three local scan chains.
TDI	I	Test data input from the backplane. All backplane scan data is supplied to BSCAN1 through this input pin.
TDO	O	Test data output to the backplane. This output drives test data from BSCAN1 back to the master controller.
TRST	I	Test reset. An active-low, asynchronous reset signal, which initializes the BSCAN1 logic.
SEL[0:5]	I	Static identification input. The configuration of these six pins is used to assign a unique address to each BSCAN1 on the system backplane.
TOE	I	Test output enable. When high, the local scan ports are enabled. When low, forces the local scan ports to tristate. This enables an alternate resource to access one or more of the three local scan chains.
TCK[1:3]	O	Local test clock outputs. Individual output to each of the three local scan ports. These are buffered versions of TCK.
TMS[1:3]	O	Local test mode select outputs. Individual output to each of the three local scan ports.
TDI[1:3]	I	Local test data inputs. Individual scan data input from each of the three local scan ports.
TDO[1:3]	O	Local test data outputs. Individual scan data output to each of the three local scan ports.

4. Backplane Interface

Via its backplane port, BSCAN1 receives instructions from the IEEE 1149.1 tester. BSCAN1 enters the Wait-for- Address state following the test logic reset. Data is shifted in through the TDI input and into the BSCAN1 Instruction register when the TAP controller is sequenced to the Shift-IR state. Note that if BSCAN1 is not properly addressed and successfully selected, no data is shifted out of the instruction register. Instead, as data is shifted into the instruction register, the data shifted out is discarded rather than exiting through the TDO output. Upon updating the instruction register with the address data, the scanned-in address is compared with the six least significant bits of the IR and the static address signals SEL(0-5) (see Figure 6.1.).

If no address match is detected, the device enters an unselected state. When an address is matched, it enters the selected state. Level 2 protocol is used to issue commands and access registers once a BSCAN1 has been selected.

5. Register Set

Selection and configuration, scan data manipulation and scan support operations registers can all be grouped as shown in Table 5.1. When a register is selected, data enters through the MSB and is shifted out through the scan input of the next device in the daisy chain (see Table 7.1.).

Table 5.1. Signal Descriptions

Register Name	Signal Description
Instruction Register	Addressing and instruction decode IEEE Standard 1149.1 required register
Boundary scan Register	IEEE Standard 1149.1 required register
Bypass Register	IEEE Standard 1149.1 required register
Device Identification Register	IEEE Standard 1149.1 required register
Mode Register	Local port configuration and control bits

6. Addressing Scheme

The basic function of BSCAN1 is to allow a large or complex system to be divided into smaller blocks for testing purposes. A central test controller is networked with one or more BSCAN1 devices and given the capability to address individual BSCAN1 devices. Both multidrop and hierarchical connectivity are supported and the test controller can dynamically select any part of the network.

BSCAN1 supports two levels of partitioning. A Level 1 protocol supports the selection of one BSCAN1 device. Within each device, a Level 2 protocol supports the selection of individual ports. The selected ports of the individual device are then presented as a single chain that can be included in the final network of the selected BSCAN1 device.

6.1. Addressing with Level 1 Protocol

One mode of addressing is supported by BSCAN1. Individual BSCAN1 devices can be selected in the “single” mode, also known as Direct Addressing.

6.1.1. Direct Addressing

BSCAN1 enters the Wait-for-Address state when: (1) Its TAP Controller enters the Test-Logic-Reset state, or (2) Its instruction register is updated with the GOTOWAIT instruction, while either selected or unselected.

While in the Wait-for-Address state, the BSCAN1 controller receives data shifted in through the instruction register. In the Update-IR state, bits 5 through 0 of the instruction register are compared with the statically configured address bits SEL(0-5). (Every BSCAN1 device in a scan network must be individually set with a unique address on its SEL(0-5) inputs.) A BSCAN1 device becomes selected, or active in the chain, when the six least significant bits of the instruction register match the static address bits SEL(0-5) (Figure 6.1.). The selected device is now ready to receive Level 2 protocol. When active, the selected device’s identification register is inserted as part of the active scan chain.

Table 6.1. Direct Address Mode

Address Type/Hex Address	Binary Address	TDO State
Direct Address 00h to 3Fh	XX000000b to XX111111b	Normal IEEE Standard 1149.1

Note: Only the six LSBs of the address are compared to the SEL (0-5) inputs. The two MSBs are “don’t cares”.

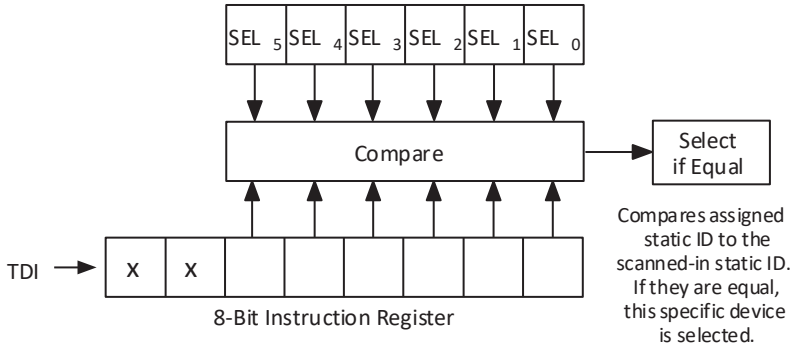

Figure 6.1. Direct Addressing: Device Address Loaded into Instruction Register

Unselected devices (where the static address did not match the six LSBs of the IR) will remain that way until their instruction register is updated with the GOTOWAIT instruction or their TAP controller enters the Test-Logic-Reset state.

6.2. Level 2 Protocol

Level 2 protocol follows IEEE standard 1149.1 TAP protocol. After being addressed and selected in the active chain, the BSCAN1 device is accessed by Level 2 protocol. Once BSCAN1 is selected, the local scan ports remain parked in one of two TAP Controller states (Run-Test/Idle, Test-Logic-Reset). The scan chain comes in through the TDI, through the instruction register or IDCODE register, and out through the TDO. Local scan ports can be inserted into the chain using the UNPARK instruction. The mode register is discussed later.

6.2.1. Level 2 Instruction Types

Level 2 has two instruction types (Table 6.2.):

1. Insert instructions bring the BSCAN1 register into the active chain, making it available to be captured or updated. (SAMPLE/PRELOAD, EXTEST, IDCODE, MODESEL and BYPASS).
2. Configure/control instructions insert the device identification into the active scan chain. (GOTOWAIT, SOFTRESET, PARKRTI, PARKTLR, UNPARK and other undefined op codes).

Table 6.2. Instruction Set

Instruction	Hex Opcode	Binary Opcode	Data Register
EXTEST	00h	00000000b	Boundary Scan Register
SOFTRESET	88h	10001000b	Device Identification Register
MODESEL	8Eh	10001110b	Mode Register
PARKRTI	84h	10000100b	Device Identification Register
SAMPLE/PRELOAD	81h	10000001b	Boundary Scan Register
PARKTLR	C5h	11000101b	Device Identification Register
GOTOWAIT	C3h	11000011b	Device Identification Register
IDCODE	AAh	10101010b	Device Identification Register
UNPARK	E7h	11100111b	Device Identification Register
BYPASS	FFh	11111111b	Bypass Register
Other Unidentified	TBD	TBD	Device Identification Register

Notes: All instructions act on selected BSCAN1s only.

6.2.2. Level 2 Instruction Descriptions

- **Bypass:** When BSCAN1 is selected, the BYPASS instruction inserts the bypass register into the active chain.
- **EXTEST:** This instruction is the same as the SAMPLE/PRELOAD instruction since there are no scalable outputs on the device. EXTEST inserts the boundary scan register into the active chain. The boundary scan register is a bank of seven “sample only” cells connected to the TOE and SEL(0-5) inputs.
- **SAMPLE/PRELOAD:** This instruction inserts the boundary scan register into the active chain (refer to EXTEST).
- **IDCODE:** IDCODE inserts the device identification register into the active scan chain. When exiting the Capture- DR state and IDCODE is the current active instruction, the device identification 0FC0E01Fh is captured.
- **PARKTLR:** Parks all unparked local scan ports in the Test-Logic-Reset TAP controller state and removes them from the active scan chain. A logic “1” is forced on the TMSn output while the LSP controller is in the Parked-TLR state (Figure 2.4.).
- **PARKRTI:** Parks all unparked Local Scan Ports in the Run-Test/Idle TAP controller state and removes them from the active scan chain. A logic “0” is forced on the TMSn output while the LSP controller is in the Parked-RTI state (Figure 2.4.).
- **UNPARK:** Unpark takes the Local Scan Port Network out of park and inserts it into the active scan chain. The mode register determines the configuration of the chain, as described later. While local scan ports (LSP) are unparked, they are synchronously sequenced with the TAP Controller State Machine. An LSP can only be unparked when the TAP controller enters the state it was in when the LSP became parked. For example: if the LSP was parked in the Test-Logic-Reset or Run-Test/Idle states, it is not unparked until an UNPARK instruction is followed by the TAP controller entering the Run-Test/Idle state (Figure 2.4.).
- **GOTOWAIT:** Parks all unparked local scan ports in the Test-Logic-Reset TAP controller state. All BSCAN1 devices are returned to the Wait-For-Address state (Figure 2.4.).
- **MODESEL:** Puts the mode register in the active scan chain.
- **SOFTRESET:** Parks all local ports in the Test-Logic-Reset state within five TCK cycles by causing all three port configuration controllers to enter the Parked-TLR state. TMSn is forced high (Figure 2.4.).

7. Register Descriptions

7.1. Instruction Register

This is an 8-bit serial shift register placed in series with the active scan chain when the TAP Controller State Machine of BSCAN1 is in the Shift-IR state. When BSCAN1 exits the Capture-IR state, the instruction register captures the value XXXXXX01b where the don’t cares represent the SEL(0-5) inputs. When it is in the Wait-for-Address state, BSCAN1’s instruction register is used for address matching. This is done by the individual chip comparing a hardwired value on BSCAN1’s static ID inputs to the address in the instruction register. Address 00h through 3Fh (000000b through 111111b) are reserved for individual BSCAN1 addressing.

7.2. Boundary Scan Register

This is a 7-bit register consisting of cells from the TOE and SEL(0-5) inputs. In order to allow testing of external circuitry, the Boundary Scan Register samples the inputs it is connected to without altering the internal logic of the chip. The shift order of the Boundary Scan register is: TDI->TOE ->SEL5 ->SEL4 -> SEL3 ->SEL2 ->SEL1 ->SEL0 ->LSP ->TDO.

7.3. Bypass Register

This one-bit register is defined by IEEE Standard 1149.1. Its primary purpose is to pass data between TDI and the local scan port. This register provides a passthrough path when none of the other registers are necessary. Using this register provides the shortest path to other registers located in the chain.

7.4. Mode Register

This is an 8-bit data register. Its primary function is to configure the local scan port network. When BSCAN1 enters the Test-Logic-Reset State, the register is initialized with 01h. The scan chain layout will be configured as shown in Table 7.1. when an UNPARK instruction executes. When all Local Scan Ports are parked, the configuration of the scan chain will be: TDI -> BSCAN1-register -> TDO.

The third bit of the mode register can be used to disconnect all the TCK signals from TCK. Its normal configuration has it set to logic “0” so that TCKn is free-running when the local scan ports are parked. Programming the third bit with a logic “1” forces the all the TCKn signals to stop. Changing the value of this Mode register bit should only be done while all the local ports are parked. Power sensitive applications can use this feature to reduce the power consumed by the test circuitry in parts of the system currently not under test.

Bits 5, 6 and 7 are currently unused (don’t care) but are reserved for future use.

Table 7.1. Mode Register Control of LSP

Mode Register	Scan Chain Configuration (if Unparked)
XXX00000b	TDI -> Register -> TDO
XXX00001b	TDI -> Register -> LSP1 -> PAD -> TDO
XXX00010b	TDI -> Register -> LSP2 -> PAD -> TDO
XXX00011b	TDI -> Register -> LSP1 -> PAD -> LSP2 -> PAD -> TDO
XXX00100b	TDI -> Register -> LSP3 -> PAD -> TDO
XXX00101b	TDI -> Register -> LSP1 -> PAD -> LSP3 -> PAD -> TDO
XXX00110b	TDI -> Register -> LSP2 -> PAD -> LSP3 -> PAD -> TDO
XXX00111b	TDI -> Register -> LSP1 -> PAD -> LSP2 -> PAD -> LSP3 -> PAD -> TDO
XXX10XXXb	TDI -> Register -> TDO (Loopback)

Notes:

1. X = don’t care
2. Register = BSCAN1 instruction register or any of the BSCAN1 test data registers
3. PAD = insertion of a 1-bit register for synchronization
4. XXX || XXXb | TDI -> Register -> TDO, TCK1-3 disabled.

7.5. Device Identification Register

This 32-bit register is defined by IEEE Standard 1149.1. When an IDCODE instruction is received, this register is loaded with 0FC0E01Fh when the device exits Capture-DR state.

Table 7.2. Detailed Device Identification (Binary)

Bits 31-28	Bits 27-12	Bits 11-1	Bit 0
Version	Part Number	Manufacturer Identity	1
0000b	1111 1100 0000 1110b	0000 0001 111b	1b

7.6. Reset

There are three levels of reset. The top level resets every BSCAN1 register and every local scan chain of both selected and unselected BSCAN1 devices. Entering the Test-Logic-Reset State automatically invokes this reset level. There are two ways to enter Test-Logic-Reset: 1) It is entered asynchronously when TRST is pulled low or 2) It can be entered synchronously by pulling TMS high for five or more TCK pulses. When a top level reset occurs, all BSCAN1 registers are initialized, all local scan chains are parked in the Test-Logic-Reset State, and all BSCAN1 are put into the Wait-for-Address state.

The SOFTRESET instruction is provided to perform a reset of all the LSPs of a selected BSCAN1. SOFTRESET forces all TMS signals high, placing the corresponding local TAP controllers in the Test-Logic-Reset state within five TCK cycles. The third level of reset is the resetting of individual local ports. An individual LSP can be reset by parking the port in the Test-Logic-Reset state via the PARKTLR instruction. To reset an individual LSP that is parked in PARKTLI state, the LSP must first be unparked via the UNPARK instruction.

Table 7.3. Reset Configuration for Registers

Register	Bit Width	Initial Value
Instruction	8	AAh (IDCODE Instruction)
Mode	8	01h

8. Port Synchronization

When a LSP is not being accessed, it is placed in one of the two TAP controller states: Test-Logic-Reset or Run-Test/Idle. BSCAN1 is able to park a local chain by controlling the local Test Mode Select outputs (TMS1-3) (Figure 2.4.). TMS is forced high for parking in the Test-Logic-Reset state and forced low for parking in the Run-Test/Idle state. Local chain access is achieved by issuing the UNPARK instruction. The LSPs do not become unparked until the BSCAN1 TAP Controller is sequenced through a specified synchronization state. Synchronization occurs in the Run-Test/Idle state for LSPs parked in Test-Logic-Reset and Run-Test/Idle states. Figure 8.1. and Figure 8.2. show the waveforms for synchronization of a local chain that was parked in the Test-Logic-Reset state. Once the UNPARK instruction is received in the instruction register, the LSP Controller forces TMSn low on the falling edge of TCK. This moves the local chain TAP controllers to the synchronization state (Run-Test/Idle), where they stay until synchronization occurs. If the next state of the BSCAN1 TAP Controller is Run-Test/Idle, TMSn is connected to TMS and the local TAP controllers are synchronized to the BSCAN1 TAP Controller State Machine as shown in the last TCK cycle of Figure 8.1. If the next state after Update-IR were Select-DR, TMSn would remain low and synchronization would not occur until the TAP controller entered the Run-Test/Idle state, as shown in TCK cycles 2 through 6 of Figure 8.1.

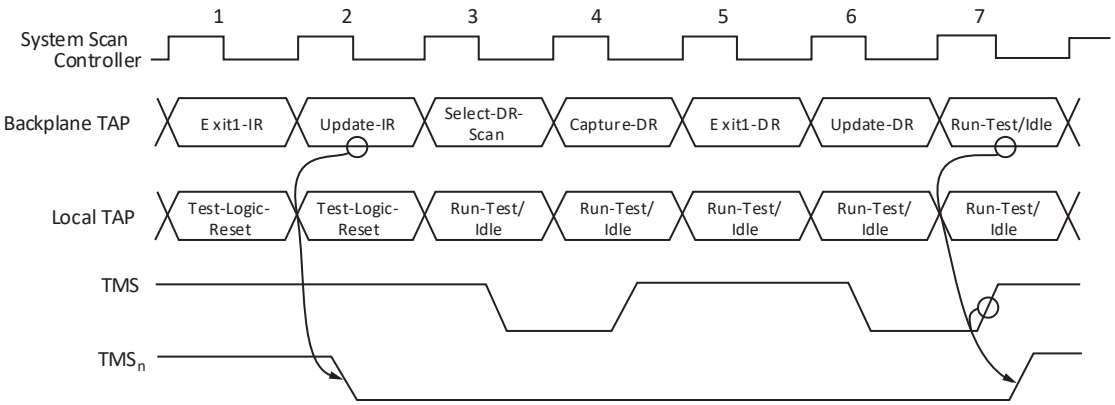

Figure 8.1. Local Scan Port Synchronization on Second Pass

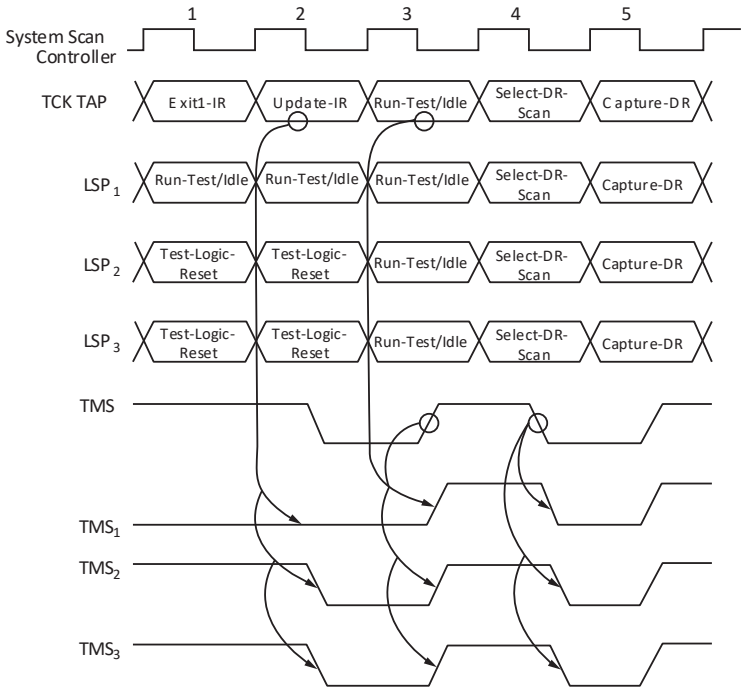

Figure 8.2. Synchronization of the Three Local Scan Ports (LSP_1, LSP_2 and LSP_3)

Each local port has its own Local Port Controller. This is necessary because the LSP can be configured in any one of eight possible combinations. Either one, some, or all of the local ports can be accessed simultaneously. Configuring the LSP is accomplished with the mode register, in conjunction with the UNPARK instruction. The LSP can be unparked in one of seven different configurations, as specified by bits 0-2 of the mode register. Using multiple ports presents not only the task of synchronizing the BSCAN1 TAP Controller with the TAP Controllers of an individual local port, but also of synchronizing the individual local ports to one another. When multiple local ports are selected for access, it is possible that two ports are parked in different states. This could occur when previous operations accessed the two ports separately and parked them in the two different states. The LSP Controllers handle this situation gracefully.

9. Implementation

This design is implemented in Verilog and VHDL. When using this design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 9.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization	f_{MAX} (MHz)	I/O	Architecture Resources
MachXO2™ [1]	Verilog	-5	182 LUTs	>30	24	N/A
	VHDL	-5	182 LUTs	>30	24	N/A
MachXO™ [2]	Verilog	-3	182 LUTs	>30	24	N/A
	VHDL	-3	182 LUTs	>30	24	N/A
LatticeXP2™ [3]	Verilog	-5	182 LUTs	>30	24	N/A
	VHDL	-5	182 LUTs	>30	24	N/A
ispMACH® 4000ZE[4]	Verilog	-5 (ns)	101 Macrocells	>40	24	N/A
	VHDL	-5 (ns)	101 Macrocells	>40	24	N/A
ispMACH 4000V/B/C/Z[5]	Verilog	-2.7 (ns)	101 Macrocells	>70	24	N/A
	VHDL	-2.7 (ns)	101 Macrocells	>70	24	N/A
Platform Manager™ [6]	Verilog	-3	182 LUTs	>30	24	N/A
	VHDL	-3	182 LUTs	>30	24	N/A

Notes:

1. Performance and utilization characteristics are generated using LCMXO2-256HC-5TG100C with Lattice Diamond™ 1.2 software.
2. Performance and utilization characteristics are generated using LCMXO256C-3T100C with Diamond 1.2 software.
3. Performance and utilization characteristics are generated using LFXP2-5E-5M132C with Lattice Diamond 1.2 software.
4. Performance and utilization characteristics are generated using LC4128ZE-5TN100C with ispLEVER® Classic 1.4 software.
5. Performance and utilization characteristics are generated using LC4128V-27T100C with ispLEVER Classic 1.4 software.
6. Performance and utilization characteristics are generated using LPTM10-1247-3TG128CES with ispLEVER 8.1 SP1 software.

Glossary

- **LSP:** Local Scan Port. A four signal port that drives a “local” (i.e. non-backplane) scan chain. (e.g., TCK1, TMS1, TDO1, TDI1).
- **Local:** Local is used to describe IEEE Standard 1149.1 compliant scan rings and the BSCAN1 Test Access Port that drives them. The term “local” was adopted from the system test architecture that BSCAN1 is most commonly used in: a system test backplane with an BSCAN1 on each card driving up to three “local” scan rings per card. Each card can contain multiple BSCAN1s, with three local scan ports per BSCAN1.
- **Park/Unpark:** Park, parked, unpark and unparked are used to describe the state of the LSP controller and the state of the local TAP controllers (the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking an LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when an LSP controller is in a parked state, TMSn is held constant, thereby holding or “parking” the local TAP controllers in a given state.
- **TAP:** Test Access Port as defined by IEEE Standard 1149.1
- **Selected/Unselected:** Selected and Unselected refers to the state of the Port Selection State Machine. A selected BSCAN1 has been properly addressed and is ready to receive Level 2 protocol. Unselected BSCAN1 devices monitor the system test backplane, but do not accept Level 2 protocol (except for the GOTOWAIT instruction). The data registers and LSPs of unselected BSCAN1 devices are not accessible from the system test master.
- **Active Scan Chain:** The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When BSCAN1 is selected with all of its LSPs parked, the active scan chain refers to the current scan bridge register only. When an LSP is unparked, the active scan chain becomes: TDI ->the current BSCAN1 register ->the local scan ring registers ->a PAD bit ->TDO. Refer to Table 7.1. for unparked configurations of the LSP network.
- **Level 1 Protocol:** Level 1 is the protocol used to address BSCAN1.
- **Level 2 Protocol:** Level 2 is the protocol that is used once BSCAN1 is selected. Level 2 protocol is IEEE Standard 1149.1 compliant when an individual BSCAN1 is selected.
- **LSB:** Least Significant Bit, the right-most position in a register (bit 0).
- **MSB:** Most Significant Bit, the left-most position in a register.
- **PAD:** A one-bit register that is placed at the end of each local scan port scan chain. The PAD bit eliminates the propagation delay that would be added by the BSCAN1 LSP logic between TDIn and TDO(n+1) or TDO by buffering and synchronizing the TDIn inputs to the falling edge of TCK. This allows data to be scanned at higher frequencies without violating set-up and hold times.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 7.4, December 2019

Section	Change Summary
All	• Changed document number from RD1001 to FPGA-RD-02105. • Updated document template.
Disclaimers	Added this section.

Revision 7.3, April 2011

Section	Change Summary
Implementation	• Added support for MachXO2 device family. • Added support for Lattice Diamond 1.2 design software.

Revision 7.2, December 2010

Section	Change Summary
Implementation	• Added support for Platform Manager device family. • Added support for Lattice Diamond 1.1 and ispLEVER 8.1 SP1 design software.

Revision 7.1, January 2010

Section	Change Summary
Implementation	• Added support for LatticeXP2 device family. • Added VHDL support for all device families.

Revision 7.0, February 2009

Section	Change Summary
All	• Updated formatting. • Removed legacy pin assignment section. • Converted pin descriptions to table.
Introduction	Corrected Figure 1.1., BSCAN1 Block Diagram.
Implementation	Added Implementation resource table.

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