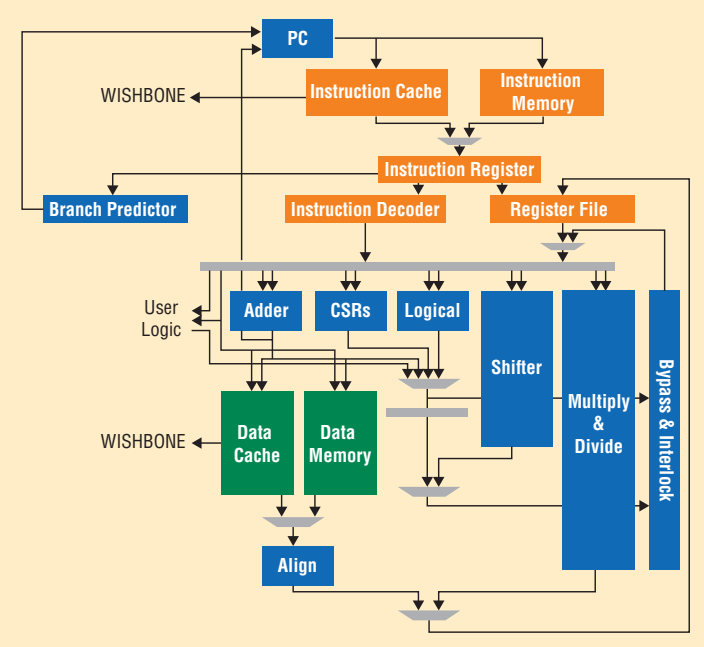
LatticeMico32

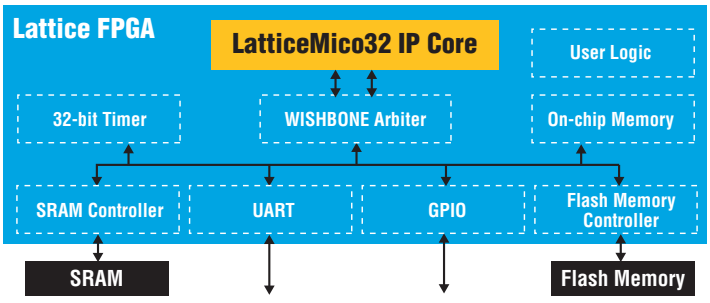
Soft Core 32-Bit Microprocessor Optimized for Lattice Programmable Devices

The LatticeMico32™ is a highly configurable 32-bit Harvard architecture "soft" microprocessor core for Lattice FPGA devices. LatticeMico32 combines a 32-bit wide instruction set with 32 general purpose registers, to provide the performance and flexibility suitable for a wide variety of markets. Using a Reduced Instruction Set Computer (RISC) architecture, the core consumes minimal device resources, while maintaining the performance required for a broad application set. The associated LatticeMico™ System Development Tools provide a fast and easy way to implement microprocessor designs. The tools coordinate processor platform definition, software development and debug. Additionally, the LatticeMico32 is available as source code under the Lattice open IP core license, thereby providing visibility, flexibility and portability – all free of charge.

LatticeMico32 Block Diagram



Build a Complete Embedded System



Key Features and Benefits

- **Optimized for Lattice FPGA Devices**
- **Innovative Open IP Core License**
- **Performance Enhanced Feature Set**
  - RISC architecture
  - 32-bit data path
  - 32-bit instructions
  - 32 general purpose registers
  - Handles up to 32 external interrupts
  - Optional instruction cache
  - Optional data cache
  - Optional inline data memory
  - Optional inline instruction memory
  - WISHBONE memory interfaces (Instruction and Data)
- **Easy to Use Development Tools**
  - LatticeMico System for:
    - Platform definition
    - C/C++ Software development
    - Debug
  - LatticeMico System operates with Lattice Diamond®
  - Includes support for:
    - Standard Make
    - Non-volatile memory deployment
- **Peripheral Components (WISHBONE)**
  - Memory controllers: DDR, DDR2 and DDR3 SDRAM controllers, asynchronous SRAM, on-chip block memory, SDRAM controller, on-chip dual port memory, SPI Flash, parallel Flash
  - I/O: 32-bit timer, Tri-Speed Ethernet MAC, DMA controller, GPIO, I²C master controller, SPI, UART, PCI Target

Development Tools

The LatticeMico System is used to implement the LatticeMico32 soft microprocessor and attached peripheral components in a Lattice FPGA. It is based on the Eclipse C/C++ Development Tools (CDT) environment, which is an industry open-source development and application framework for building software. The LatticeMico System contains two integrated tools (detailed below) that combine with Diamond to coordinate the building of an embedded processor system on an FPGA device and to write the software that drives it.

- **Mico System Builder (MSB)**
  - Choose peripheral components to attach to the LatticeMico32
  - Specify connectivity between peripheral components
  - Generate platform description and associated HDL for hardware implementation
- **C/C++ Software Project Environment (SPE) and Debugger**
  - Develop the code that runs on platforms created with MSB
  - Interfaces to compiler, assembler, linker, and debugger tools

Open IP Core Licensing

The generated LatticeMico32 core and selected peripheral component HDL codes are available through a unique open IP core licensing agreement, while the GNU-based compiler, assembler, linker and debugger are licensed under the GNU GPL agreement. The main benefits of open source IP are:

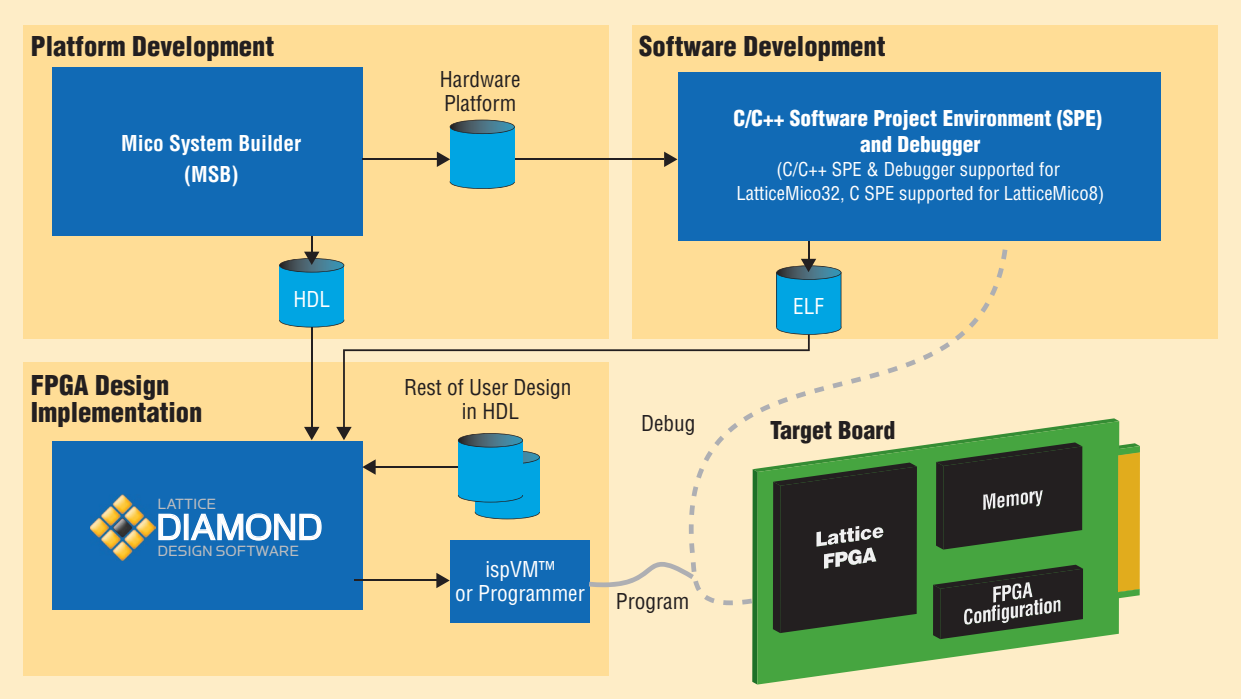
- **Visibility**
  - Allows complete understanding of the detailed operation of the core
- **Flexibility**
  - User can develop alternate micro-architectures or implementations
- **Portability**
  - Architecture independence
  - Migrate to an ASIC or an SoC
- **Free of Charge**

Resource Utilization/Performance*

Lattice FPGA Family	LUTs	Max. Clock Frequency
LatticeECP3™	2370	115 MHz
LatticeXP2™	2406	85 MHz
LatticeECP2/M	2497	110 MHz

** Standard configuration with 8K instruction cache.*

LatticeMico System Development Flow



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LATTICE DIAMOND DESIGN SOFTWARE

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