LOW COST SERIAL TRANSMISSION WITH THE LatticeECP2M FPGA

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Shifting the Programmable SERDES Paradigm

While many SERDES-based designs will continue to need a high performance FPGA fabric and I/O structure, there is a growing need for low cost solutions as well. PCI Express and Serial Ethernet based designs are replacing legacy PCI and Fast Ethernet interfaces. As these standards become ubiquitous and an integral part of FPGA designs, there will be a need for an accompanying low cost FPGA to handle the relatively lower performance bridging, co-processing and glue logic functionality of those designs.

Traditionally, SERDES based FPGAs have only been offered as part of a vendor's flagship FPGA portfolio, meaning that customers have had two choices when it comes to architecting a programmable platform to address Serial multi-protocol transmission: pay the premium for an integrated, high performance FPGA family or forego the integration and revert to the 2 chip solution of a discrete PHY plus low cost FPGA.

There are many applications where neither of these choices is palatable. These include lower bandwidth, high volume, small form factor applications where both cost and board real estate are tightly budgeted. Applications such as wireless BTS or node Bs, edge/access platforms enabling Triple Play technologies and low cost industrial, audio/video and medical applications that require both high speed signal processing and serial transmission integrated a low cost programmable platform. The emergence of ATCA and microTCA standard form factors in these application areas coupled with its adoption by OEMs will also drive the need to provide more hardware integration at increasingly lower cost points. Often the only solution available is to pay a large NRE to one of the shrinking number of Structured ASIC vendors, which provides a non-programmable solution that is more costly, inflexible and has an extending the time to market.

Lattice is the only FPGA vendor that has addressed both the high performance and low cost areas of the SERDES application space. In its LatticeSC flagship FPGA, it

has provided all the ingredients for Extreme Performance FPGA design with the highest level of hard IP integration and industry leading I/O and fabric speeds. In the Lattice ECP2M FPGA, it offers a solution that couples a low cost FPGA fabric with a high performance MAC (Multiply Accumulate) engine together with the industry's first integrated, low-cost SERDES on a single chip.

The key to achieving a low cost SERDES is to adequately target the needs of the low cost SERDES market and ensure that it meets the specifications needed to achieve reliable transmission and reception of key serial protocols over nominal PCB (FR-4 based) distances. These specifications include:

- Reliable transmission and recovery of serial signals for chip to chip and small form factor back planes (20 inches of FR-4 or less)
- Embedded digital logic to support popular serial protocols, focusing mainly on Ethernet and PCI Express as well as other packet based derivatives such as CPRI, OBSAI, SRIO and Fibre Channel
- Providing complete protocol stack support by developing key pieces of IP for the industry's lowest cost FPGA fabric with embedded SERDES ($0.65 per KLUT)
- Easy configuration of SERDES and supplemental IP blocks.

Although each protocol is unique, one thing that they all have in common is a layered protocol stack. However, all protocol stacks are not created equal: their implementation can vary greatly from one layer to the next. Typically, the physical layer consists of fixed functionality that is common to multiple packet-based protocols, while the upper layers tend to be more customizable. The dynamic of upper layer functionality is necessitated by both the natural evolution that takes place when dealing with an emerging standard as well as the desire of system vendors to create their own "value add" via proprietary functionality. Therefore, the value of programmability for implementation of these upper layer serial standards means a SERDES-based FPGA solution will remain a necessity for the foreseeable future. Figure 1 shows the functional partitioning of the physical and the upper layers of the protocol stacks.

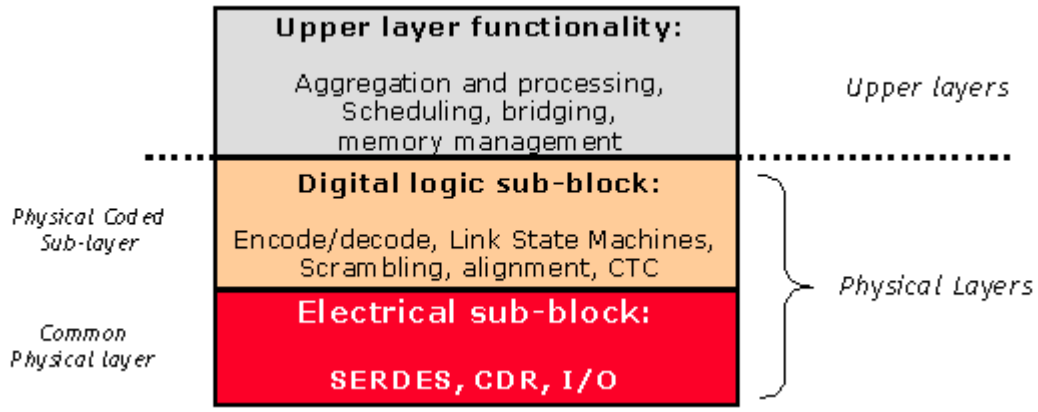

Figure 1 – Serial Protocol stack functional partitioning

This paper examines the implementation of these multi-protocol standards and their associated stacks and discusses why they are ideally suited to an FPGA-based SERDES implementation such as the Lattice ECP2M family of devices.

Physical Layer

As shown in Figure 1, many elements of the Physical Layer (PHY) are common across many of the packet-based protocols. The functionality is partitioned into the electrical sub-block and the digital logic sub-block. These blocks provide the foundation for implementing a multitude of existing and emerging serial packet based protocols that will be explored in greater detail later in the following sections.

The Importance of a Cost Effective Robust SERDES

System level designers are often faced with moving large blocks of data from one location to another over moderate distances and high rates of speed. Historically, this was accomplished by a source synchronous parallel interface, which required large banks of parallel line drivers and receivers. In addition, it has become more and more difficult to ensure the data integrity of these types of interfaces from board to board at the gigabit plus data rates that are required in systems today.

With the inception and growing acceptance of Serializer/Deserializer (SERDES) devices, designers can alleviate the concerns inherent in the implementation of a parallel interface. SERDES technology permits smaller, less expensive cables and

connectors, while providing a more robust solution in terms of signal integrity when moving large blocks of data at rates of 3.125Gbps and beyond.

The Lattice ECP2M delivers the industry's lowest cost integrated SERDES and FPGA solution by focusing on delivering a very tight range of specification that delivers robust performance at the lowest cost.

- **Drive length** (across passive channel) - 20 inches of FR-4 backplane @ 3.125Gbps (aided by built-in Tx pre-emphasis and Rx equalization).
- **Tx/Rx jitter tolerance** - Tx/Rx jitter values (0.24UI at 2.5G for Tx, 0.80UI tolerance for Rx, typical) meet PCI Express, GbE and FC jitter specifications.
- **Power** - 100 mW/channel (typical) @ 3.125Gbps, including I/O buffers and Rx equalization.
- **Flexibility** - 270Mbps-3.2Gbps serial data rates (full and half rate data rates selectable per channel)**,** with emphasis on PCI Express and Ethernet based applications.

Physical Coded Sublayer (PCS)

In addition to a quality SERDES, it is also essential to offer the associated Physical Coded Sublayer (PCS) functionality that is required in order to comply with existing packet-based industry standards such as PCI Express, Serial RapidIO, GbE, XAUI, Fibre Channel and emerging standards such as CPRI and OBSAI. The Lattice ECP2M FPGA provides such a solution by coupling industry leading SERDES technology with associated higher layer PCS logic implemented as a mixture of embedded hard and soft IP. Unlike the LatticeSC, the LatticeECP2M provides only basic common PCS functionality, relying on the industry's most cost effective FPGA fabric to implement low cost protocol stack implementations.

Among the features supported in the PCS logic are:

- Link Synchronization State Machines
- 8b/10b Encoding/Decoding
- Clock Tolerance Compensation

The following section describes how an entire protocol stack can be implemented in the FPGA fabric at the lowest existing price points in the industry.

Wireline Networks: PCI Express, Serial RapidIO, Ethernet and Fibre Channel

These are four of the most popular serial protocols utilized in wireline applications. Figure 2 shows the PHY layer support offered by the Lattice ECP2M PCS logic. The following sections provide a more detailed look at each protocol and the inherent advantages the Lattice ECP2M programmable platform provides.

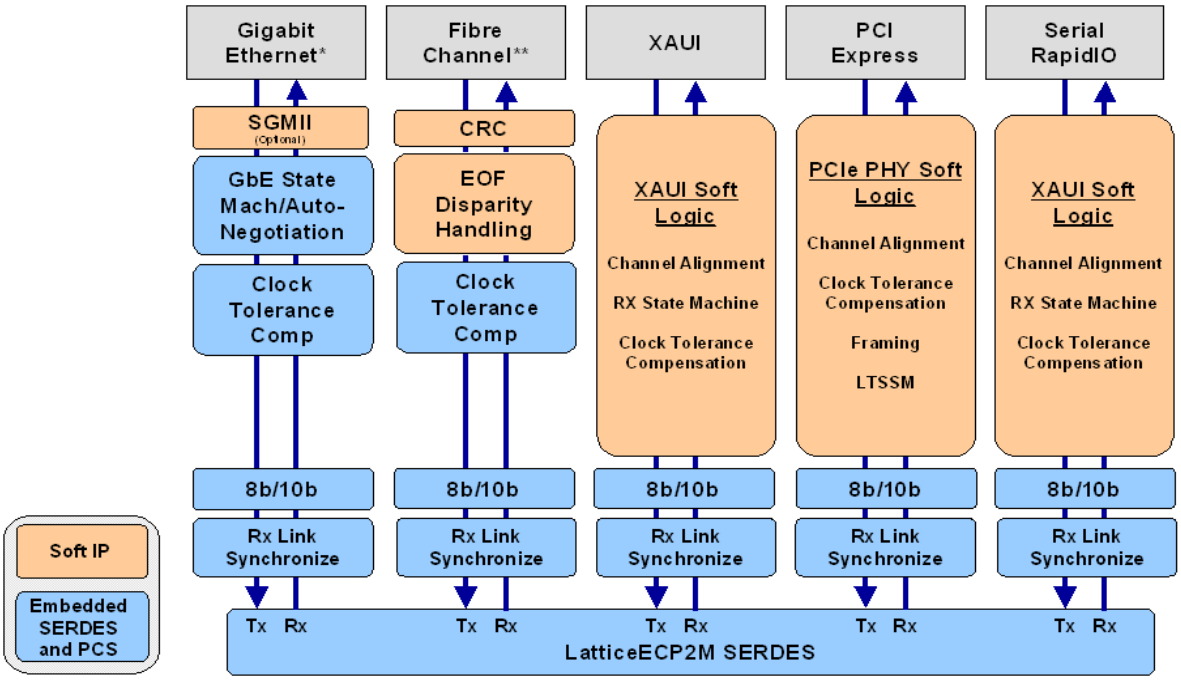

Figure 2 – ECP2M Supported Packet Protocols

PCI Express

Conventional PCI, once the standard I/O bus with its roots in the early 90's, is now showing its age. This has led designers to implement newer versions such as PCI-x and PCI-x 2.0, allowing them to maintain the existing software base while achieving greater throughput. But even with these enhancements, processor throughput still outpaces I/O throughput.

PCI Express was conceived in order to address these ever increasing bandwidth needs by providing a scalable, point-to-point serial connection between chips, over

cable or via connector slots for expansion cards, while maintaining compatibility with conventional PCI at the software layer.

A single PCI Express serial link is a dual-simplex connection, specified to speeds of up to 2.5Gbps per link that can be scaled in x1, x2, x4, x8, x12, x16 and x32 lane widths to achieve greater bandwidth. A serial implementation is cheaper, can be driven further distances and alleviates common mode noise and skew concerns inherent in existing source synchronous parallel interfaces (such as conventional PCI), as well as reducing the overall number of connections required. For practical purposes, this paper will discuss lane widths available for implementation on standard cable connectors.

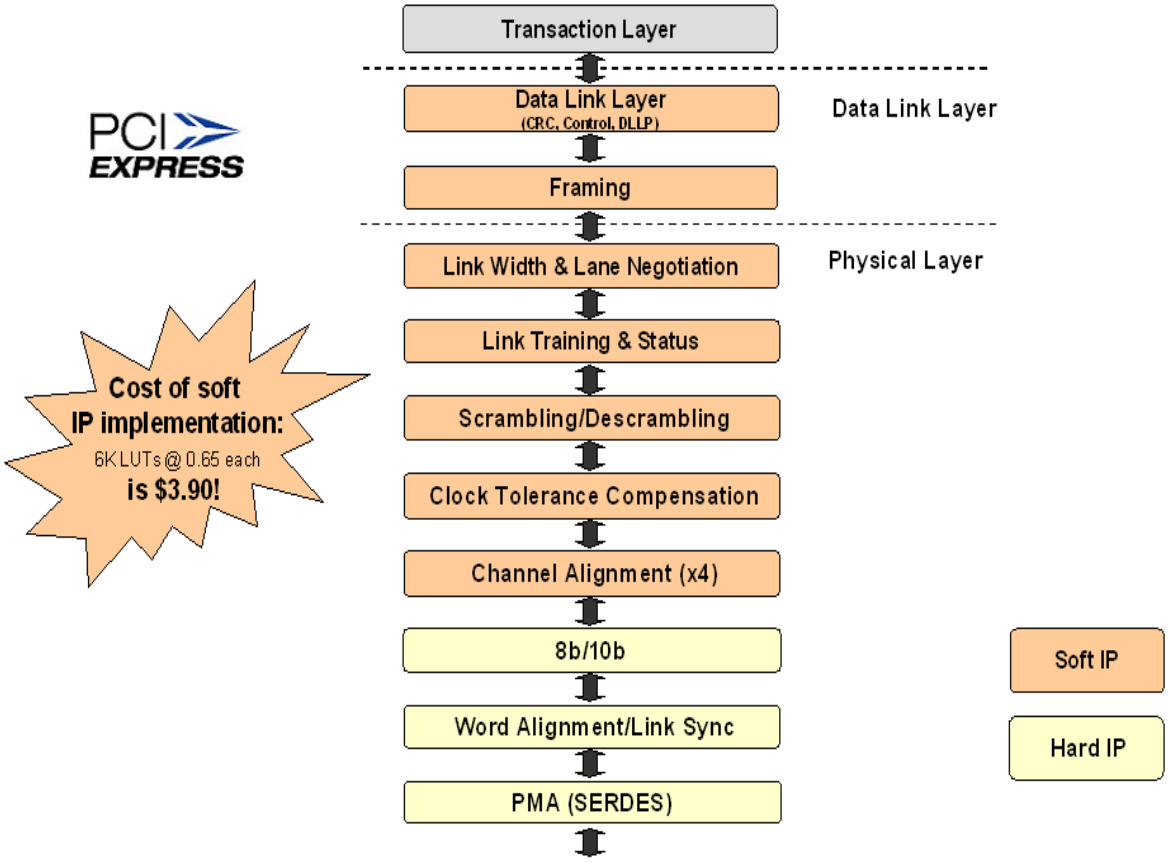

Figure 3 – Lattice ECP2M PCI Express protocol stack implementation

As Figure 3 illustrates, PCI Express is a packetized and layered protocol structure. The stack consists of the Physical (PHY), Data Link and Transaction layers. This white paper has previously noted the value of a programmable solution when implementing the protocol stacks of these emerging standards and, in this case, both

the data link layer and transaction layers of the PCI Express stack are good examples of functionality that takes advantage of programmability.

Depending upon the design, these layers can be customized to support an end point implementation or in many cases in which an FPGA is involved, a bridging function to a legacy communications protocol such as conventional PCI.

Serial RapidIO

Another emerging serial standard is Serial RapidIO. Like PCI Express, Serial RapidIO has its roots in the source synchronous world. When combined with the existing RapidIO parallel specification, Serial RapidIO allows designers to standardize on a single interconnect technology for networking, telecommunications and other embedded applications.

Serial RapidIO is a scalable, point-to-point, low pin count interconnect designed to address increasing system bandwidth needs. Serial RapidIO leverages industry-standard signaling technology found in Fibre Channel, 10G Ethernet XAUI interfaces and Infiniband, and operates at 1.25, 2.5 and 3.125 Gigabaud per link, providing the required bandwidth for signal processors and backplane applications. The serial specification defines both a single differential link in each direction between devices and support for ganging four links together for higher throughput applications.

As illustrated in Figure 4, Serial RapidIO also has a layered protocol structure. Lattice Semiconductor also offers a family of devices that, when coupled with available embedded hard and soft IP cores, provides a low cost, low power and highly integrated solution that addresses the physical, with future support for the logical and transport, layers of the Serial RapidIO specification.

As with PCI Express, a Serial RapidIO implementation also benefits from the inherent flexibility that a programmable device provides. Here, the malleable logical and transport layer functionality can be implemented in FPGA gates, while the fixed functionality of the physical layer is dedicated to the embedded portion of the device.

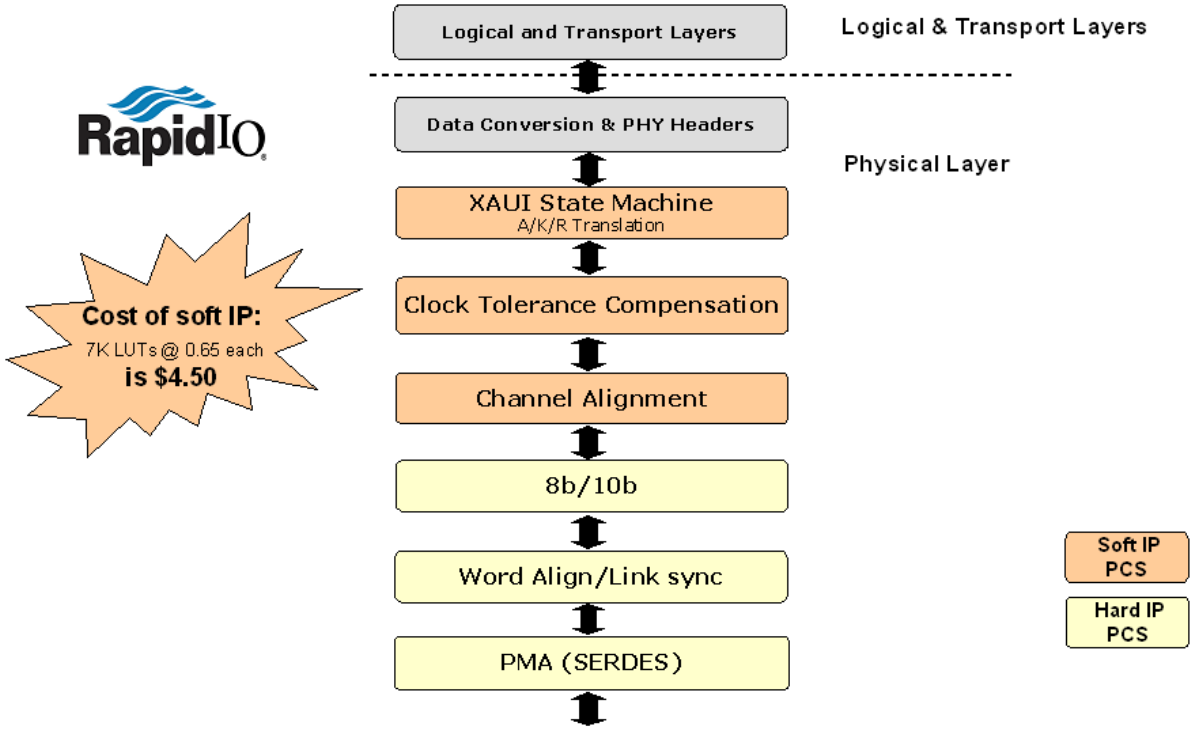

Figure 4 – Serial RapidIO protocol stack implementation

Ethernet

Gigabit Ethernet

Based on the volume of installed ports, Ethernet is the most dominant networking protocol by virtue of its cost performance relative to other solutions.

Gigabit Ethernet builds on top of the Ethernet protocol, but increases the speed tenfold over Fast Ethernet from 100Mbps to 1000 Mbps, or 1 gigabit per second (Gbps). By leveraging the Fast Ethernet protocol stack, GbE allows customers to migrate their Fast Ethernet solutions while maintaining software compatibility with existing products.

As Figure 5 shows, GbE is a layered protocol structure. The stack consists of the Physical (PHY) layers as well as the MAC, Logical Link and other customizable upper layers. Once again, there is value in a programmable solution for GbE applications. The Lattice ECP2M family offers a fully compliant 802.3z implementation of a GbE PHY in the PCS portion of our SERDES. This EMBEDDED block provides functionality such as 8b/10 encode/decode, link state machine, auto-negotiation and

clock tolerance compensation. When combined with available MAC layer IP and proprietary upper layer functionality, the Lattice ECP2M allows the user to design a fully integrated GbE solution.

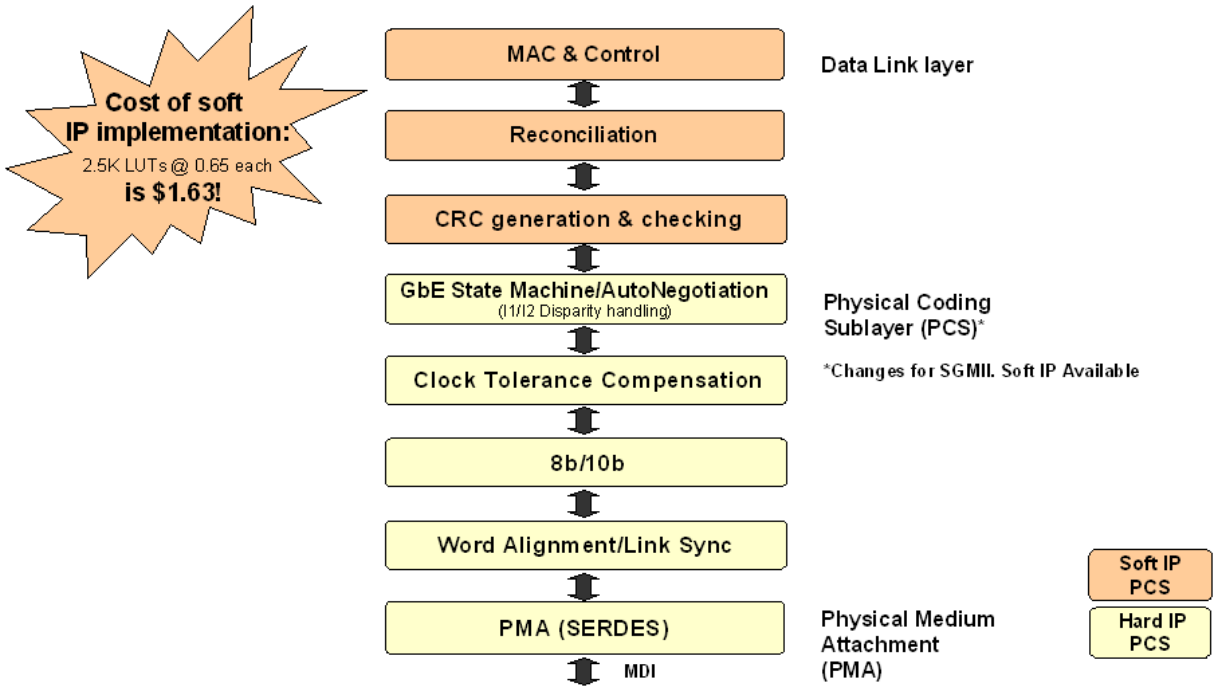

Figure 5 – LatticeECP2M GbE stack implementation

XAUI

XAUI transceivers are comprised of four 3.125-Gbit/s SERDES channels and employ the same 8B/10B-transmission code of GbE to provide the high level of signal integrity necessary to traverse both chip-to-chip and backplane interfaces. By virtue of its serial nature, XAUI reduces 10G Ethernet's 72-pin XGMII interface to 16 pins, simplifying and extending the reach of the interface. The same PCS block can also be used for 10G Fibre Channel applications with minor changes that can be implemented in the FPGA.

Figure 6 illustrates the XAUI interface and where it resides in the 10G Ethernet stack. The LatticeECP2M family of devices offer a fully compliant 802.3ae-2002 XAUI implementation, including EMBEDDED block functionality such as 8b/10 encode/decode, Tx/Rx state machines with programmable |A|, |K|, |R| characters,

lane alignment and deskew and clock tolerance compensation. This block also provides an XGMII to support interfacing with the Lattice 10G MAC IP that is also available. This Lattice IP, when combined with proprietary upper layer functionality, allows the LatticeECP2M to offer a fully integrated XAUI solution.

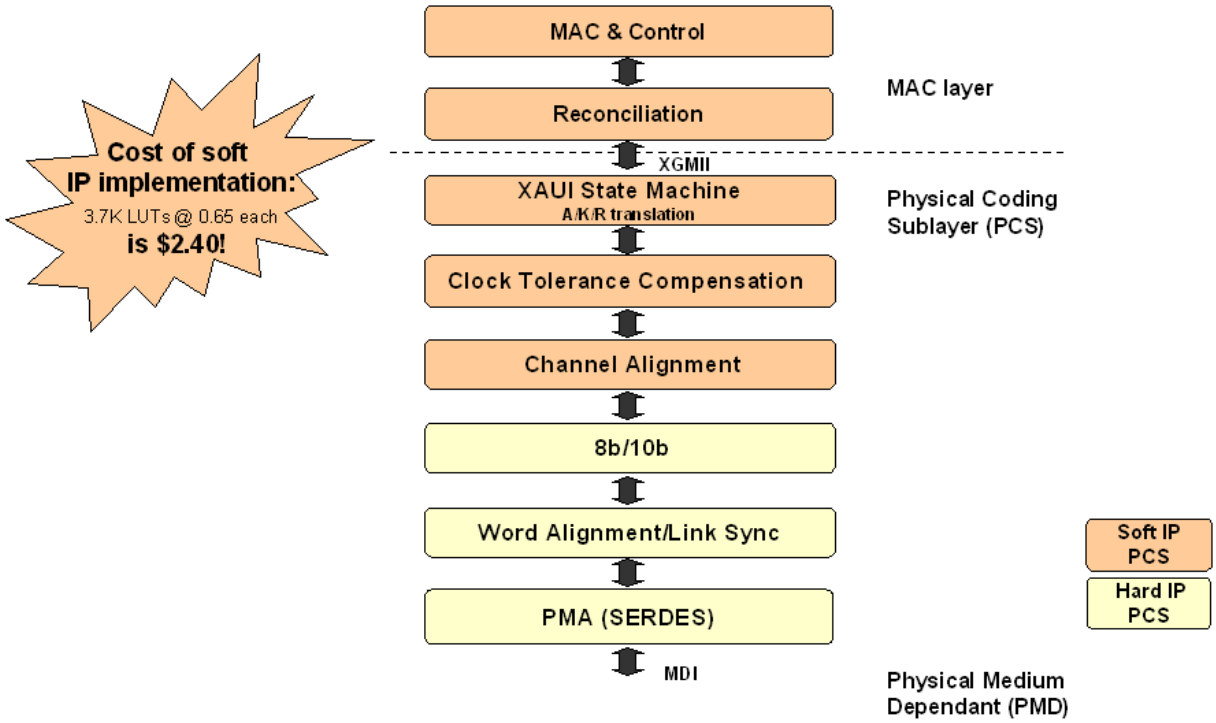

Figure 6 – LatticeECP2M XAUI implementation

Fibre Channel

Fibre Channel (FC) was developed as a practical, inexpensive and expendable means of quickly transferring data between workstations, mainframes, supercomputers, desktop computers, storage devices, displays and other peripherals. Fibre channel is a high performance serial link supporting its own, as well as other higher-level protocols, such as the FDDI, SCSI, HIPPI and IPI. The Fibre Channel standard addresses the need for very fast, reliable transfers of large amounts of information. The bulk of current implementations operate at 1Gbps on a single serial channel; however, specifications exist for single channel data rates of 2G, 4G and 10Gbps as well.

The Fibre Channel mode of the Lattice ECP2M SERDES/PCS block supports the 1G and 2G Fibre Channel protocol. Layers FC-0 and FC-1 are implemented in the embedded PCS block, which includes capabilities such as Tx/Rx state machines, 8b/10b encode/decode and word alignment. Figure 7 shows the Lattice implementation of the FC protocol stack. The remaining FC-2 functionality and any other customer specific upper layer functionality can be implemented in the FPGA portion of the device.

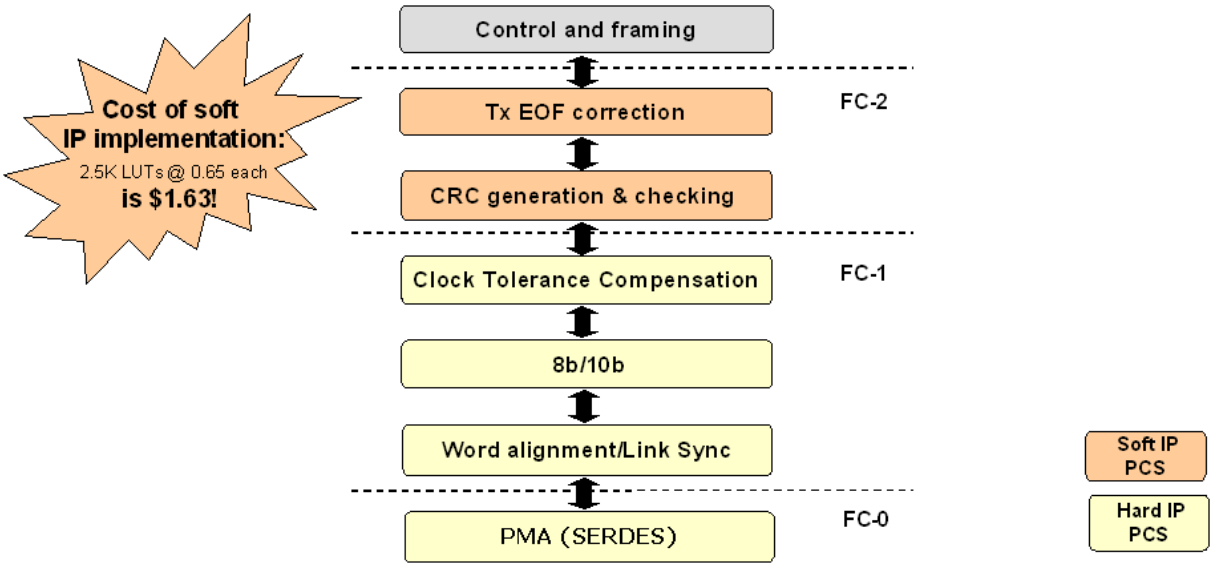

Figure 7- LatticeECP2M Fibre Channel stack implementation

Wireless Networks

CPRI and OBSAI

In the wireless domain, two initiatives are currently competing to facilitate the more rapid development of cellular base stations. Both the CPRI and OBSAI standards focus on the standardization of serial transmission protocols, with the primary objective the reduction of overall system cost though the standardization of its components.

CPRI

The CPRI (Common Public Radio Interface) is an industry initiative with the intent to support a flexible basestation architecture by partitioning the base station into two basic building blocks, the radio equipment control (REC), which handles the base band functionality, and the Radio Equipment (RE), which provides the RF functionality.

Building blocks are interconnected by a serial data link that is 8b10b encoded and intended to utilize existing High Speed Serial standards such as Ethernet and Fibre Channel. Physical layer line rates of 614Mbs, 1.228Gbs or 2.456Gbps are supported with three different information flows (User Plane data, Control & Management (C&M) and Synchronization) multiplexed over a single serial interface.

Lattice Semiconductor offers a complete system solution for CPRI applications. The physical layer functionality is supported via the embedded PCS core in the LatticeECP2M devices, with associated soft IP cores addressing data link layer functionality, as shown in Figure 9.

OBSAI

Similarly, OBSAI partitions the base station into baseband and RF blocks, but also defines an additional Transport and Control block. In contrast to CPRI, the interfaces between each of these are unique reference points, defined as RP1 (control plane), RP2 (user plane between transport to base band blocks) and RP3 (user plane between base band and RF blocks). These building blocks are specified as Ethernet interfaces, but for the purposes of this white paper the focus will be on the RP3 interface, since it is an 8b/10b encoded serial link similar to the CPRI specification mentioned above.

Physical layer line rates of 768Mb, 1.536Gbps and 3.072Gbps are supported for the RP3-01 interface in support of high speed data transfer and associated control. The protocol stack is again a packet concept utilizing a layered protocol, as shown in Figure 9 below.

Again, the SERDES and 8b/10b-based nature of the Lattice ECP2M devices provide an integrated platform in support of a complete OBSAI system solution. Physical layer functionality is supported via the embedded PCS core of the devices, with associated soft IP core addressing data link layer functionality.

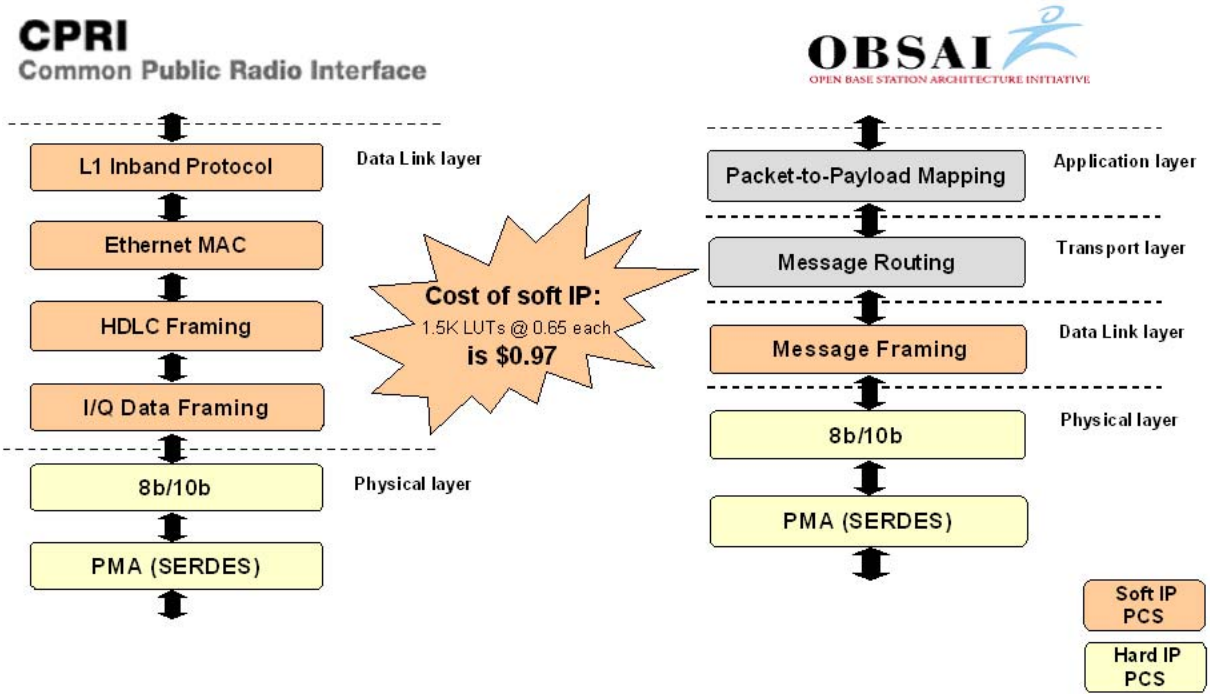

Figure 9 – LatticeECP2M CPRI/ OBSAI RP3-01 protocol stack implementation

Summary

The LatticeECP2M family maintains all of the compelling features of the base LatticeECP2 family, including DSP functionality, that are required for high-volume, cost sensitive applications. The SERDES integrated into the LatticeECP2M is implemented in a cost optimized, quad-based architecture with 1 to 4 quads per device, depending on the size of the device. Each quad features 4 SERDES channels (4 complete TX and RX channels) and supports data rates from 270 Mbps to 3.125 Gbps. A flexible PCS layer that includes 8b/10b encoding, an Ethernet link state machine and rate matching circuitry are also built onto the chip. The SERDES/PCS combination is designed to support today's most common packet-

based protocols, which include PCI Express, Gigabit Ethernet, XAUI, Serial RapidIO, wireless interface standards (OBSAI and CPRI), etc.

The combination of SERDES, high performance DSP, and a low cost FPGA fabric is extremely attractive to Edge and Access system vendors that are integrating these serial protocols into their wireless base stations, radio network controllers, DSLAMs, and other last mile aggregation equipment that enable “triple play” technologies. Medical imaging and industrial equipment vendors interested in low cost signal processing will also benefit from the unique combination of features available on the LatticeECP2M family. This feature- and cost-optimized SERDES is available in an FPGA family priced from $0.65/KLUT, a 70% decrease compared to previous SERDES-based FPGAs.

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