LatticeSC™ Communications Platform Evaluation Board: LFSC25E-H-EV

User's Guide

April 2007
Revision: ebug16_01.3

Introduction

This user's guide describes the LatticeSC Communications Platform Evaluation Board featuring the LatticeSC 900-fpBGA FPGA device. The stand-alone evaluation PCB provides a functional platform for development and rapid prototyping of applications that incorporate high-performance, source-synchronous interfaces such as SFI-4, XSBI, SPI-4.2, and DDR2 SDRAM.

The evaluation board includes provisioning to connect high-speed SERDES channels via SMA connectors to test and measurement equipment. The board is manufactured using standard FR-4 dielectric and through-hole vias. The nominal impedance is 50-ohm for single-ended traces and 100-ohm for differential traces.

The board has several debugging and analyzing features for complete customer evaluation of the LatticeSC device. This guide is intended to be referenced in conjunction with evaluation design tutorials to demonstrate the LatticeSC FPGA.

Features

- Single Data Rate (SDR) performance for SFI-4.1/XSBI applications via a 300-pin MSA transponder interconnection
- System packet interface level 4-phase 2 (SPI-4.2) via a Molex VHDM interconnection
- DDR2 dual in-line memory module (DIMM) via a 200-pin SODIMM socket supporting 64-bit 200-pin DDR-2 SDRAM
- SERDES high-speed interface SMA test points and clock connections
- Power connections and power sources
- ispVM® programming support
- On-board and external reference clock sources
  - Interchangeable clock oscillators
  - On-board reference clock management using Lattice ispClock™ devices
- ORCAstra™ demonstration software interface via standard ispVM JTAG connection
- Various high-speed layout structures
- User-defined input and output points
  - 24 board programmable switches or LEDs
  - 2 defined debounced push-buttons connected to GPIO
- SMA connectors included (10) for high-speed clock or data interfacing
- On-board Flash configuration memory
- Performance monitoring via Agilent logic analyzer connectors and 100-mil test headers
- Flash memory devices for on-board non-volatile configuration storage
- On-board voltage margin testing with multiple voltage regulators Verification and Debug capabilities

Figure 1. LatticeSC Communications Platform Evaluation Board (LFSC25E-H-EV), Top View

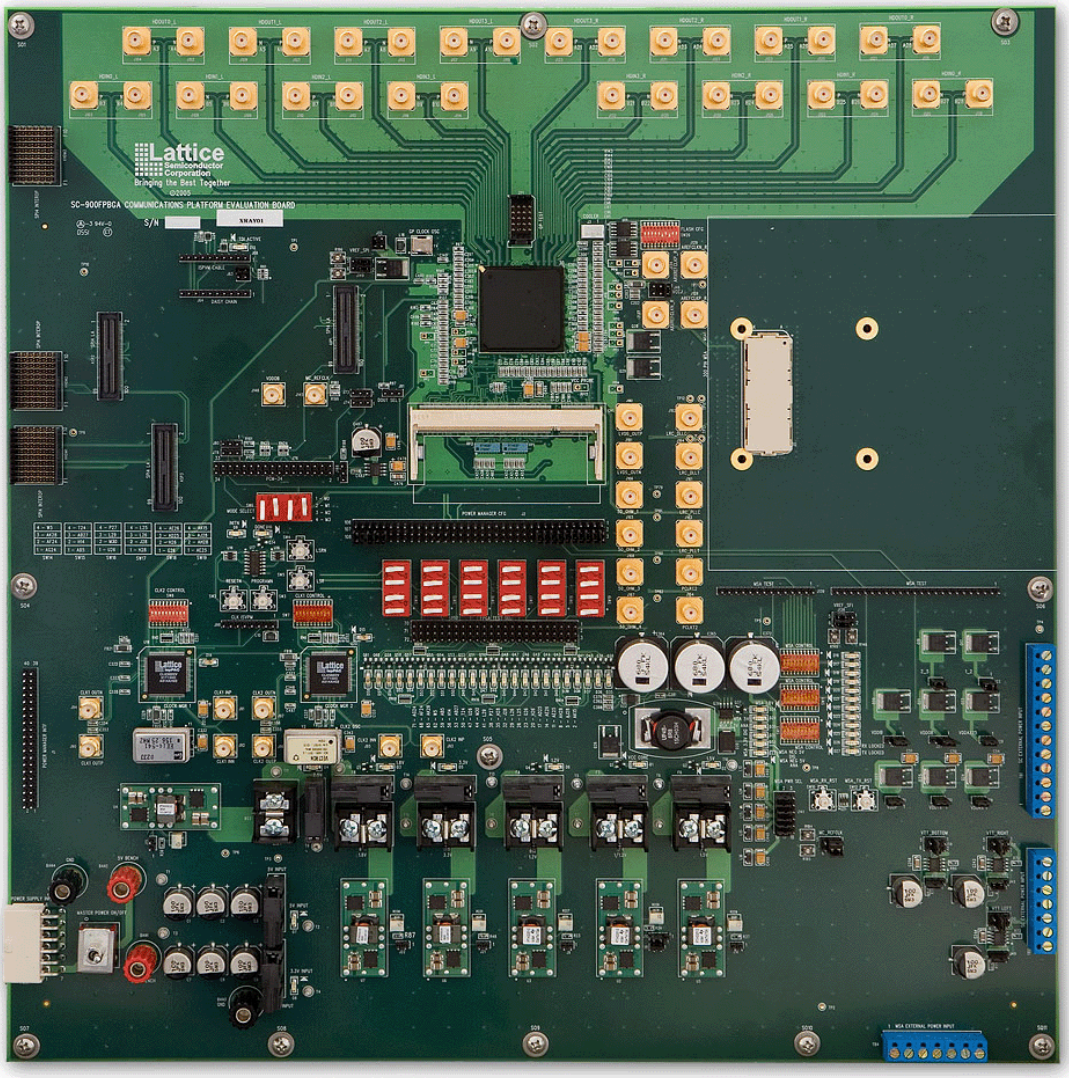
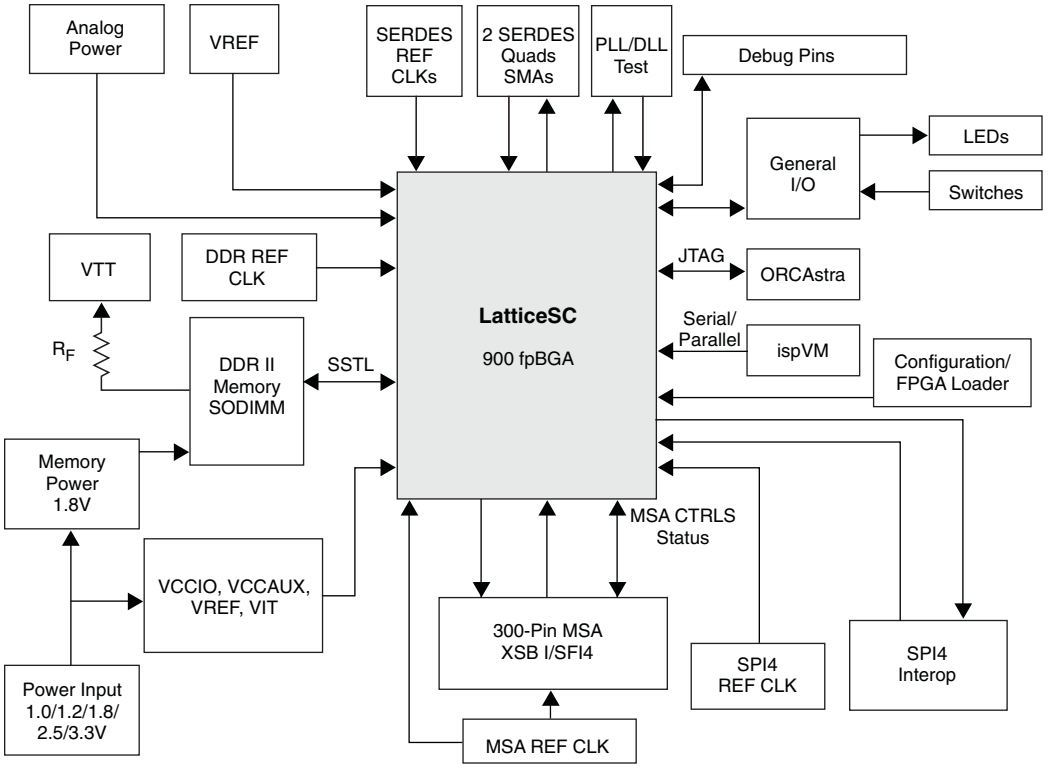


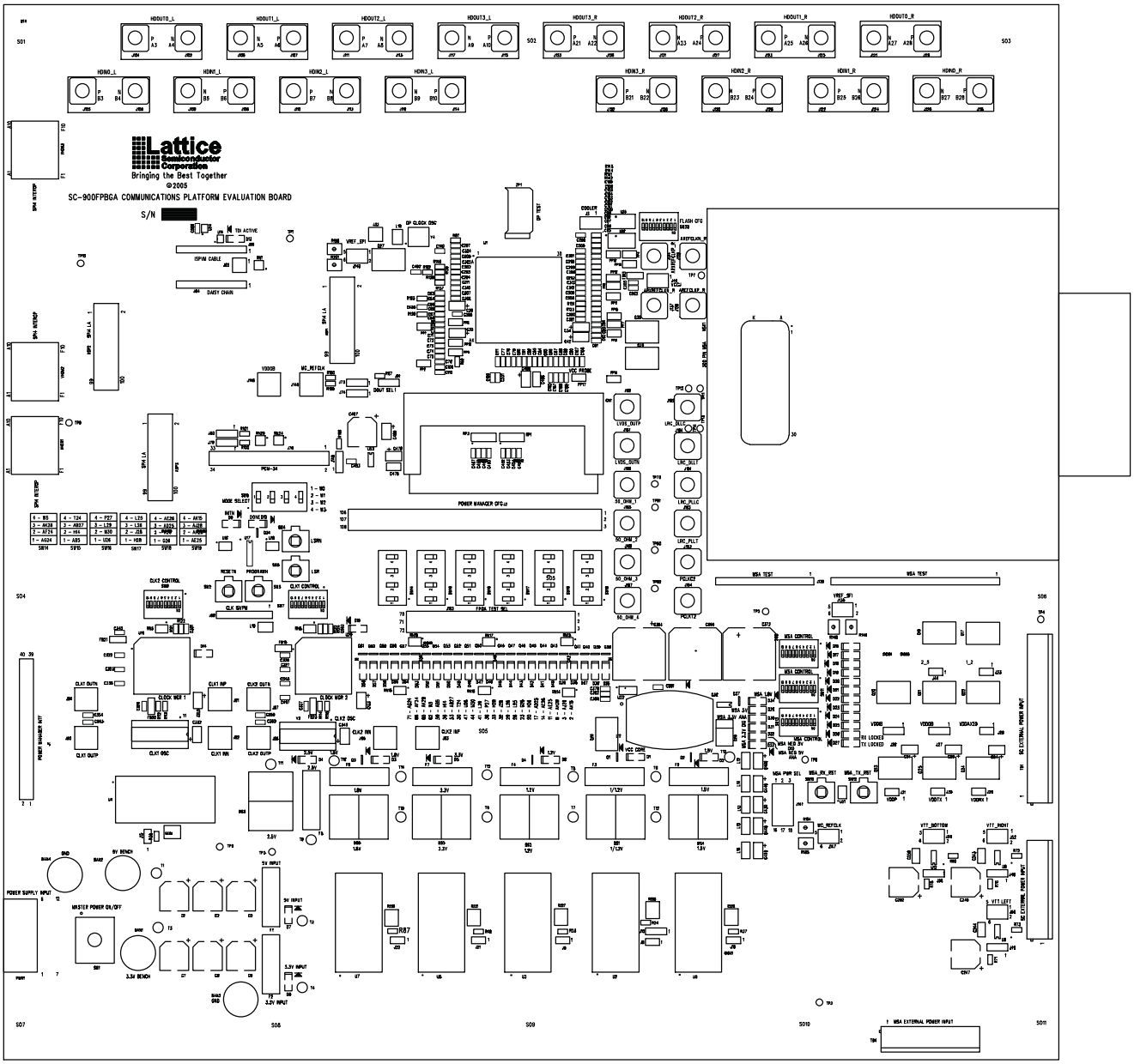
Figure 2. LatticeSC Communications Platform Evaluation Board Block Diagram



The contents of this user's guide include top-level functional descriptions of the various portions of the evaluation board, descriptions of the on-board connectors, diodes and switches and a complete set of schematics of the board. Figure 3 shows the functional partitioning of the board.

Lattice makes its best effort to provide evaluation board designs to help users with evaluation and development. However it remains the user's responsibility to verify proper and reliable operation of Lattice products in their end application by consulting documentation provided by Lattice. Differences in component selection and/or PCB layout in the user's application may significantly affect circuit performance and reliability.

Figure 3. LatticeSC Communications Platform Evaluation Board Functional Partitioning



LatticeSC Device

This board features a LFSC25E FPGA with a 1.2V core supply in the 900-ball fpBGA (1mm pitch) package. A complete description of this device can be found in the LatticeSC Family Data Sheet on the Lattice web site at www.latticesemi.com.

Note: The connections referenced in this document refer to the LFSC25E device. Available I/Os and associated PURESPEED™ I/O banks may differ for other densities within this device family.

Applying Power to the Board

The LatticeSC Communications Platform Evaluation Board is delivered ready to power-on. The evaluation system is shipped with AC line cord for the included multi-voltage power supply. Follow these steps to power-on the board.

1. Connect the power supply unit to the board using the attached rainbow cable from the power supply to the power input connector on the board (PWR1).
2. Confirm that the ON-OFF switch, SW1, is in the OFF position. Back towards the Molex input connector.
3. Plug the desktop power supply AC line cord into an electrical outlet supplying the appropriate voltage.
4. Turn on switch on desktop power supply unit. Toggle switch is located on the side of the unit.
5. Turn SW1 to the ON position. The power indicators for all regulator modules should illuminate, indicating output from the regulators.

Power Supplies

(For schematics, see Appendix A, Figures 7-10)

Many methods can be used to provide power to the board. The board is equipped to accept a main supply via the PWR1 connection. This connection is provided to use with the switching supply provided with the kit using a Molex 87427-1203 connector.

This power supply sources the needed intermediate power and is used for turnkey evaluations without the need to control and supply power from other sources. This supply provides intermediate 5V DC and 3.3V DC to the secondary power stages of the PCB. The intermediate supplies can also be sourced from adequately sized benchtop supplies via banana jacks located near the PWR1 input connector.

Table 1. External Power Supply Input Jack (See Appendix A, Figure 5)

BAN1	Bench Supply for 3.3V Intermediate Supply Input
BAN2	Bench Supply for Intermediate Supply 5.0V Input
BAN3	Ground connection
BAN4	Ground connection

The intermediate supplies are fused on-board with indicating fuses and have green LEDs to indicate power GOOD status of the intermediate supplies

Table 2. Input Supply Fuses/Indicators (See Appendix A, Figure 5)

F1	5.0VDC Input Indicator Fuse
F2	3.3VDC Input Indicator Fuse
D7	5.0VDC Input Source Good Indicator
D8	3.3VDC Input Source Good Indicator

SW1 is used to enable the off-board switching power supply module as well as discrete power inputs from a benchtop power supply. The intermediate power supplies are supplied to the secondary POL supply modules. These five independent supplies, U2, U3, U4, U5, and U6, are used to provide the necessary power supplies for the LatticeSC FPGA and other on-board devices. All five DC/DC outputs are fused on board with indicating fuses and have GREEN power good indicating LEDs.

Table 3. Board Power Supply Fuses (See Appendix A, Figure 6)

F3	1.0V/1.2V POL Source Indicator Fuse
F4	1.2V POL Source Indicator Fuse
F5	2.5V POL Source Indicator Fuse
F6	1.5V POL Source Indicator Fuse
F7	3.3V POL Source Indicator Fuse
F8	1.8V POL Source Indicator Fuse

Table 4. Board Power Supply Indicators (See Appendix A, Figure 6)

D1	1.0V/1.2V VCC Core Source Good Indicator
D2	1.5V Source Good Indicator
D3	1.8V Source Good Indicator
D4	2.5V Source Good Indicator
D5	3.3V Source Good Indicator
D6	1.2V Source Good Indicator

External power can be alternatively connected rather than the POL DC/DC modules. Barrier strips can isolate the supplies allowing for benchtop supplies to source power the secondary rails. Table 5 shows these barrier connections.

Table 5. Board Supply Disconnects (See Appendix A, Figure 6)

BS1	Screw terminal for VCC Core
BS2	Screw terminal for 1.2V source/On Board disconnect
BS3	Screw terminal for 2.5V source/On Board disconnect
BS4	Screw terminal for 1.5V source/On Board disconnect
BS5	Screw terminal for 3.3V source/On Board disconnect
BS6	Screw terminal for 1.8V source/On Board disconnect

The on-board power supplies can be adjusted by trimming potentiometers. The on-board supplies can be margined up or down from the nominal operating level. The variable resistors are outlined in Table 6.

Table 6. Variable Resistors for Power Supply Margining

Adjust	Supply
R226	CORE
R228	1.5V
R230	1.8V
R227	1.2V
R229	2.5V
R230	3.3V

The board is designed to provide a standard platform as well as a diagnostic platform for device evaluations. The board is capable of user provisioning that can provide the means to change and re-assign supplies other than the factory supplied settings. These settings are accomplished by reassignment of two-position jumpers. Two-position shunts such as AMP/Tyco Electronics part number 881545-2 are used for field PCB provisioning.

The POL DC/DC modules, U2, U3, U4, U5, and U6, include pins to control features of the modules. These DC modules convert either the 5V DC or 3.3V DC input.

Table 7. Board Supply Voltage Source Selectors (See Appendix A, Figures 7 and 10)

J23	VCC12 Power Source Select
J25	VCCAUX Power Source Select
J28	VDDAX25 Power Source Select
J29	VDDRX Power Source Select
J30	VDDTX Power Source Select
J31	VDDP Power Source Select
J26	VDDIB Power Source Select
J27	VDDOB Power Source Select

External Power Interface

Power sources can be independently sourced to the board via terminal blocks located on the PCB edge. This interface allows the user to provide power sources from benchtop power supplies. The table below identifies the terminals of the interface.

Table 8. External Power Source Inputs (See Appendix A, Figure 5)

TB1		TB2	
1	VDDP	1	VTT RIGHT
2	VDDTX	2	VTT BOTTOM
3	VDDRX	3	VTT LEFT
4	VDDAX25	4	VCCIO18
5	VDDOB	5	VCCIO25
6	VDDIB	6	GND
7	VCCAUX	7	GND
8	VCC12		
9	VCC		
10	VCCJ		
11	GND		
12	GND		

J10 is used to control the output voltage setting of the U2 DC/DC module. A two-position shunt will connect the appropriate trim resistor to the module.

Exclusively the LatticeSC device for VCC core supply uses this power source.

Table 9. VCC Core Voltage Select (See Appendix A, Figure 6)

J10	VCC Core DC/DC Module Output/ [1:2]= 1V, [3-2]= 1.2V

VCCIO1 Selection

VCCIO1 is board programmable using the 2X2 0.1 headers. These jumpers select the input for the VCCIO1 voltage.

Table 10. VCCIO1 Bank Voltage Select (See Appendix A, Figure 9)

J32	VCCIO1 Power Source Select (2.5V or 3.3V on-board generated)

VCCIO18 and VCCIO25

VCCIO to banks 2-7 have predetermined settings and can be supplied from external benchtop supplies by using the external terminal block. The associated VCCIO source will enter the board via a terminal block TB2 (see Appendix A, Figure 5).

VCCIO Banks 2, 3, 6 and 7 are planed together on the board and notated as VCCIO25.

Banks 4 and 5 are planed together and notated as VCCIO18.

- VCCIO25 is board connected to a 2.5V supply.
- VCCIO18 is board connected to a 1.8V supply.

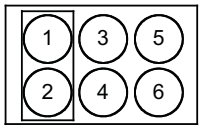
VCCAUX

VCCAUX can be board-programmed to connect to a common 2.5V supply. Placing a jumper between on J44 (see Appendix A, Figure 10) connects all VCCAUX device pins to a board-generated 2.5V supply. A connection to terminal block TB1 (see Appendix A, Figure 5) is available.

VCCJ

The VCCJ supply of the LatticeSC device can be selected via J46 (see Appendix A, Figure 10). J46 is a 2x3 0.1header that can select VCCJ to be 3.3V, 2.5V, or 1.8V using a jumper between the supply voltage and adjacent pin of J46.

Table 11. VCCJ Supply Selector (See Appendix A, Figure 10)

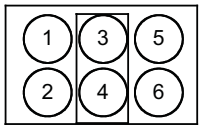


2	3.3V
4	2.5V
6	1.8V

VTT

On-board voltage regulators are available for generation of VTT supplies for use with SSTL and HSTL I/Os. These regulators are designed to provide precision voltages for the LatticeSC VTT pins per bank. The regulators can be shut down according to the following.

Table 12. VTT Generation Source (See Appendix A, Figure 11)



J48	Regulated VTT Right Source (U8) Shutdown
J56	Regulated VTT Left Source (U12) Shutdown
J49	Regulated VTT Bottom Source (U9) Shutdown

3x2-pin headers select the source of the VTT supplies. This selection is between the on-board VTT regulators, external source, or AC-coupled ground. A jumper between pins 3 and 4 will connect the on-board VTT regulator to the device, jumper between pins 1 and 2 will connect VTT to an external connection via the terminal block, and an AC-coupled ground is connected by placing a jumper between pins 3 and 5.

Table 13. VTT Termination Type (See Appendix A, Figure 11)

J52	VTT Right Selector
J59	VTT Bottom Selector
J50	VTT Left Selector

Programming/FPGA Configuration

Two programming headers are provided on the evaluation board, providing access to the LatticeSC JTAG port. The standard 1x10 pin header is available for compatibility with all Lattice download cables. The 10-pin 0.100"pitch header connector which plugs directly into a mating connector provided.

Note: An ispDOWNLOAD® cable is included with this board, and with each ispLEVER® design tool shipment. Cables may also be purchased separately from Lattice.

ispVM Download Interface

J68 is an 10-pin JTAG connector used in conjunction with the ispVM USB download cable to program and control the device.

Table 14. ispVM JTAG Connector (See Appendix A, Figure 13)

Pin 1	VCC
Pin 2	TDO
Pin 3	TDI
Pin 4	PROGRAMN
Pin 5	NC
Pin 6	TMS
Pin 7	GND
Pin 8	TCK
Pin 9	DONE
Pin 10	INITN

Download Procedures

Requirements:

- PC with ispVM System v.14.4 (or later) programming management software, installed with appropriate drivers (USB driver for USB Cable, Windows NT/2000/XP parallel port driver for ispDOWNLOAD Cable).

  Note: An option to install these drivers is included as part of the ispVM System setup.

- ispDOWNLOAD Cable (pDS4102-DL2A, HW7265-DL3A, HW-USB-1A, etc.)

JTAG Download

The LatticeSC device can be configured easily via its JTAG port. The device is SRAM-based; it must remain powered on to retain its configuration when programmed in this fashion.

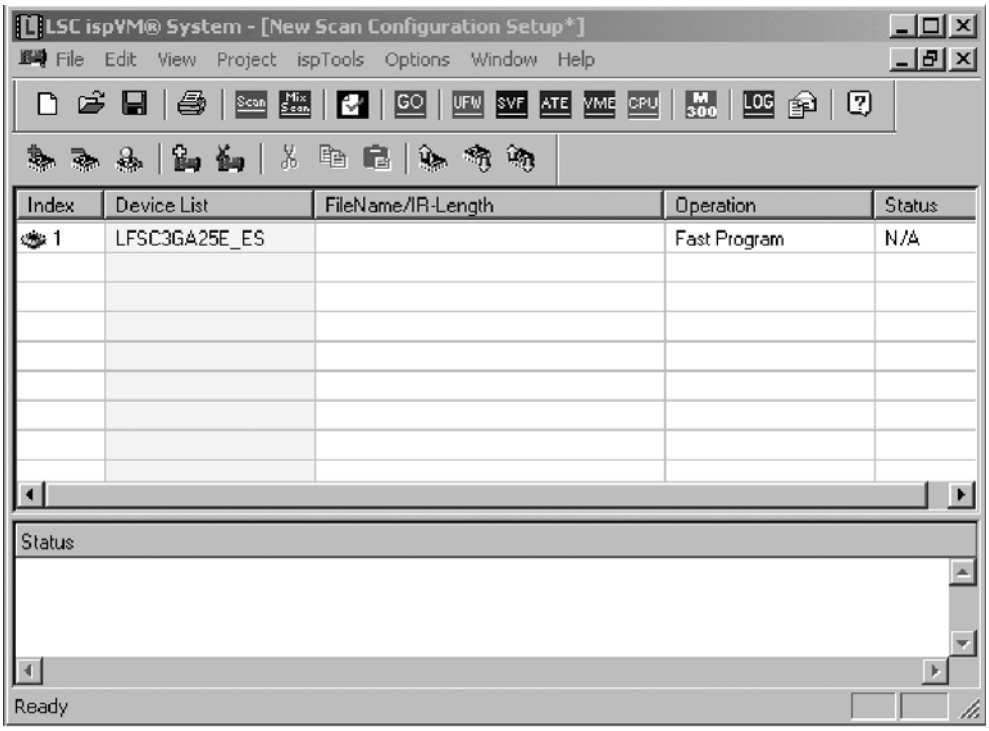
1. Connect the ispDOWNLOAD cable to the appropriate header. J68 is used for the 1x10 cable.

   Important Note: *The board must be un-powered when connecting, disconnecting, or reconnecting the ispDOWNLOAD Cable. Always connect the ispDOWNLOAD Cable's GND pin (black wire), before connecting any other JTAG pins. Failure to follow these procedures can in result in damage to the LatticeSC FPGA device and render the board inoperable.*

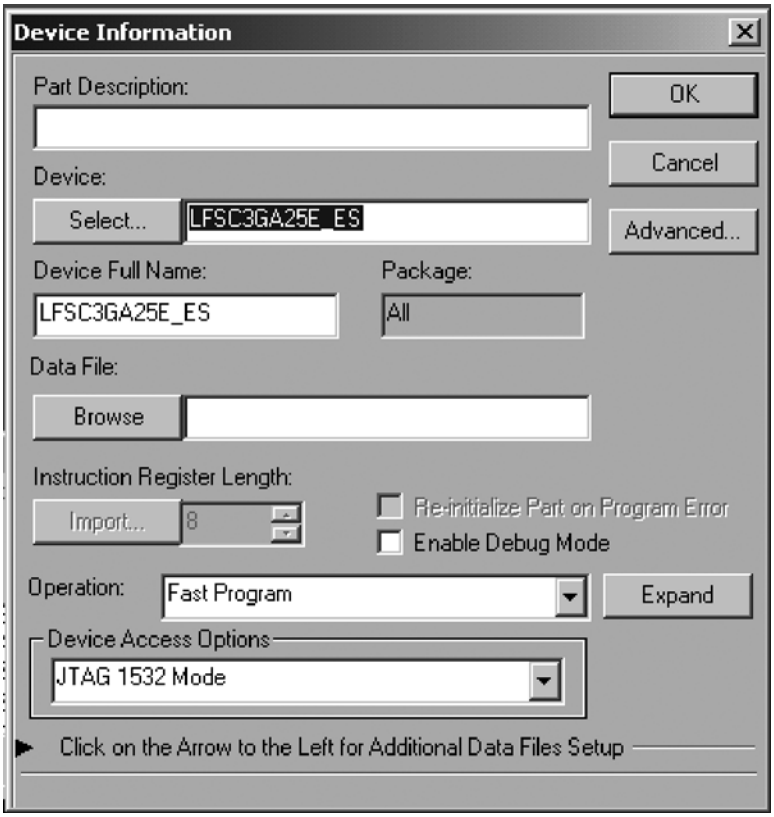
2. Connect the LatticeSC Evaluation Board to the appropriate power sources and power up board.

3. Start the ispVM System software.

4. Press the 'SCAN' button located in the toolbar. The LatticeSC device should be automatically detected.



5. Double-click the device to open the device information dialog. In the device information dialog, click the Browse button located under 'Data File'. Locate the desired bitstream file (.bit or .rbt). Click OK to both dialog boxes. The 'Operation' should be 'Fast Program' and 'Device Access Options' set to 'JTAG 1532 Mode'.



6. Click the green 'GO' button. This will begin the download process into the device. Upon successful download, the device will be operational.

Note: Bitstreams that have been compressed with Bitgen will not download via the JTAG configuration port.

Header Connections

Standard 0.1 headers are provided for interconnecting points on the board. This can be accomplished with 0.100 IDC connectors and ribbon cable for bus connections or 0.025 pin socket patch cords (such as Pomona Electronics #5948 www.pomonelectronics.com). Most connections can be made using two-pin shunts provided with the board kits.

Configuration Status Indicators

(see Appendix A, Figure 13)

These LEDs indicate the status of configuration to the FPGA.

- D9 (RED) illuminated, this indicates that the programming was aborted or reinitialized driving the INITN output low.
- D10 (GREEN) is illuminated, this indicates the successful completion of configuration by releasing the open collector DONE output pin.
- D13 (GREEN) will flash indicating TDI activity.

PROGRAMN and RESETN

(see Appendix A, Figure 13)

These push button switches assert/de-assert the logic levels on the PROGRAMN (SW3) and RESETN (SW2). Depressing the button drives a logic level "0" to the device.

MODE [3:0]

(see Appendix A, Figure 13)

The FPGA MODE pins can be selected via the SW6 DIP-switch. These settings must be selected accordingly for the particular configuration mode. However for ispVM downloading via the download cable, the settings of these pins are required.

FPGA Loader Interface

(see Appendix A, Figure 13)

A 2x17 header is provided to connect the LatticeSC to the Serial Configuration Module (SCM) or Parallel Configuration Module (PCM). These modules are available from Lattice and are utilized to verify the parallel and serial loading of the configuration memory.

On-Board Flash Memory

(see Appendix A, Figure 13)

Two memory devices (U25 and U26) are on-board for non-volatile configuration memory storage. SW20 is used to control writing and reading from the memory. When used to configure the board, the user must set the MODE[3:0] pins accordingly [0101] with SW6. Refer to Lattice technical note number TN1100, *SPI Serial Flash Programming Using ispJTAG on LatticeSC FPGAs* for recommended procedures and software usage.

To use both SPI Flash devices to program the LatticeSC device, the user must write to the Flash devices individually. This is accomplished by setting SW20 accordingly. Writing to Flash #1(U26), close 3 and 5 switch positions (ON) and open all others.

Writing to Flash #2(U25), close 2 and 4 switch positions (ON) and open all others.

For reading from the Flash devices individually, use the same switch settings and described for writing.

For reading from both Flash devices in cascading format, close switch positions (1, 3, 4, 5, 8).

FPGA Clock Management

(see Appendix A, Figure 14)

The evaluation board includes various features for generating and managing on-board clocks. The clocks are generated either from input provided from SMAs (see table below) or from crystal oscillators (Y1 and Y2), which are socketed. Both of these input clock sources are routed through the Lattice ispClock5620 programmable clock manager devices (U19 and U20). These clock management devices allow for clock synthesis and buffering.

Table 15. External ispCLOCK5620 Reference Clock Input Connections

J91	U19 Reference + Input
J92	U19 Reference - Input
J93	U20 Reference + Input
J95	U20 Reference - Input

U19 and U20 are Lattice ispClock5620 In-System-Programmable Analog Circuit allows designers to implement clock distribution networks supporting multiple, synchronized output frequencies using a single integrated circuit.

By integrating a Phase-Locked Loop (PLL) along with multiple output dividers, the ispClock5620 can derive up to five separate output frequencies from a single input reference frequency. PAC-Designer® software (available from the Lattice web site at www.latticesemi.com) is used to program the ispClock features.

The ispClock5620 supports reference clocks in the range of 10 to 320 MHz. The duty cycle of the clock source need not be 50%; the only requirement is that both the HIGH and LOW times of this signal must be 1.25ns or longer. The following standards are supported with either minimal or no external components: LVTTL / LVCMOS / SSTL2 / SSTL3 / HSTL / LVDS / LVPECL.

When the ispClock5620 is in a LOCKED state, the LOCK output pin goes LOW. The LOCKN pins are connected to amber LEDs, D14 and D15, that will illuminate when the LOCKN pin goes low. The lock detector has two operating modes; phase lock mode and frequency lock mode. In phase lock mode, the LOCK signal is asserted if the phases of the reference and feedback signals match. In frequency lock mode the LOCK signal is asserted when the frequencies of the feedback and reference signals match.

Table 16. ispClock Lock Indicators (See Appendix A, Figure 14)

D14	CLK5560 #1(U19) PLL Lock Indicator- Locked when Lit
D15	CLK5560 #2 (U20) PLL Lock Indicator- Locked when Lit

U19 and U20 are controlled by SW8 and SW7 respectively. These DIP switches control the ispClock devices. The reference clock selection and device reset is controlled using the switches. The switches controlling the ispClock outputs can be synchronously controlled by the SGATE output on a bank-by-bank basis or tri-stated on an output-by-output basis using the OEXb and OEYb inputs. All outputs may be tri-stated by bringing the GOEb input high.

The VCCO voltage is board connected to 2.5V.

J98 is provided to allow reprogramming of the ispClock devices. Both devices are in the same JTAG chain. Please refer to the ispClock documentation for altering the designs. The output clocks, U19 and U20, are routed to devices to provide system level clocking. These pre-defined board clocks are routed to input LatticeSC input clock pins for SERDES reference clocks, primary clocks, PLL inputs and DLL inputs as well as connection to the external MSA (MSA1) transponder site. There are also two output pairs available via 50-ohm terminated SMA connections for off-board interconnections.

Table 17. ispClock Output SMA Connections (See Appendix A, Figure 14)

J90	U19 Reference + Output
J94	U19 Reference - Output
J96	U20 Reference + Output
J97	U20 Reference - Output

SERDES

SERDES Reference Clock

J128/J129 are provided to allow a DC-coupled reference clocks from an external clock generator. This reference clock is for the Quad PCS 3E0.

J134/137 are available for the same Quad to provide a separate Rx Clock.

For Quad PCS 360, this reference clock is sourced from the ispClock device.

The following 50-ohm terminated SMA connectors are provided the supply reference clocks directly to the LatticeSC device.

Table 18. SERDES Reference Clock Input Connectors (See Appendix A, Figure 15)

J128	A_REFCLKN_R
J129	A_REFCLKP_R

SERDES Channels

DC coupled SMA connectors connect to the SERDES Tx and Rx channels of both the Quad A SERDES on the left and right device sides. These pins are directly coupled to the designated SMA connector creating a path for both input and output differential data.

Table 19. SERDES Connectors (See Appendix A, Figure 15)

J105	A_HDINN0_L	J120	A_HDINN0_R
J103	A_HDINP0_L	J118	A_HDINP0_R
J108	A_HDINN1_L	J124	A_HDINN1_R
J106	A_HDINP1_L	J122	A_HDINP1_R
J112	A_HDINN2_L	J130	A_HDINN2_R
J110	A_HDINP2_L	J126	A_HDINP2_R
J116	A_HDINN3_L	J135	A_HDINN3_R
J114	A_HDINP3_L	J132	A_HDINP3_R
J102	A_HDOUTN0_L	J121	A_HDOUTN0_R
J104	A_HDOUTP0_L	J119	A_HDOUTP0_R
J109	A_HDOUTN1_L	J125	A_HDOUTN1_R
J107	A_HDOUTP1_L	J123	A_HDOUTP1_R
J113	A_HDOUTN2_L	J131	A_HDOUTN2_R
J111	A_HDOUTP2_L	J127	A_HDOUTP2_R
J117	A_HDOUTN3_L	J136	A_HDOUTN3_R
J115	A_HDOUTP3_L	J133	A_HDOUTP3_R

Note: For accurate electrical analysis of SERDES transmit outputs, it is recommended to terminate the unused output SMAs with 50-ohm terminations.

Multi-Chip Alignment

(see Appendix A, Figure 15)

ZP1 connector interconnects test points for multi-chip alignment pins. It is not populated for general use. This connector type is an Amp Z-Pack 2mm header. A cable similar to one from W.L Gore (www.wlgore.com) P/N 2MMA3192-01 adapts the 2mm Z-Pack to individual SMA connectors and is useful to observe signals or connect to other test devices

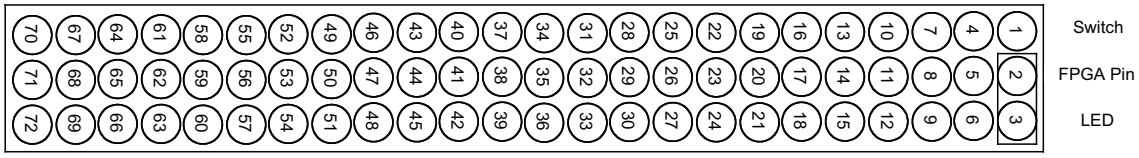
FPGA Test Pins

(see Appendix A, Figure 21)

General-purpose FPGA pins are available via a 36 x 3 pin header. The use of this header connects FPGA pins to either a Switch or LED based on the user's requirement by placing a jumper across the appropriate pins of J152. The switch nets are tied to 4-position DIP switches designated according to the following table.

Table 20. FPGA Test Selector Header (See Appendix A, Figure 21)

Switch	Pin	Netname	Pin	BGA	Pin	NetName	LED
SW19D	1	Switch1	2	AK15	3	RED1	D35
SW19C	4	Switch2	5	AJ28	6	RED2	D36
SW19B	7	Switch3	8	AH28	9	RED3	D37
SW19A	10	Switch4	11	AE25	12	RED4	D38
SW18D	13	Switch5	14	AE26	15	RED5	D39
SW18C	16	Switch6	17	AD25	18	YELLOW1	D40
SW18B	19	Switch7	20	H26	21	YELLOW2	D41
SW18A	22	Switch8	23	G26	24	YELLOW3	D42
SW17D	25	Switch9	26	L25	27	YELLOW4	D43
SW17C	28	Switch10	29	L26	30	YELLOW5	D44
SW17B	31	Switch11	32	J28	33	GREEN1	D45
SW17A	34	Switch12	35	H28	36	GREEN2	D46
SW16D	37	Switch13	38	P27	39	GREEN3	D47
SW16C	40	Switch14	41	L29	42	GREEN4	D48
SW16B	43	Switch15	44	M30	45	GREEN5	D49
SW16A	46	Switch16	47	U26	48	BLUE1	D50
SW15D	49	Switch17	50	T24	51	BLUE2	D51
SW15C	52	Switch18	53	AB27	54	BLUE3	D52
SW15B	55	Switch19	56	H14	57	BLUE4	D53
SW15A	58	Switch20	59	AB5	60	BLUE5	D54
SW14D	61	Switch21	62	W5	63	ORANGE1	D55
SW14C	64	Switch22	65	AK28	66	ORANGE2	D56
SW14B	67	Switch23	68	AF24	69	ORANGE3	D57
SW14A	70	Switch24	71	AG24	72	ORANGE4	D58



Note: LEDs will illuminate if connected to an un-programmed FPGA pin. It is recommended that a pull-down be programmed on FPGA output pins.

Test SMA Connections

General-purpose FPGA pins are available via SMA test connections. These connections are designed to permit evaluations of several types of FPGA I/O buffers. The use of several termination schemes permit easy interfaces for the type of buffer.

Table 21. FPGA I/O Test SMA Connectors (See Appendix A, Figure 21)

SMA Designation	Name	Signal	900-BGA	Termination Description	Termination Resistor(s)
J154	LVDS_INP	PR27C/PCLKT2_2	P26	DC-Coupled	n/a
J153	LVDS_INN	PR27D/PCLKC2_2	N27	DC-Coupled	n/a
J182	LVDS_OUTP	PR57A/LRC_DLLT_IN	AF29	100-ohm Differential Termination	R205
J181	LVDS_OUTN	PR57B/LRC_DLLC_IN	AF28	100-ohm Differential Termination	R205
J161	LRC_PLLC	PB69B/LRC_PLLC_IN_A	AH30	50-ohm Ground Termination	R215
J163	LRC_PLLT	PB69A/LRC_PLLT_IN_A	AJ30	50-ohm Ground Termination	R214
J162	LRC_DLLC	PB68B/LRC_DLLC_IN_C	AH29	50-ohm Ground Termination	R217
J164	LRC_DLLT	PB68A/LRC_DLLT_IN_C	AJ29	50-ohm Ground Termination	R216
J166	50_OHM_1	PB61B	AH27	50-ohm VTT/GND	R222/R219
J165	50_OHM_2	PB61A	AH26	50-ohm VTT/GND	R223/R218
J168	50_OHM_3	PB60C	AE22	50-ohm VTT/GND	R224/R221
J167	50_OHM_4	PB60B	AK29	50-ohm VTT/GND	R225/R220

LSR and LSRN

(see Appendix A, Figure 13)

These push button switches assert/de-assert the logic levels on the LSR (SW5) and LSRN (SW4).

Depressing the LSRN (SW4) drives a logic level "0" to the device.

Depressing the LSR (SW5) drives a logic level "1" to the device.

300-pin MSA Transponder Interface

(see Appendix A, Figure 16)

MSA1 connector provides an interface for interoperability to 300-pin SFI4.2 or XSBI transponders. The interface is complete with high-speed parallel connections to the LatticeSC device as well as clocking, status, control, and power. The interface pin-out is outlined in the table below.

Table 22. SFI-XSBI 300-Pin Connector Standard (See Appendix A, Figure 16)

Receiver

K	J	H	G	F	E	D	C	B	A
5.0V Analog	*RxTRACE*	Frame GND	RxDout12P	*APS Digital*	RxDout8P	Digital GND	RxDout4P	Digital GND	RxDout0P
5.0V Analog	FFU	Frame GND	RxDout12N	*APS Digital*	RxDout8N	Digital GND	RxDout4N	Digital GND	RxDout0N
RxRATESEL0	*RxRATESEL1*	*APDTEMPMON*	Digital GND	RxPOWMON	Digital GND	*I2CAD0*	Digital GND	*RxDTV*	Digital GND
3.3V Analog	NUC	Frame GND	RxDout13P	3.3V Digital	RxDout9P	Digital GND	RxDout5P	Digital GND	RxDout1P
3.3V Analog	NUC	Frame GND	RxDout13N	3.3V Digital	RxDout9N	Digital GND	RxDout5N	Digital GND	RxDout1N
RxRESET	NUC	*DLOOPENB*	Digital GND	*RxPOWALM*	Digital GND	*I2CAD1*	Digital GND	*RxMUTEDout*	Digital GND
3.3V Analog	FFU	Analog GND	RxDout14P	3.3V Digital	RxDout10P	Digital GND	RxDout6P	Digital GND	RxDout2P
3.3V Analog	FFU	Analog GND	RxDout14N	3.3V Digital	RxDout10N	Digital GND	RxDout6N	Digital GND	RxDout2N
RxMUTEPOCLK	NUC	FFU	Digital GND	*RxSIGMON*	Digital GND	*I2CAD2*	Digital GND	*RxLCKREF*	Digital GND
-5.2V Analog	*APS Sense*	Analog GND	RxDout15P	-5.2V Digital	RxDout11P	Digital GND	RxDout7P	Digital GND	RxDout3P
-5.2V Analog	*APS Set*	Analog GND	RxDout15N	-5.2V Digital	RxDout11N	Digital GND	RxDout7N	Digital GND	RxDout3N
RXMUTEMCLK	NUC	FFU	Digital GND	*RxSIGALM*	Digital GND	*MOD_RESET*	Digital GND	*RxMCLKSEL*	Digital GND
-5.2V Analog	FFU	Analog GND	FFU	-5.2V Digital	RxPOCLKP	Digital GND	*RxMCLKP*	Digital GND	RxREFCLKP
-5.2V Analog	*RxALM INT*	Analog GND	FFU	-5.2V Digital	RxPOCLKN	Digital GND	*RxMCLKN*	Digital GND	RxREFCLKN
I2CCLOCK	NUC	*ALM INT*	Digital GND	*RxREFSEL*	Digital GND	FFU	Digital GND	*RxLOCKERR*	Digital GND

Receiver power and GND supplies
Receiver DC signals
622 differential signals

NUC = No user connection
FFU = Reserved for future use
Italics = Optional feature

Transmitter

K	J	H	G	F	E	D	C	B	A
5.0V Analog	*TxALM INT*	Analog GND	TxDin12P	*APS Digital*	TxDin8P	Digital GND	TxDin4P	Digital GND	TxDin0P
5.0V Analog	FFU	Analog GND	TxDin12N	*APS Digital*	TxDin8N	Digital GND	TxDin4N	Digital GND	TxDin0N
I2CDATA	NUC	*LsTUNE0*	Digital GND	LsBIASMON	Digital GND	LsPOWMON	Digital GND	*TxSKEWSEL0*	Digital GND
3.3V Analog	*ModBIASMON*	Analog GND	TxDin13P	3.3V Digital	TxDin9P	Digital GND	TxDin5P	Digital GND	TxDin1P
3.3V Analog	*ModBIASALM*	Analog GND	TxDin13N	3.3V Digital	TxDin9N	Digital GND	TxDin5N	Digital GND	TxDin1N
TxRATESEL0	*TxRATESEL1*	*LsTUNE1*	Digital GND	LsENABLE	Digital GND	*LsTEMPMON*	Digital GND	*TxSKEWSEL1*	Digital GND
3.3V Analog	FFU	Analog GND	TxDin14P	3.3V Digital	TxDin10P	Digital GND	TxDin6P	Digital GND	TxDin2P
3.3V Analog	FFU	Analog GND	TxDin14N	3.3V Digital	TxDin10N	Digital GND	TxDin6N	Digital GND	TxDin2N
TxRESET	NUC	*LsTUNE2*	Digital GND	*LsBIASALM*	Digital GND	*TxPHSAD30*	Digital GND	*LsTWEAK*	Digital GND
-5.2V Analog	NUC	Frame GND	TxDin15P	-5.2V Digital	TxDin11P	Digital GND	TxDin7P	Digital GND	TxDin3P
-5.2V Analog	NUC	Frame GND	TxDin15N	-5.2V Digital	TxDin11N	Digital GND	TxDin7N	Digital GND	TxDin3N
TxFIFO RES	NUC	*LLOOPENB*	Digital GND	*LsTEMPALM*	Digital GND	*TxPHSAD31*	Digital GND	*TxPICLKSEL*	Digital GND
-5.2V Analog	*LsWAVEMON*	Frame GND	TxPICLKP	-5.2V Digital	TxPCLKP	Digital GND	*TxMCLKP*	Digital GND	TxREFCLKP
-5.2V Analog	*TxTRACE*	Frame GND	TxPICLKN	-5.2V Digital	TxPCLKN	Digital GND	*TxMCLKN*	Digital GND	TxREFCLKN
TxFIFO ERR	NUC	*TxLINETIMSEL*	Digital GND	*TxREFSEL*	Digital GND	*LsPOWALM*	Digital GND	TxLOCKERR	Digital GND

Transmitter power and GND supplies
Transmitter DC signals
622 differential signals

NUC = No user connection
FFU = Reserved for future use
Italics = Optional feature

Table 23 outlines the physical connections between the 300-pin MSA connector and the LatticeSC device.

Table 23. SFI4/XSBI Interface Pinout (See Appendix A, Figure 16)

LatticeSC	To XPNDR	MSA	LatticeSC	FROM XPNDR	MSA
D29	MSA_TX_P_00	A16	R27	MSA_RX_P_00	A1
D30	MSA_TX_N_00	A17	T27	MSA_RX_N_00	A2
G28	MSA_TX_P_01	A19	V28	MSA_RX_P_01	A4
F28	MSA_TX_N_01	A20	W28	MSA_RX_N_01	A5
G27	MSA_TX_P_02	A22	T30	MSA_RX_P_02	A7
H27	MSA_TX_N_02	A23	U30	MSA_RX_N_02	A8
L27	MSA_TX_P_03	A25	V26	MSA_RX_P_03	A10
M27	MSA_TX_N_03	A26	W26	MSA_RX_N_03	A11
E29	MSA_TX_P_04	C16	V29	MSA_RX_P_04	C1
E30	MSA_TX_N_04	C17	W29	MSA_RX_N_04	C2
F29	MSA_TX_P_05	C19	V30	MSA_RX_P_05	C4
G29	MSA_TX_N_05	C20	W30	MSA_RX_N_05	C5
H30	MSA_TX_P_06	C22	Y27	MSA_RX_P_06	C7
J30	MSA_TX_N_06	C23	W27	MSA_RX_N_06	C8
K30	MSA_TX_P_07	C25	Y30	MSA_RX_P_07	C10
L30	MSA_TX_N_07	C26	AA30	MSA_RX_N_07	C11
P28	MSA_TX_P_08	E16	AA25	MSA_RX_P_08	E1
R28	MSA_TX_N_08	E17	AB25	MSA_RX_N_08	E2
N28	MSA_TX_P_09	E19	AD30	MSA_RX_P_09	E4
N29	MSA_TX_N_09	E20	AE30	MSA_RX_N_09	E5
P29	MSA_TX_P_10	E22	AB28	MSA_RX_P_10	E7
R29	MSA_TX_N_10	E23	AC28	MSA_RX_N_10	E8
T28	MSA_TX_P_11	E25	AD29	MSA_RX_P_11	E10
U28	MSA_TX_N_11	E26	AE29	MSA_RX_N_11	E11
M29	MSA_TX_P_12	G17	AF30	MSA_RX_P_12	G1
N30	MSA_TX_N_12	G16	AG30	MSA_RX_N_12	G2
T29	MSA_TX_P_13	G19	AB26	MSA_RX_P_13	G4
U29	MSA_TX_N_13	G20	AC26	MSA_RX_N_13	G5
P30	MSA_TX_P_14	G22	AC27	MSA_RX_P_14	G7
R30	MSA_TX_N_14	G23	AD28	MSA_RX_N_14	G8
U27	MSA_TX_P_15	G25	AD26	MSA_RX_P_15	G10
V27	MSA_TX_N_15	G26	AC25	MSA_RX_N_15	G11

MSA Power Supplies

(See Appendix A, Figure 17)

Table 24. MSA Power Indicators (See Appendix A, Figure 17)

D34	MSA +1.8VDC Auxiliary Supply Good Indicator
D30	MSA +3.3VDC Analog Supply Good Indicator
D31	MSA +3.3VDC Digital Supply Good Indicator
D29	MSA +5VDC Analog Supply Good Indicator
D32	MSA -5VDC Analog Supply Good Indicator
D33	MSA -5VDC Digital Supply Good Indicator

J141 is a 3x6-pin header is board programmed using jumpers. The header selects between use of on-board regulated power supplies or connections to terminal block TB4 for connection to external supplies for supplying the 300-pin module.

MSA Status Indicators

The status signals of the MSA interface are observed via the LED indicators listed below

Table 25. MSA Status Indicators (See Appendix A, Figure 16)

D17	MSA ALM_INT Indicator- Error when lit
D24	MSA LSBIASALM Indicator- Error when lit
D22	MSA LSPOWALM Indicator- Error when lit
D23	MSA LSTEMPALM Indicator- Error when lit
D21	MSA MODBIAS_ALM Indicator- Error when lit
D19	MSA RXALM_INT Indicator- Error when lit
D26	MSA RXLOCKERR Indicator- RX PLL Locked when lit
D20	MSA RXPOWALM Indicator- Error when lit
D16	MSA RXSIGALM Indicator- Error when lit
D18	MSA TXALM_INT Indicator- Error when lit
D25	MSA TXFIFOERR Indicator- Error when lit
D27	MSA TXLOCKERR Indicator- TX PLL Locked when lit

J139 and J140 provide connections to analog MSA outputs and undetermined use pins respectively.

SW10 and SW12 are push-button switches used to drive the MSA RXRESET and TXRESET pins to logic "0" when depressed.

MSA Input Switches

The 300-pin MSA pin out standard includes logical inputs to various transponder implementations. The evaluation board is equipped with DIP switches that are connected to the MSA pins for the users to setup their particular transponder. Table 26 outlines the switch and signal.

Table 26. MSA Static input switches (See Appendix A, Figure 16)

Switch	Position	Signal
9	1	MOD-RESET
9	2	I2CAD2
9	3	I2CAD1
9	4	I2CAD0
9	5	TXPICLKSEL
9	6	TXSKEWSEL1
9	7	TXSKEWSEL0
9	8	RXMCLKSEL
9	9	RXLCKREF
9	10	RXMUTED-OUT
11	1	LSENABLE
11	2	RXREFSEL
11	3	DLOOPENB
11	4	LSTUNE0
11	5	LSTUNE1
11	6	LSTUNE2
11	7	LLOOPENB
11	8	TXLINETIM-SEL
11	9	TXPHSADJ1
11	10	TXPHSADJ0
13	1	nc
13	2	nc
13	3	TXFIFO_RES
13	4	RXMUTEM-CLK
13	5	RXMUTEPO-CLK
13	6	TXRATESEL0
13	7	TXRATESEL1
13	8	RXRATESEL0
13	9	RXRATESEL1
13	10	TXREFSEL

SFI/XSBI Interface Voltage References

The SFI/XSBI I/O interface requires a voltage reference for proper operation. This voltage reference is VCCAUX/2 typical. This reference is sourced from a regulator (Appendix A, U8 schematic, Figure 11) or can be trimmed by the user with potentiometers (Appendix A, R146/R148 schematic, Figure 16). J138 is used to select the source of the voltage reference.

SPI4.2/PL-4 Interface Support

Provided for SPI 4.2 interfaces are two active 6x10 backplane connectors. MOLEX-VHDM-74057-002 connectors are used to provide off-board connections to SPI4.2 devices. Connector VHDM1 includes necessary data pairs and control signals for transmit data from a PHY to the LatticeSC, while VHDM2 has been configured for receive data from the PHY to the LatticeSC device.

The SPI4.2 Interface is also visible via high-speed Agilent Logic Analyzer connections (P/N ASP65067-01). The table below references the appropriate signal and connector.

Table 27. SPI4.2 Test Interface (See Appendix A, Figure 20)

SPI4 NET	Logic Analyzer	LA Pin	LA Signal	SPI4 Test Connector	SPI4 Pin	LatticeSC BGA
TDAT_P0	ASP1	8	D0P	VHDM1	A1	J6
TDAT_P14	ASP1	64	D14P	VHDM1	A10	Y5
TDAT_P2	ASP1	16	D2P	VHDM1	A2	K5
TDAT_P4	ASP1	24	D4P	VHDM1	A3	L5
TDAT_P6	ASP1	32	D6P	VHDM1	A4	T3
TDAT_P8	ASP1	40	D8P	VHDM1	A7	U3
TDAT_P10	ASP1	48	D10P	VHDM1	A8	V1
TDAT_P12	ASP1	56	D12P	VHDM1	A9	Y1
TDAT_N0	ASP1	7	D0N	VHDM1	B1	J5
TDAT_N14	ASP1	63	D14N	VHDM1	B10	Y6
TDAT_N2	ASP1	15	D2N	VHDM1	B2	K6
TDAT_N4	ASP1	23	D4N	VHDM1	B3	M5
TDAT_N6	ASP1	31	D6N	VHDM1	B4	R3
TDAT_N8	ASP1	39	D8N	VHDM1	B7	V3
TDAT_N10	ASP1	47	D10N	VHDM1	B8	W1
TDAT_N12	ASP1	55	D12N	VHDM1	B9	AA1
TCTL_P	ASP3	56	D12P	VHDM1	C10	AC3
TSCLK_P	ASP3	80	D16P/CLKP	VHDM1	C5	AF2
TSTAT0_P	ASP3	28	D5P	VHDM1	C6	AC4
TCTL_N	ASP3	55	D12N	VHDM1	D10	AD3
TSTAT1_P	ASP3	36	D7P	VHDM1	D6	AF1
TDAT_P1	ASP1	12	D1P	VHDM1	E1	K4
TDAT_P15	ASP1	68	D15P	VHDM1	E10	AD2
TDAT_P3	ASP1	20	D3P	VHDM1	E2	E1
TDAT_P5	ASP1	28	D5P	VHDM1	E3	R7
TDAT_P7	ASP1	36	D7P	VHDM1	E4	R5
TDCLK_P	ASP1	80	D16P/CLKP	VHDM1	E5	P8
TDAT_P9	ASP1	44	D9P	VHDM1	E7	T5
TDAT_P11	ASP1	52	D11P	VHDM1	E8	V5
TDAT_P13	ASP1	60	D13P	VHDM1	E9	Y3
TDAT_N1	ASP1	11	D1N	VHDM1	F1	J4
TDAT_N15	ASP1	67	D15N	VHDM1	F10	AE2
TDAT_N3	ASP1	19	D3N	VHDM1	F2	D1
TDAT_N5	ASP1	27	D5N	VHDM1	F3	R6
TDAT_N7	ASP1	35	D7N	VHDM1	F4	R4

Table 27. SPI4.2 Test Interface (See Appendix A, Figure 20) (Continued)

SPI4 NET	Logic Analyzer	LA Pin	LA Signal	SPI4 Test Connector	SPI4 Pin	LatticeSC BGA
TDCLK_N	ASP1	79	D16N/CLKN	VHDM1	F5	R8
TDAT_N9	ASP1	43	D9N	VHDM1	F7	T4
TDAT_N11	ASP1	51	D11N	VHDM1	F8	V4
TDAT_N13	ASP1	59	D13N	VHDM1	F9	W3
RDAT_P14	ASP2	64	D14P	VHDM2	A1	V2
RDAT_P0	ASP2	8	D0P	VHDM2	A10	D3
RDAT_P12	ASP2	56	D12P	VHDM2	A2	T1
RDAT_P10	ASP2	48	D10P	VHDM2	A3	P1
RDAT_P8	ASP2	40	D8P	VHDM2	A4	N3
RDAT_P6	ASP2	32	D6P	VHDM2	A7	J1
RDAT_P4	ASP2	24	D4P	VHDM2	A8	K3
RDAT_P2	ASP2	16	D2P	VHDM2	A9	F3
RDAT_N14	ASP2	63	D14N	VHDM2	B1	W2
RDAT_N0	ASP2	7	D0N	VHDM2	B10	D2
RDAT_N12	ASP2	55	D12N	VHDM2	B2	U1
RDAT_N10	ASP2	47	D10N	VHDM2	B3	R1
RDAT_N8	ASP2	39	D8N	VHDM2	B4	P3
RDAT_N6	ASP2	31	D6N	VHDM2	B7	K1
RDAT_N4	ASP2	23	D4N	VHDM2	B8	L3
RDAT_N2	ASP2	15	D2N	VHDM2	B9	G3
RCTL_P	ASP3	48	D10P	VHDM2	C1	AB1
RSTAT0_P	ASP3	12	D1P	VHDM2	C5	AB6
RSCLK_P	ASP3	68	D15P	VHDM2	C6	AC6
RCTL_N	ASP3	47	D10N	VHDM2	D1	AC1
RSTAT1_P	ASP3	16	D2P	VHDM2	D5	AE3
RDAT_P15	ASP2	68	D15P	VHDM2	E1	Y2
RDAT_P1	ASP2	12	D1P	VHDM2	E10	E3
RDAT_P13	ASP2	60	D13P	VHDM2	E2	U4
RDAT_P11	ASP2	52	D11P	VHDM2	E3	T2
RDAT_P9	ASP2	44	D9P	VHDM2	E4	P2
RDCLK_P	ASP2	80	D16P/CLKP	VHDM2	E6	L1
RDAT_P7	ASP2	36	D7P	VHDM2	E7	N2
RDAT_P5	ASP2	28	D5P	VHDM2	E8	F2
RDAT_P3	ASP2	20	D3P	VHDM2	E9	G2
RDAT_N15	ASP2	67	D15N	VHDM2	F1	AA2
RDAT_N1	ASP2	11	D1N	VHDM2	F10	E2
RDAT_N13	ASP2	59	D13N	VHDM2	F2	U5
RDAT_N11	ASP2	51	D11N	VHDM2	F3	U2
RDAT_N9	ASP2	43	D9N	VHDM2	F4	R2
RDCLK_N	ASP2	79	D16N/CLKN	VHDM2	F6	M1
RDAT_N7	ASP2	35	D7N	VHDM2	F7	N1
RDAT_N5	ASP2	27	D5N	VHDM2	F8	F1
RDAT_N3	ASP2	19	D3N	VHDM2	F9	G1

SPI4.2 Interface Voltage References

The SPI4.2 I/O interface requires a voltage reference for proper operation. This voltage reference is VCCAUX/2 typical. This reference is sourced from a regulator (Appendix A, U9 schematic, Figure 11) or can be trimmed by the user with potentiometers (Appendix A, R196/R201 schematic, Figure 20). J149 is used to select the source of the voltage reference.

DDR2 Interface Support

The LatticeSC Evaluation Board is equipped to be interconnected to DDR2 SDRAM memory modules. The DDR2 memory interface includes a 64-bit wide DIMM connection to one 200-pin DDR2 SODIMM socket. The evaluation board includes termination of address, command, and control lines to the DIMM.

For the SODIMM data-path, the data bytes are spread across multiple banks of the FPGA device. The board includes all power and external components needed to demonstrate the memory controller of the LatticeSC device

Table 28. DDR2 Memory SODIMM Module Interface (See Appendix A, Figure 18)

DDR2 Net	900-fpBGA Ball	5S25 Site	SODIMM Pin	SODIMM Signal
MEMINTF_A0	AG3	PB4A	102	A0
MEMINTF_A1	AH2	PB4B	101	A1
MEMINTF_A2	AD6	PB4C	100	A2
MEMINTF_A3	AJ2	PB5A	99	A3
MEMINTF_A4	AK2	PB5B	98	A4
MEMINTF_A5	AD7	PB5C	97	A5
MEMINTF_A6	AD8	PB5D	94	A6
MEMINTF_A7	AF7	PB7A	92	A7
MEMINTF_A8	AF6	PB7B	93	A8
MEMINTF_A9	AH4	PB8A	91	A9
MEMINTF_BA0	AF9	PB11C	107	BA0
MEMINTF_BA1	AE10	PB11D	106	BA1
MEMINTF_DM0	AK3	PB12A	10	DM0
MEMINTF_DM1	AK5	PB16B	26	DM1
MEMINTF_DM2	AJ12	PB23B	52	DM2
MEMINTF_DM3	AH12	PB31A	67	DM3
MEMINTF_DM4	AK16	PB37A	130	DM4
MEMINTF_DM5	AK19	PB41B	147	DM5
MEMINTF_DM6	AJ21	PB49B	170	DM6
MEMINTF_DM7	AG21	PB55A	185	DM7
MEMINTF_DQ0	AJ4	PB12B	5	DQ0
MEMINTF_DQ1	AE11	PB13A	7	DQ1
MEMINTF_DQ2	AF10	PB13B	17	DQ2
MEMINTF_DQ3	AH7	PB15A	19	DQ3
MEMINTF_DQ4	AH8	PB15B	4	DQ4
MEMINTF_DQ5	AE12	PB15C	6	DQ5
MEMINTF_DQ6	AE13	PB15D	14	DQ6
MEMINTF_DQ7	AK4	PB16A	16	DQ7
MEMINTF_DQ8	AJ5	PB17A	23	DQ8
MEMINTF_DQ9	AJ6	PB17B	25	DQ9
MEMINTF_DQ10	AJ7	PB19A	35	DQ10
MEMINTF_DQ11	AJ8	PB19B	37	DQ11

Table 28. DDR2 Memory SODIMM Module Interface (See Appendix A, Figure 18) (Continued)

DDR2 Net	900-fpBGA Ball	5S25 Site	SODIMM Pin	SODIMM Signal
MEMINTF_DQ12	AH11	PB20B	20	DQ12
MEMINTF_DQ13	AE14	PB20D	22	DQ13
MEMINTF_DQ14	AF14	PB21C	36	DQ14
MEMINTF_DQ15	AF15	PB21D	38	DQ15
MEMINTF_DQ16	AG13	PB23C	43	DQ16
MEMINTF_DQ17	AK9	PB24B	45	DQ17
MEMINTF_DQ18	AH14	PB25A	55	DQ18
MEMINTF_DQ19	AG14	PB25B	57	DQ19
MEMINTF_DQ20	AK10	PB28A	44	DQ20
MEMINTF_DQ21	AK11	PB28B	46	DQ21
MEMINTF_DQ22	AH15	PB29A	56	DQ22
MEMINTF_DQ23	AG15	PB29B	58	DQ23
MEMINTF_DQ24	AJ13	PB31B	61	DQ24
MEMINTF_DQ25	AD15	PB31C	63	DQ25
MEMINTF_DQ26	AE15	PB31D	73	DQ26
MEMINTF_DQ27	AK12	PB32A	75	DQ27
MEMINTF_DQ28	AK13	PB32B	62	DQ28
MEMINTF_DQ29	AJ14	PB33A	64	DQ29
MEMINTF_DQ30	AJ15	PB33B	74	DQ30
MEMINTF_DQ31	AK14	PB35A	76	DQ31
MEMINTF_DQ32	AK17	PB37B	123	DQ32
MEMINTF_DQ33	AJ16	PB38A	125	DQ33
MEMINTF_DQ34	AJ17	PB38B	135	DQ34
MEMINTF_DQ35	AE16	PB38C	137	DQ35
MEMINTF_DQ36	AH16	PB39A	124	DQ36
MEMINTF_DQ37	AG16	PB39B	126	DQ37
MEMINTF_DQ38	AF16	PB38D	134	DQ38
MEMINTF_DQ39	AK18	PB41A	136	DQ39
MEMINTF_DQ40	AH17	PB42A	141	DQ40
MEMINTF_DQ41	AH18	PB42B	143	DQ41
MEMINTF_DQ42	AF17	PB42C	151	DQ42
MEMINTF_DQ43	AG17	PB42D	153	DQ43
MEMINTF_DQ44	AJ18	PB43A	140	DQ44
MEMINTF_DQ45	AJ19	PB43B	142	DQ45
MEMINTF_DQ46	AK21	PB46B	152	DQ46
MEMINTF_DQ47	AG18	PB47B	154	DQ47
MEMINTF_DQ48	AF19	PB49D	157	DQ48
MEMINTF_DQ49	AK23	PB51B	159	DQ49
MEMINTF_DQ50	AH19	PB51C	173	DQ50
MEMINTF_DQ51	AH20	PB51D	175	DQ51
MEMINTF_DQ52	AE19	PB52C	158	DQ52
MEMINTF_DQ53	AE20	PB52D	160	DQ53
MEMINTF_DQ54	AE21	PB53A	174	DQ54
MEMINTF_DQ55	AF21	PB53B	176	DQ55
MEMINTF_DQ56	AG22	PB55B	179	DQ56

Table 28. DDR2 Memory SODIMM Module Interface (See Appendix A, Figure 18) (Continued)

DDR2 Net	900-fpBGA Ball	5S25 Site	SODIMM Pin	SODIMM Signal
MEMINTF_DQ57	AH22	PB56A	181	DQ57
MEMINTF_DQ58	AH23	PB56B	189	DQ58
MEMINTF_DQ59	AH21	PB56C	191	DQ59
MEMINTF_DQ60	AD23	PB57A	180	DQ60
MEMINTF_DQ61	AE23	PB57B	182	DQ61
MEMINTF_DQ62	AH24	PB59A	192	DQ62
MEMINTF_DQ63	AH25	PB59B	194	DQ63
MEMINTF_DQS0	AH10	PB20A	13	DQS0
MEMINTF_DQS1	AF13	PB20C	31	DQS1
MEMINTF_DQS2	AJ11	PB23A	51	DQS2
MEMINTF_DQS3	AK8	PB24A	70	DQS3
MEMINTF_DQS4	AK20	PB46A	131	DQS4
MEMINTF_DQS5	AF18	PB47A	148	DQS5
MEMINTF_DQS6	AJ20	PB49A	169	DQS6
MEMINTF_DQS7	AK22	PB51A	188	DQS7
MEMINTF_K	AK24	PB52A	30	CK0
MEMINTF_K#	AK25	PB52B	32	CK0#
MEMINTF_K#_COPY	AF27	PB65B	164	CK1
MEMINTF_K_COPY	AG26	PB65A	166	CK1#
MEMINTF_RAS#	AJ1	PB3B	108	RAS#
MEMINTF_WE#	AE5	PB3D	109	WE#

SSTL Memory Interface Voltage References

The SSTL I/O interface requires a voltage reference for proper operation. This voltage reference is VCCIO18/2 typical. This reference is sourced from a regulator (Appendix A, U12 schematic, Figure 11) or can be trimmed by the user with potentiometers (Appendix A, R185/184 schematic, Figure 17). J147 is used to select the source of the voltage reference.

Memory Interface Voltage Terminations

The DDR2 interface needs termination of the memory module. This is accomplished using the VTT regulator (Appendix A, U23 schematic, Figure 19). The VTT is used by the resistor terminations provided on the board. This regulator also provides a dedicated voltage reference to the SODIMM.

The LatticeSC also has an optional termination that can be supplied to the device. This termination voltage is generated on board by (Appendix A, U12 Figure 11) and must be selected by the user's design. This VTT source also needs to be chosen on the board with the adjacent J59.

Technical Support Assistance

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+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
March 2006	01.0	Initial release.
July 2006	01.2	Updated FPGA Test Selector Header table and FPGA I/O Test SMA Connectors table.
April 2007	01.3	Added important information for proper connection of ispDOWNLOAD (Programming) Cables.

Appendix A. PCB Schematics

Figure 4. Block Diagram

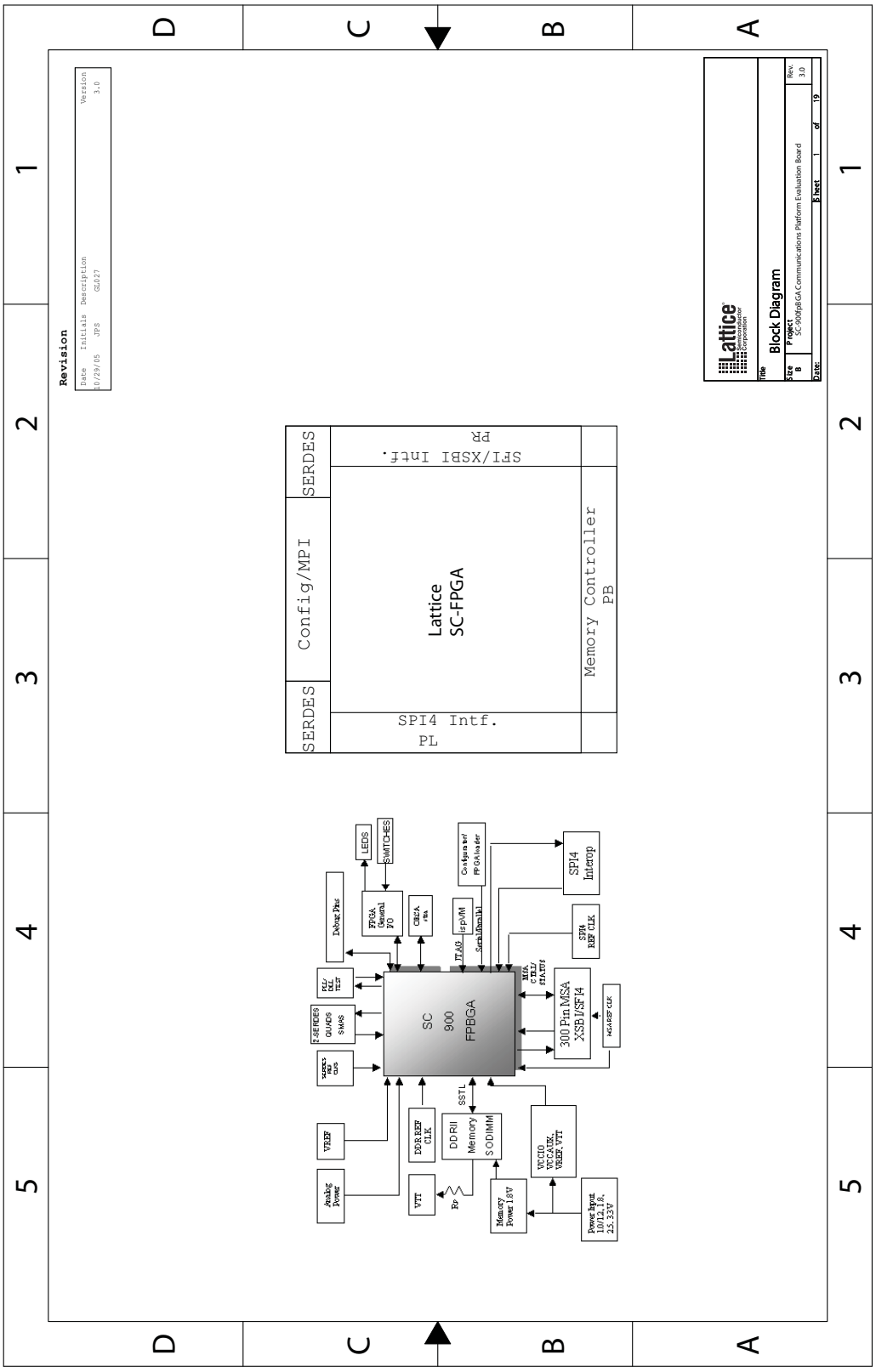

Figure 5. Power Input

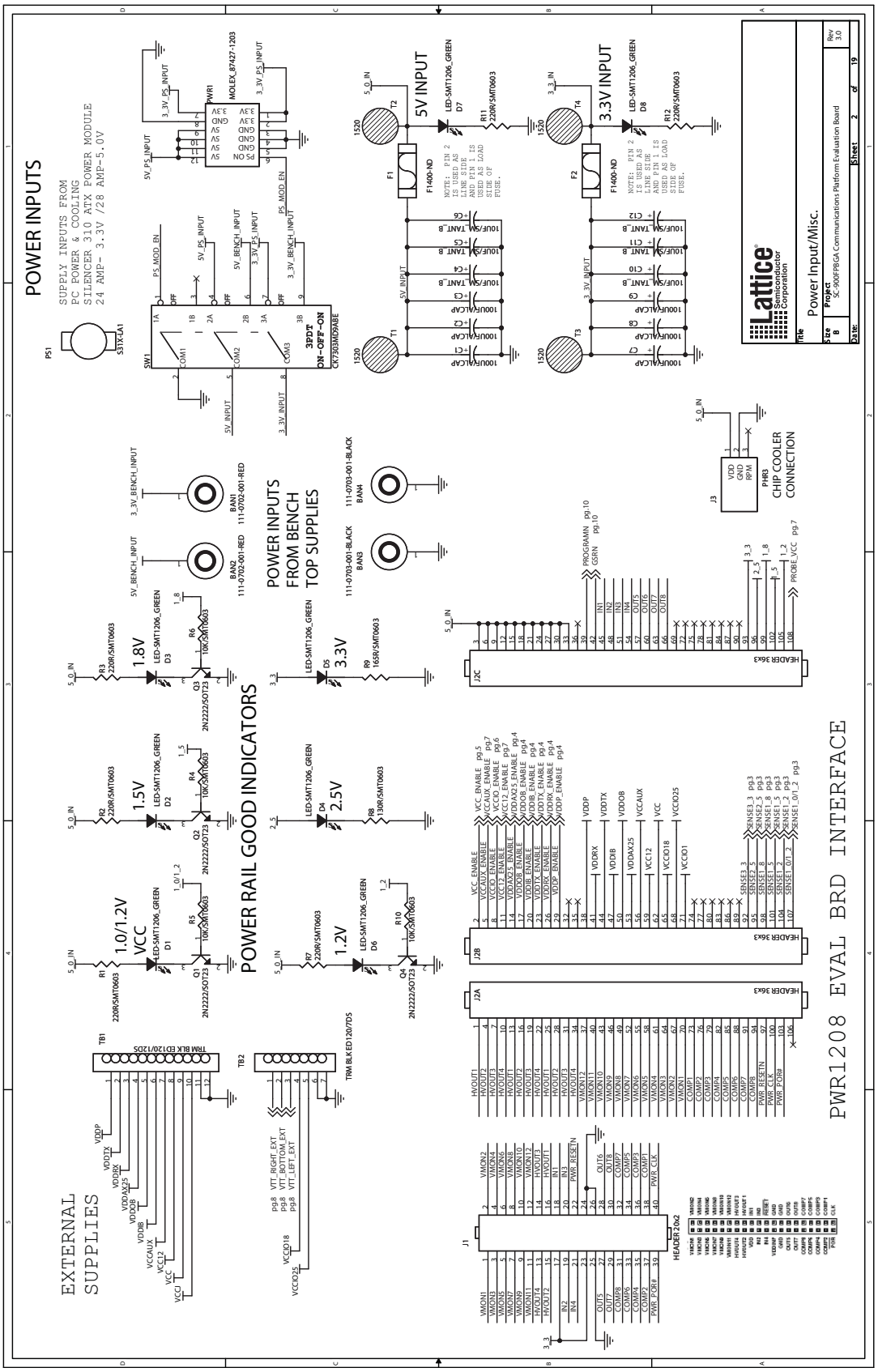

Figure 6. Power Regulation

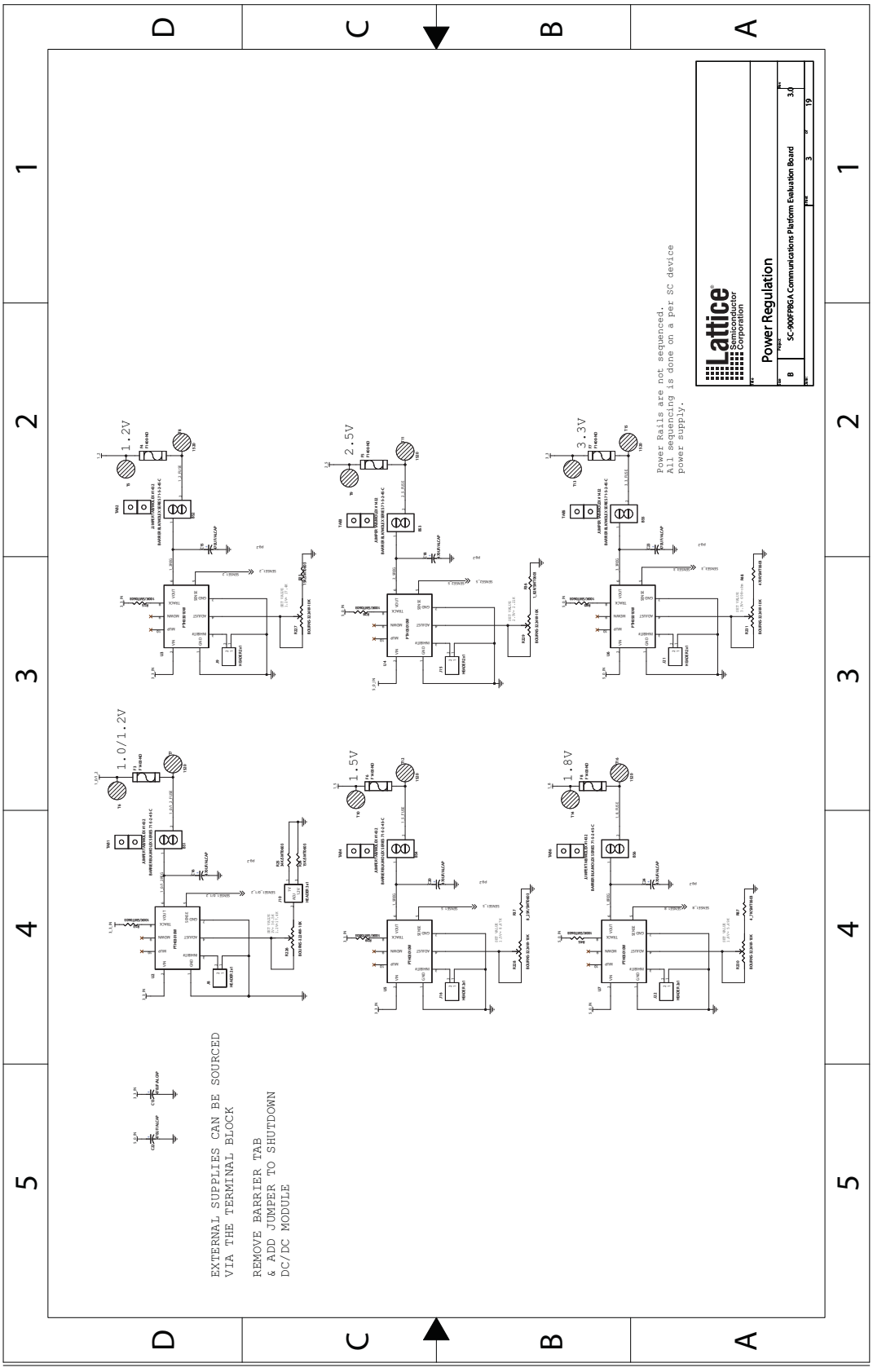

Figure 7. SERDES Supplies

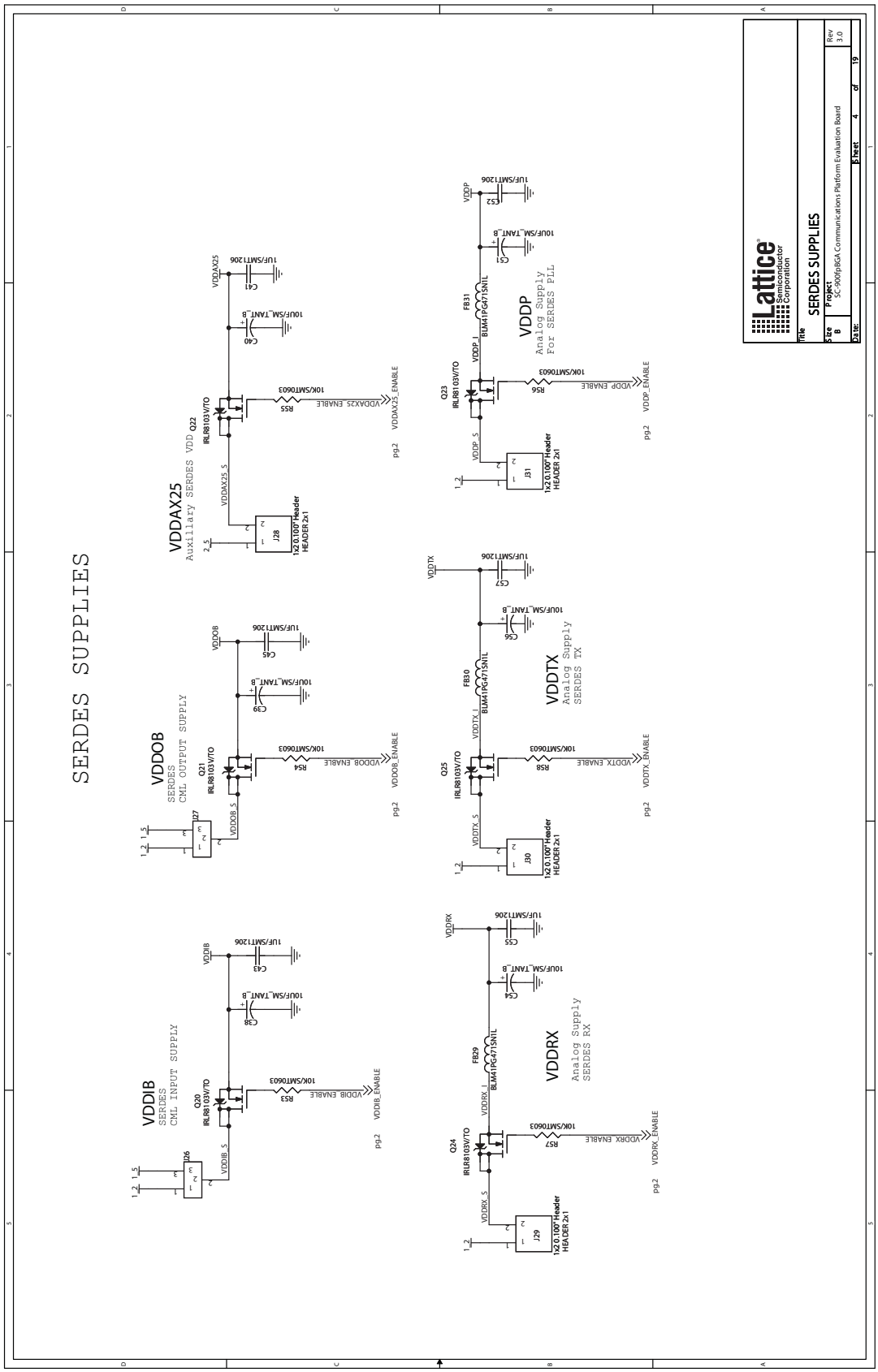

Figure 8. Power/Bypass

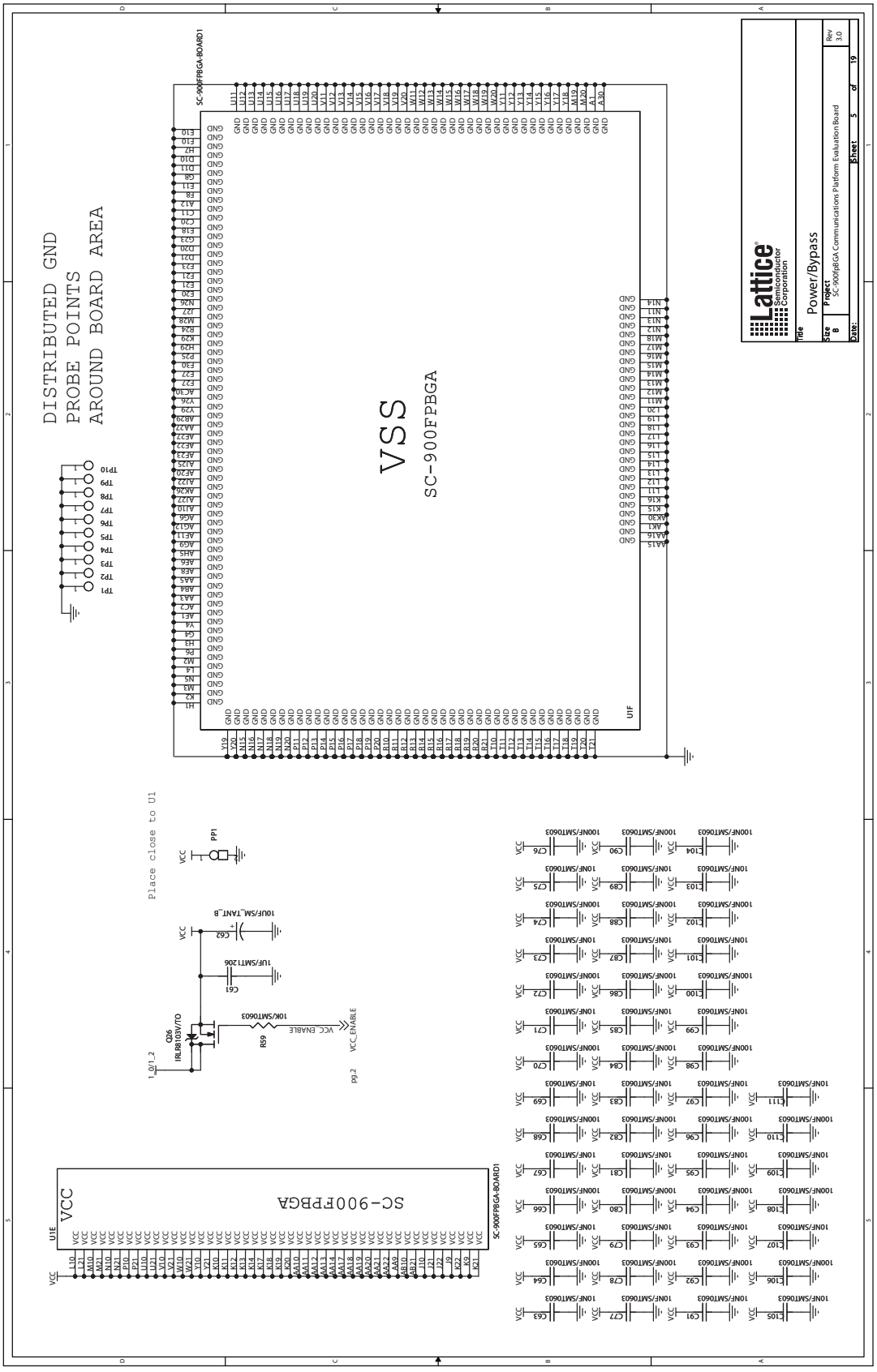

Figure 9. VCCIO

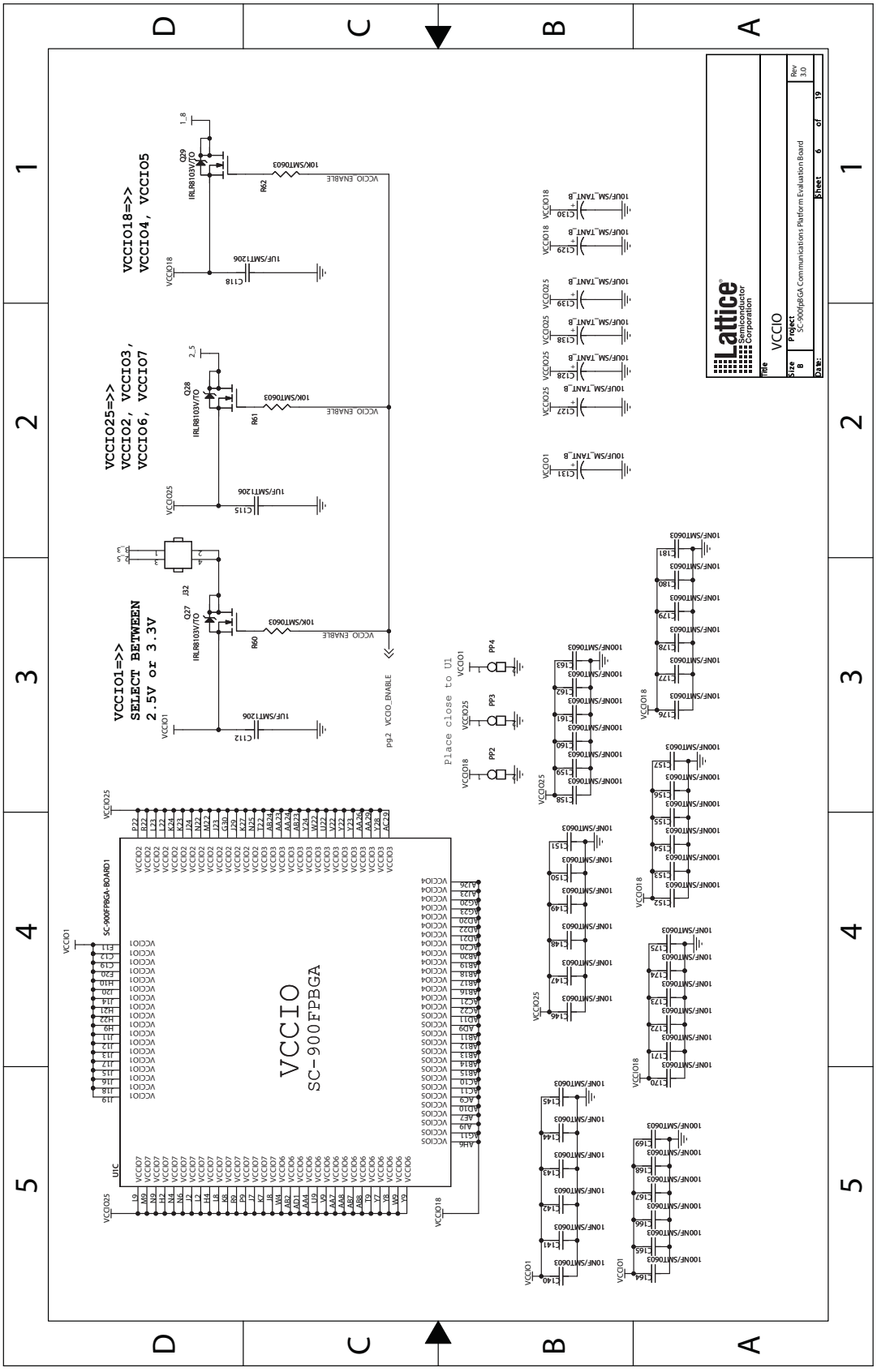

Figure 10. VCCIP2

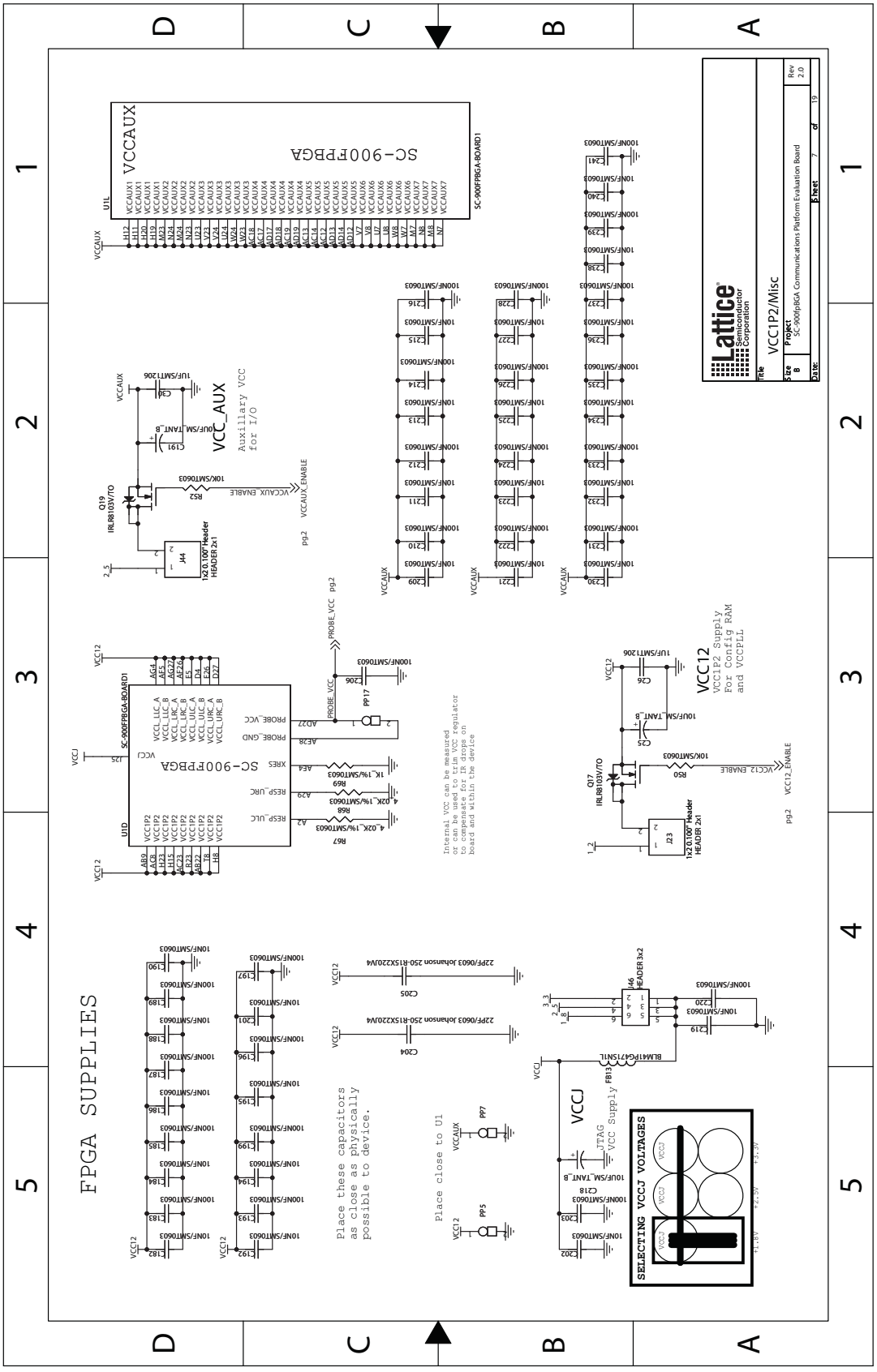

Figure 11. VTT

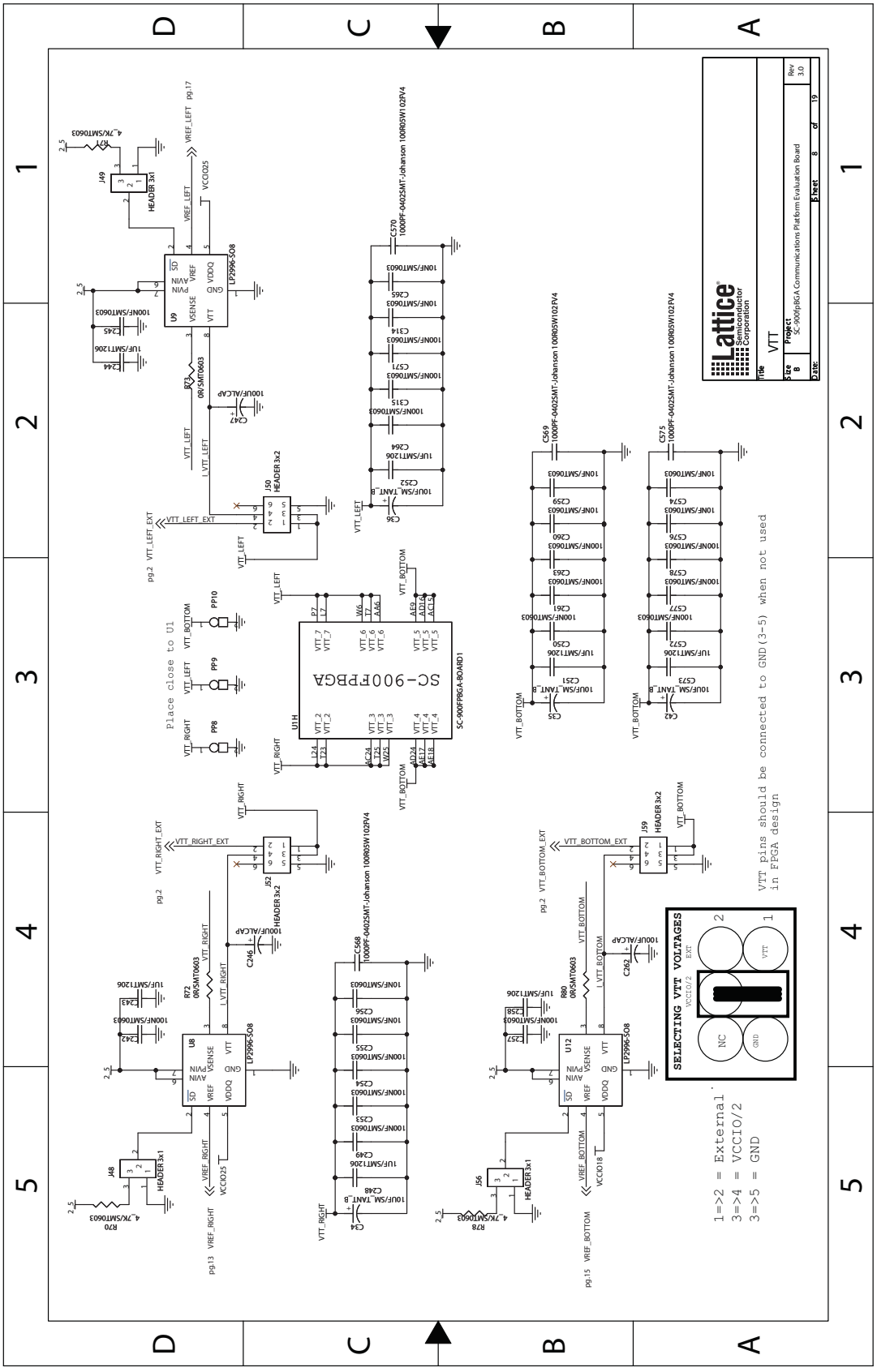

Figure 12. SERDES Analog Supplies

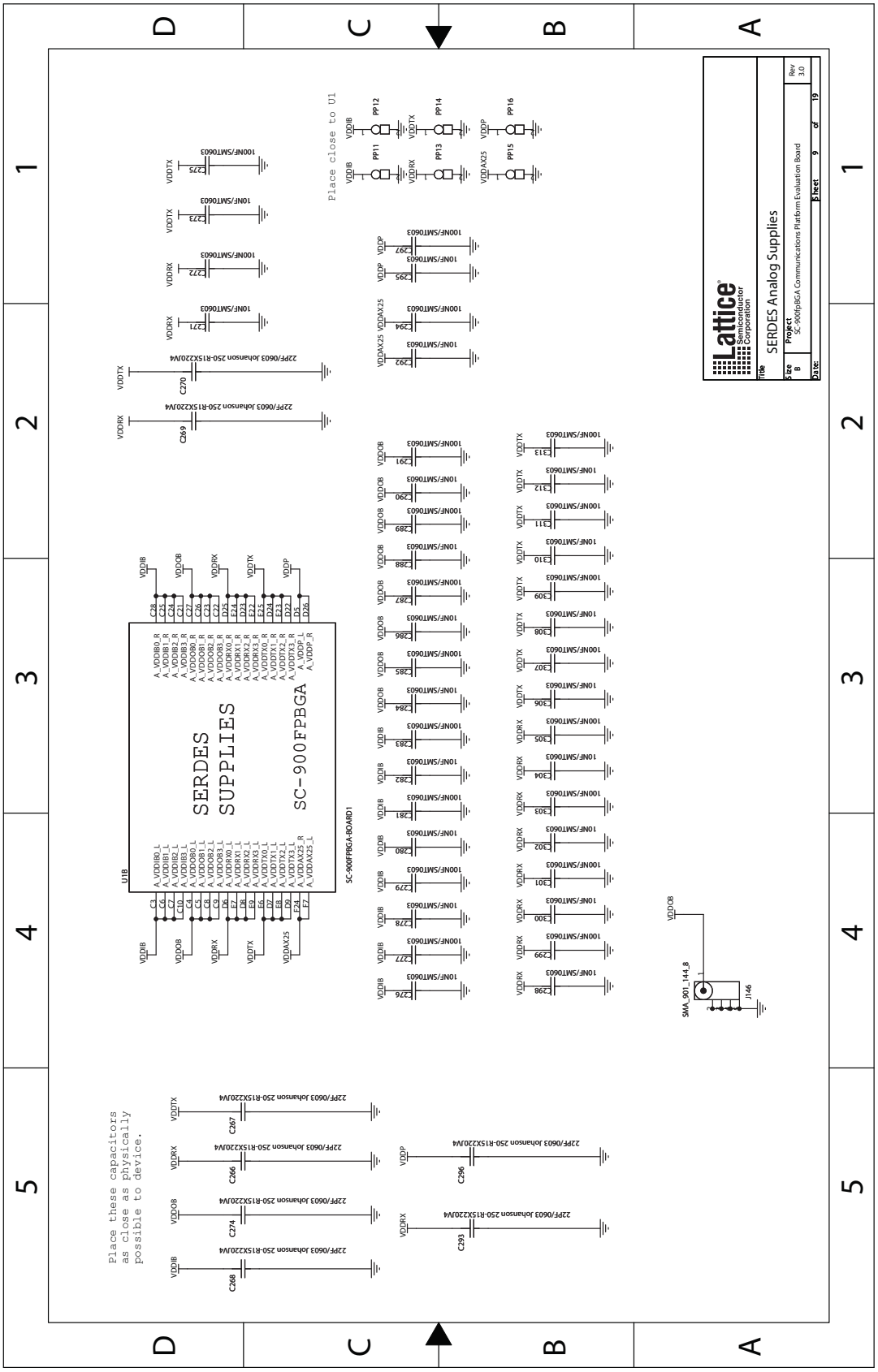

Figure 13. Configuration/JTAG

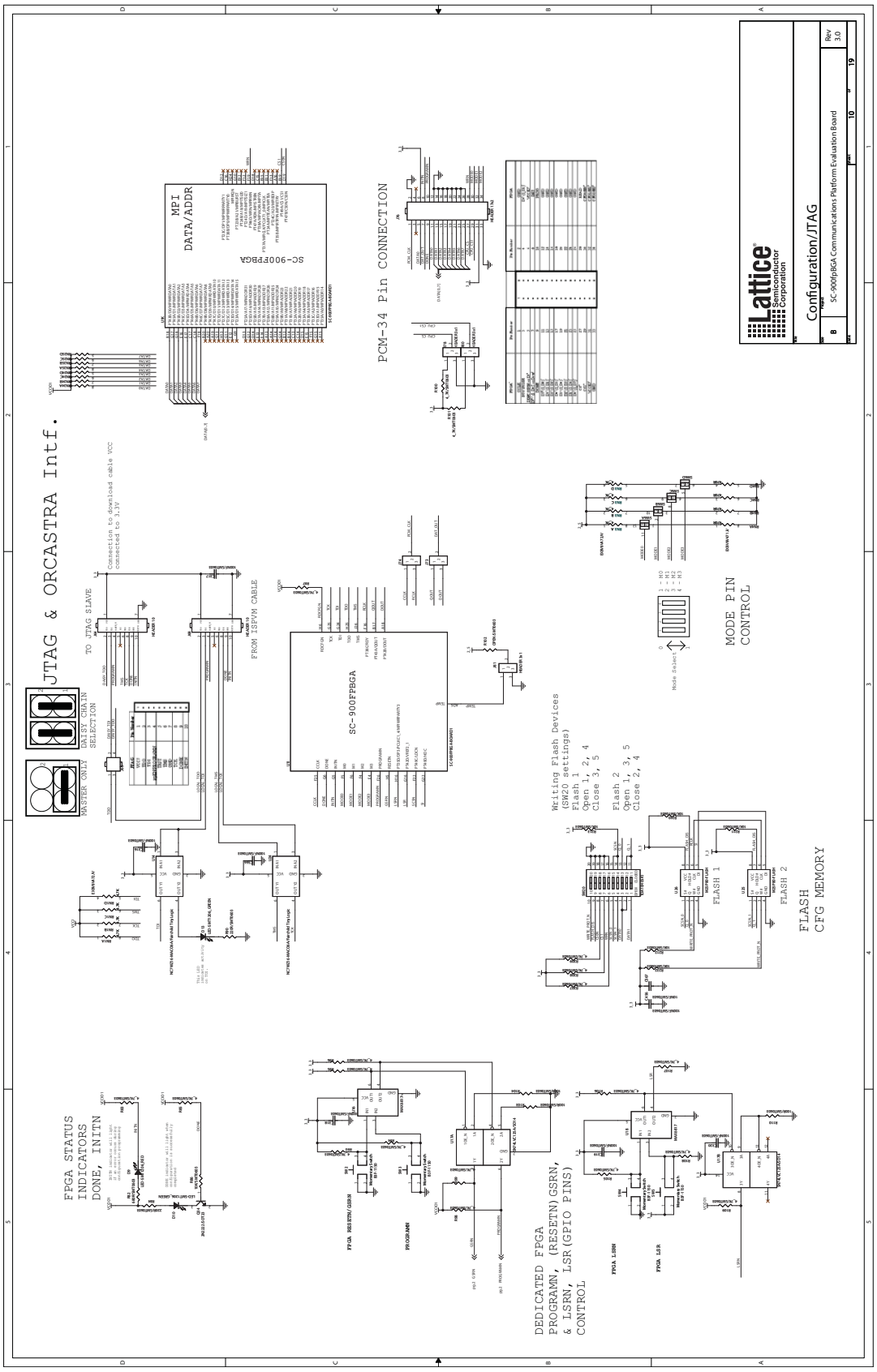

Figure 14. Clock Sources

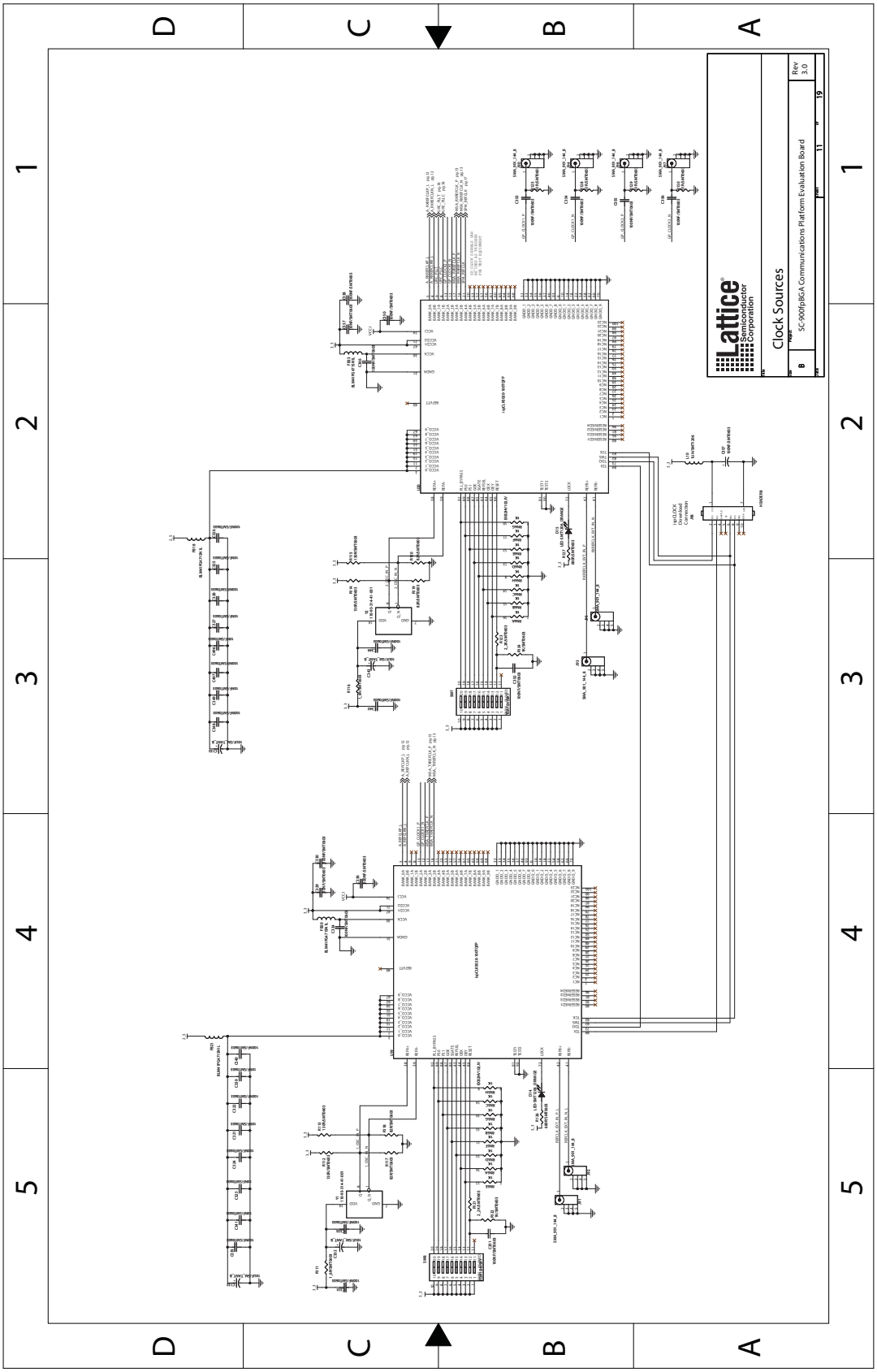

Figure 15. SERDES

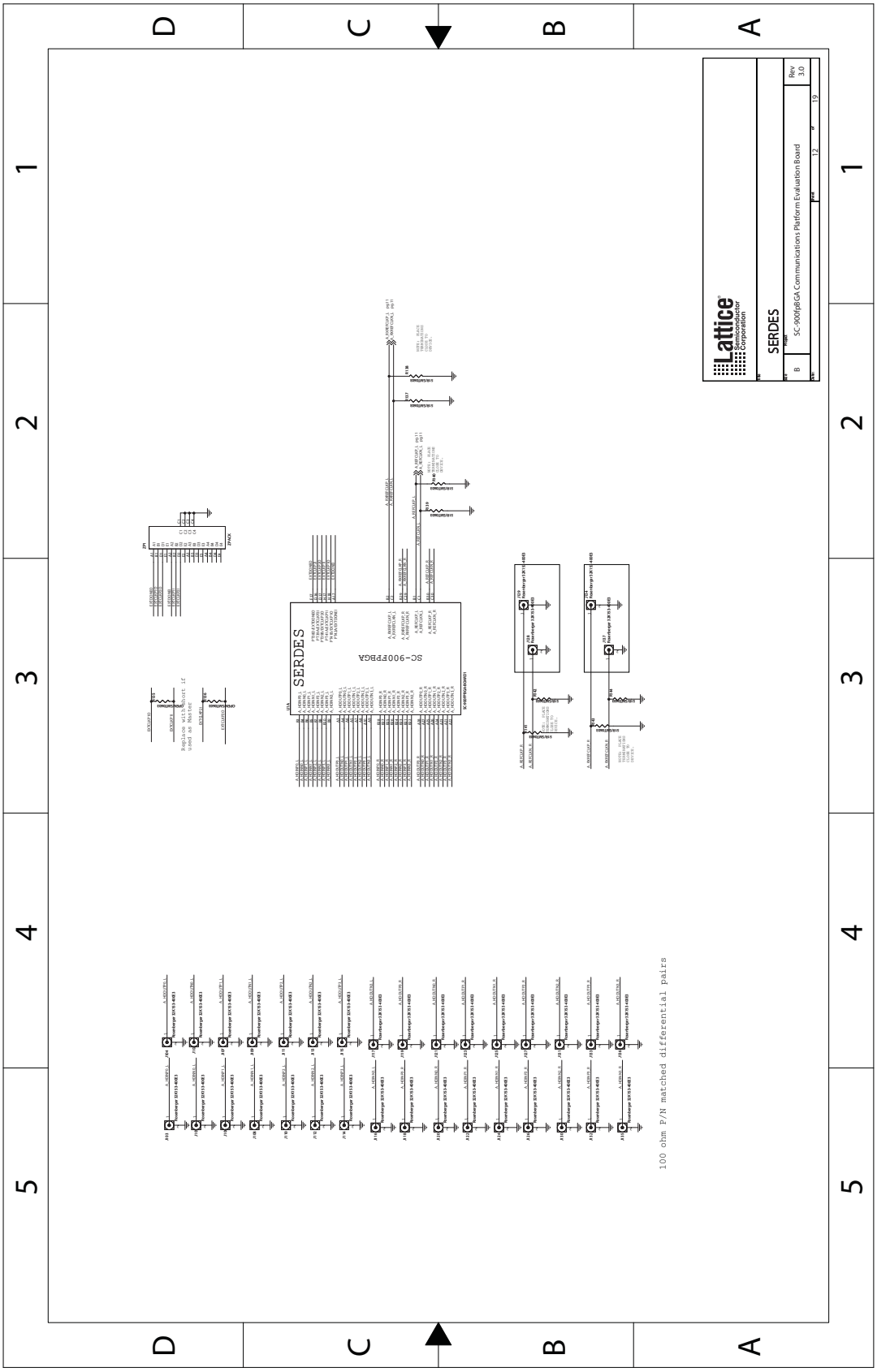

Figure 16. Transponder Interface

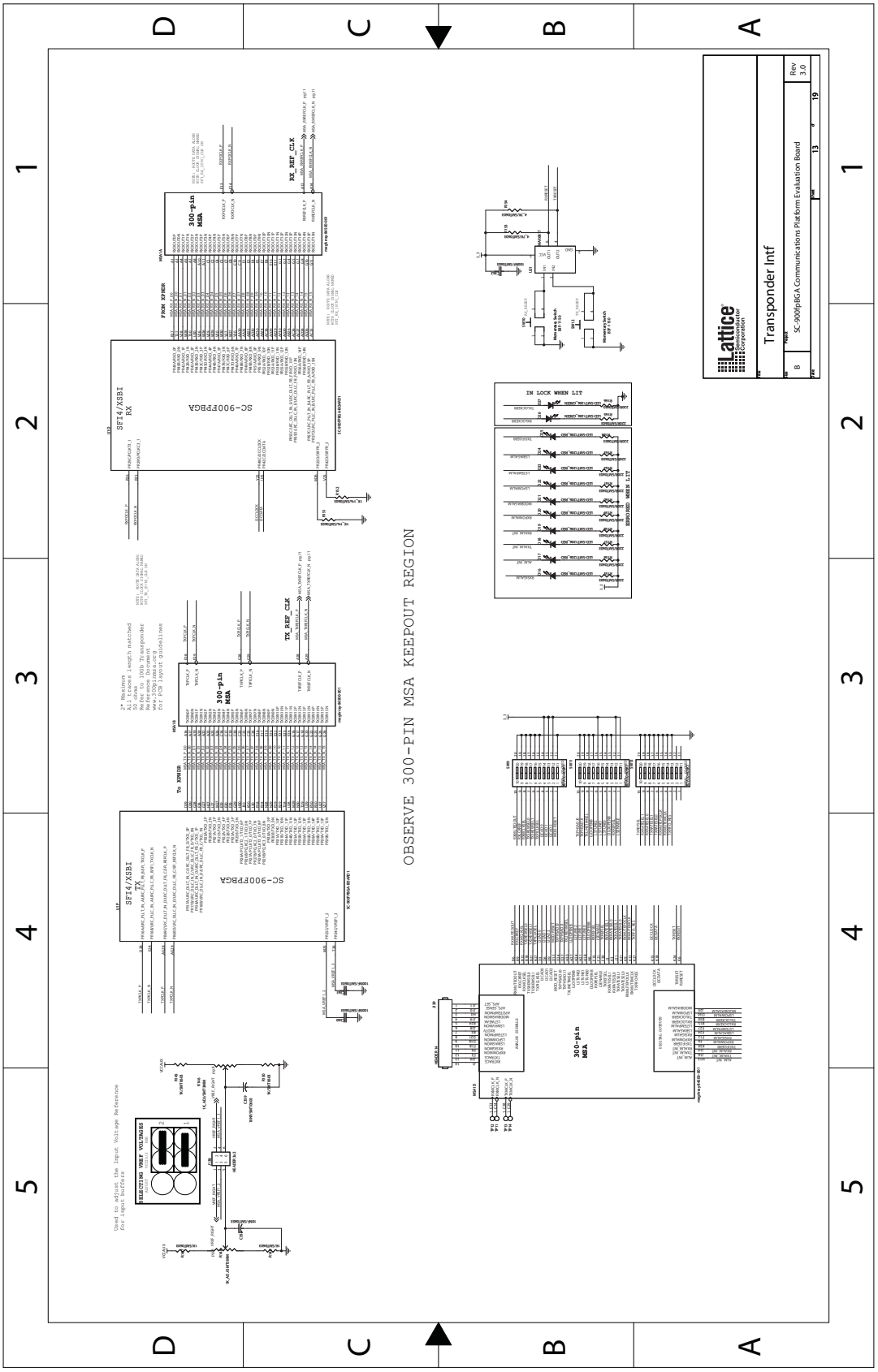

Figure 17. 300-Pin MSA Power

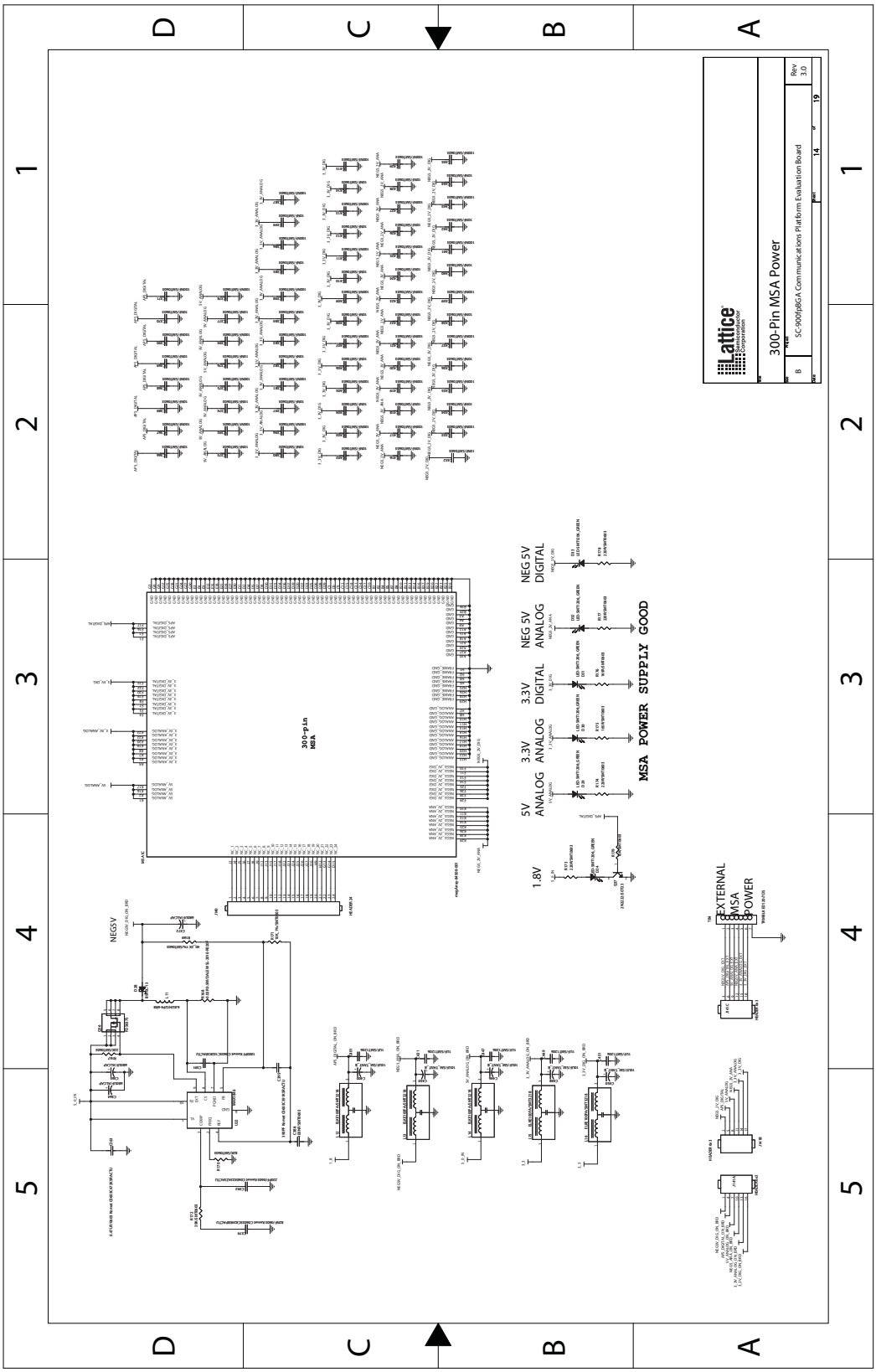

Figure 18. DDR2 Memory Controller/SODIMM

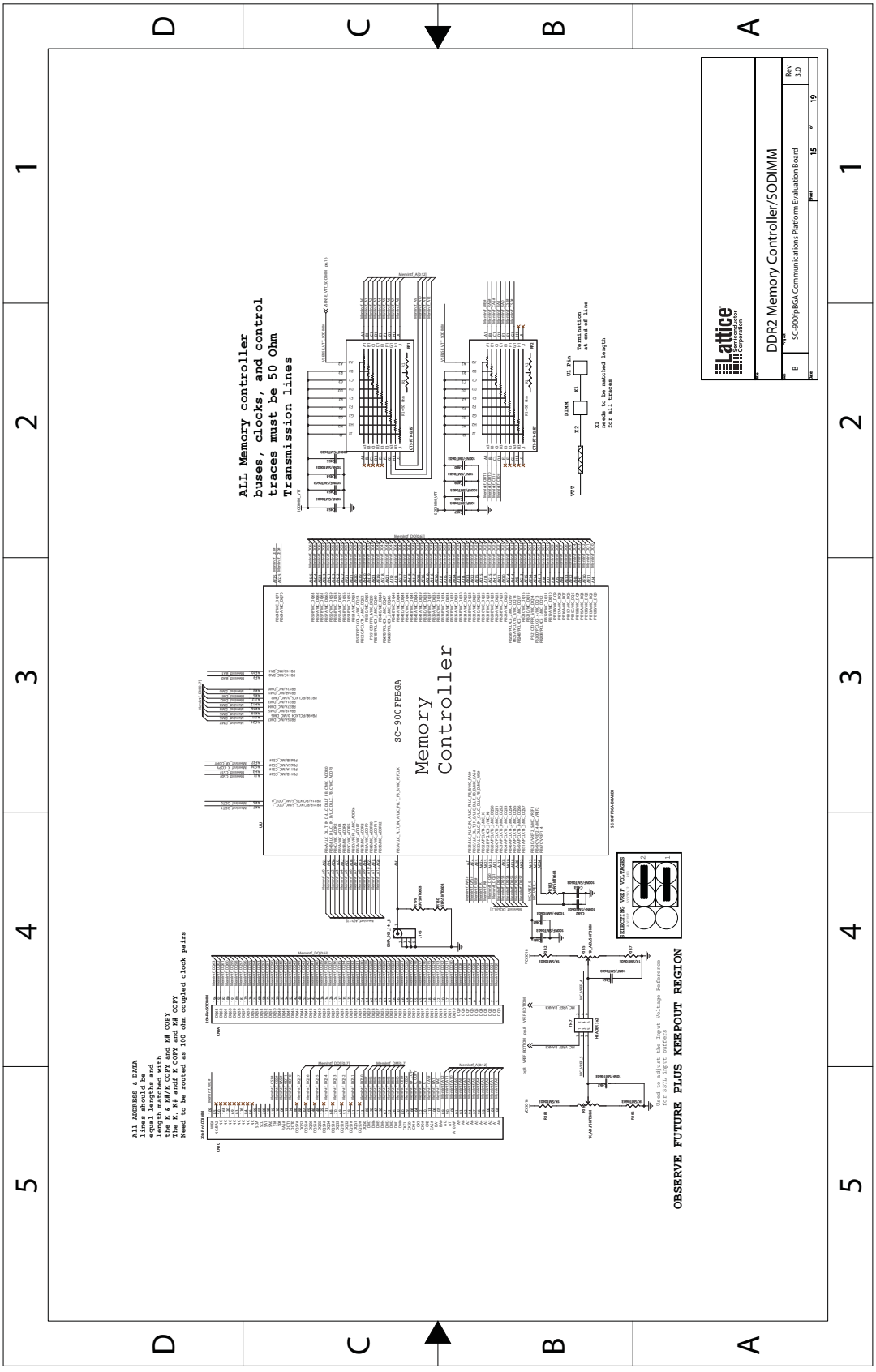

Figure 19. SODIMM Power/VTT

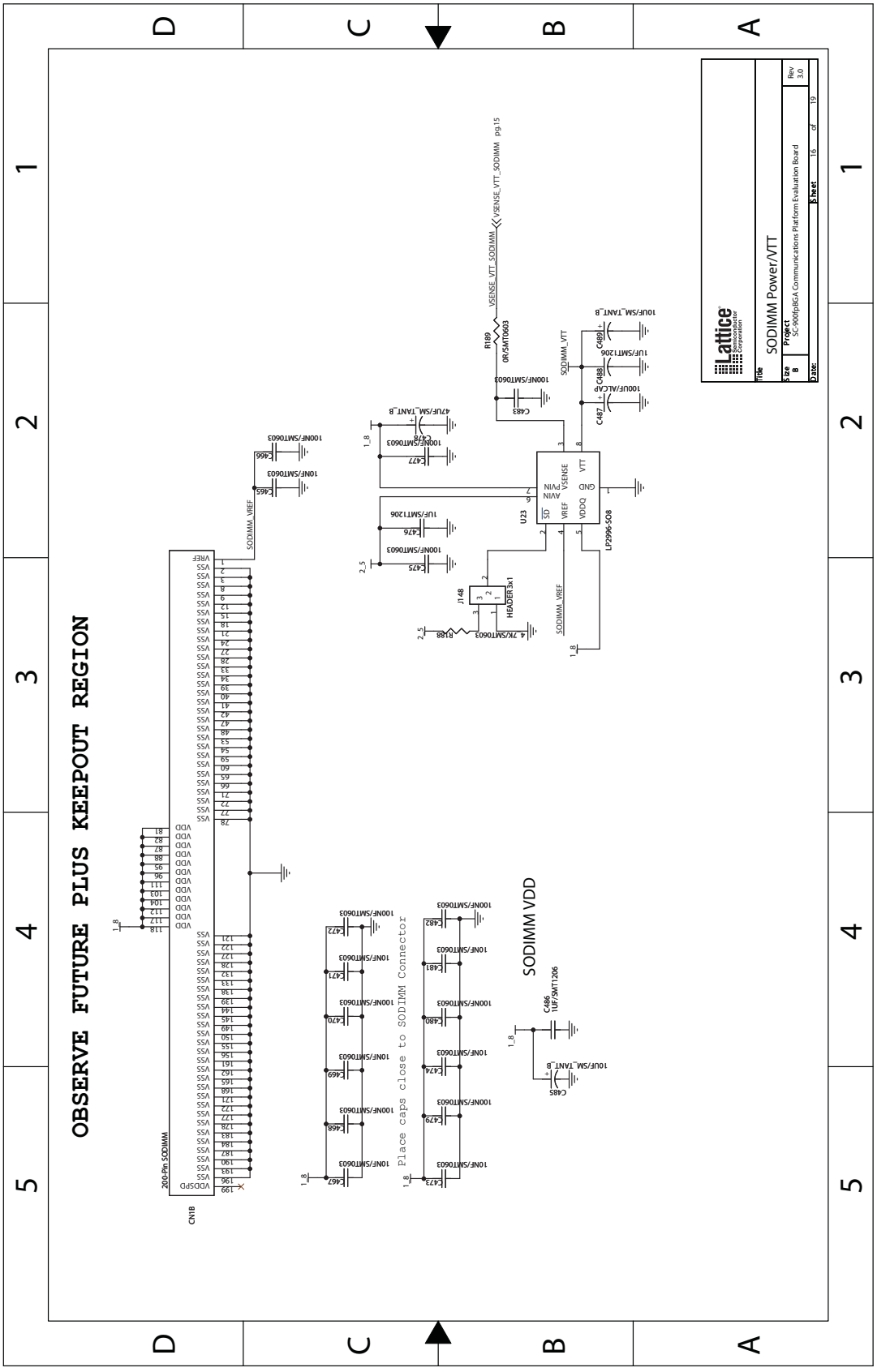

Figure 20. SPI4 Interface

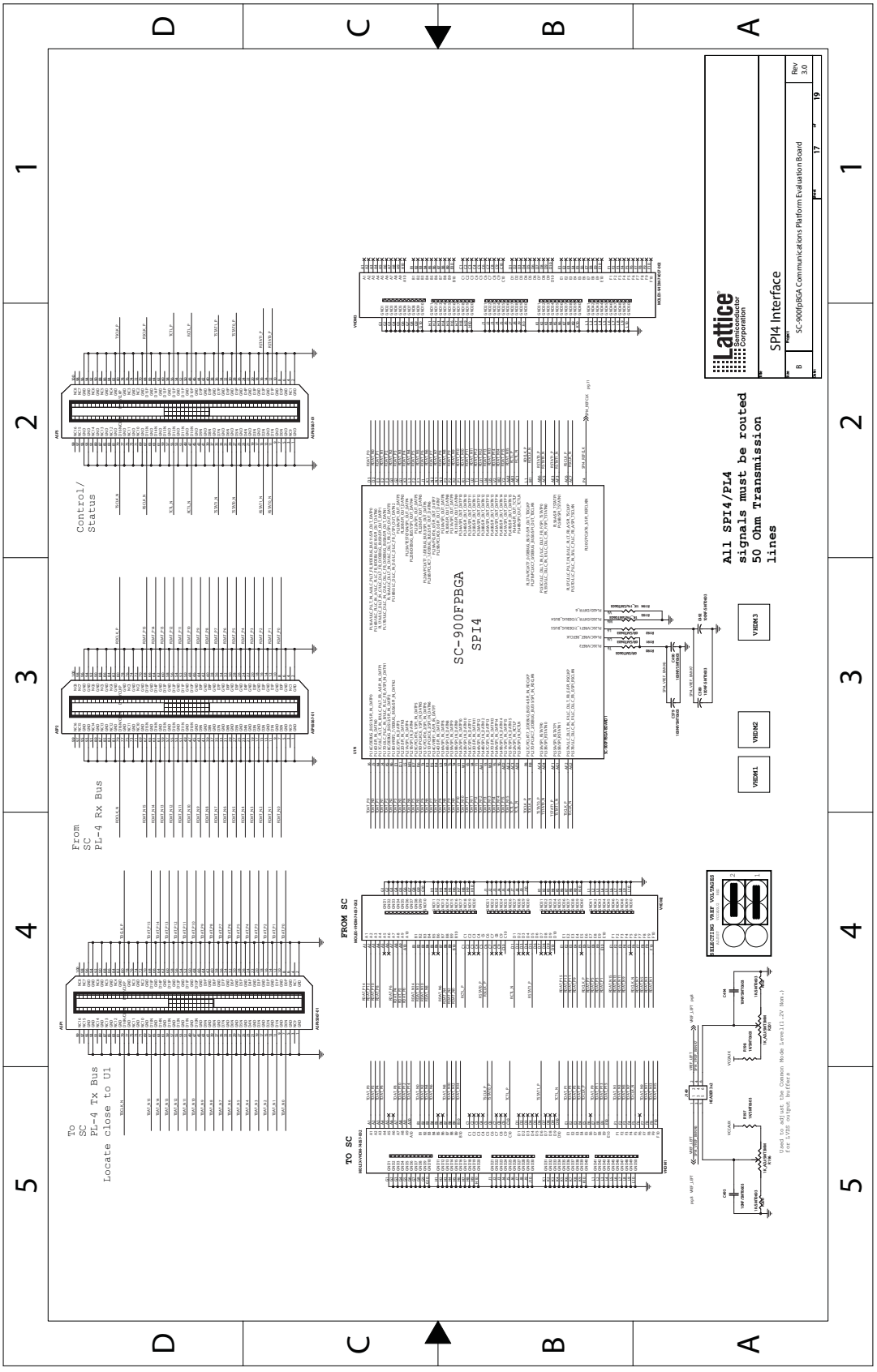

Figure 21. FPGA Test

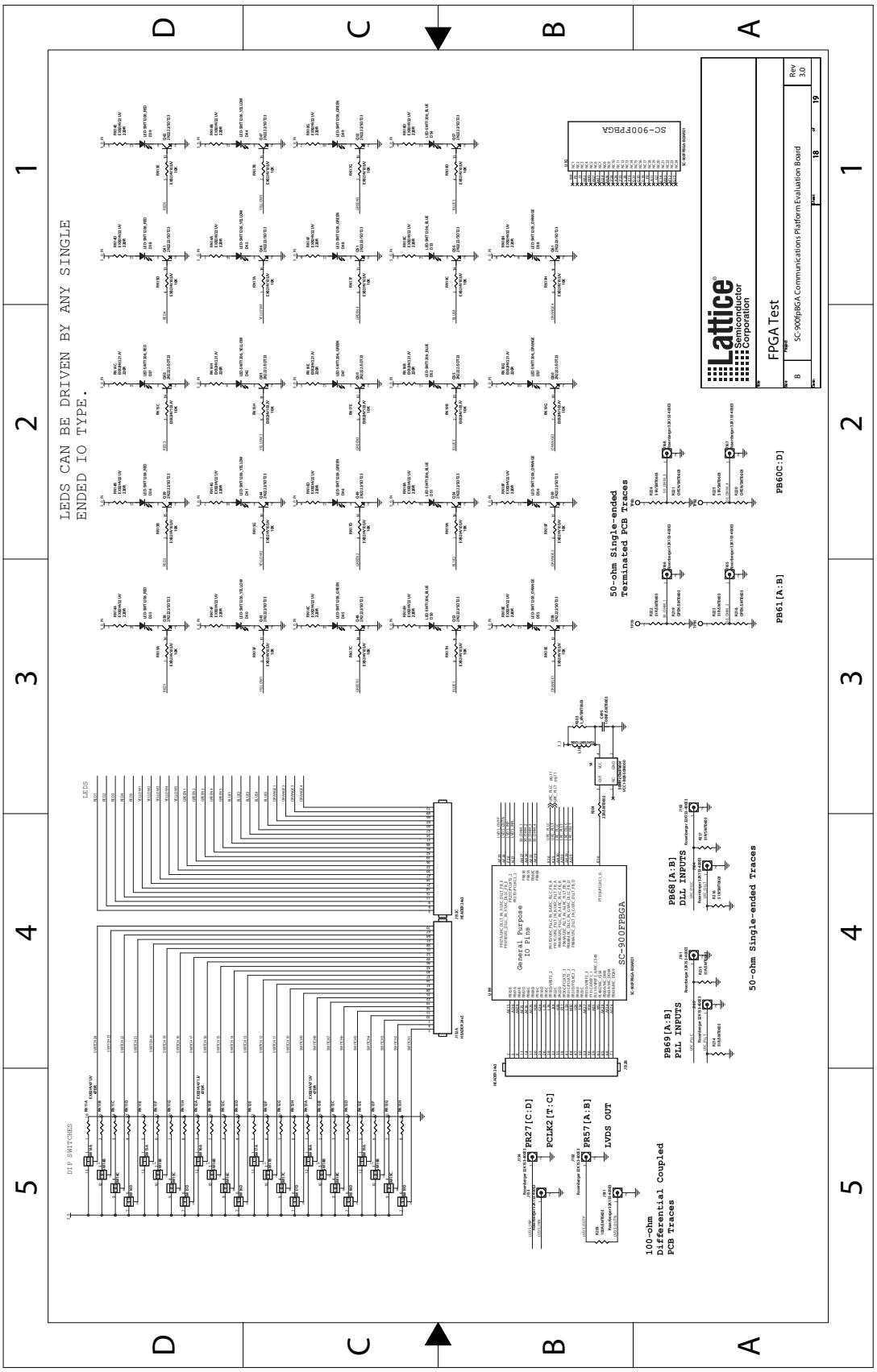

Figure 22. BGA Decoupling