Electrical Recommendations for Lattice SERDES

Technical Note

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
CDR	Clock Data Recovery
CML	Current Mode Logic
FIFO	First In First Out
FPGA	Field-Programmable Gate Array
LVDS	Low-Voltage Differential Signaling
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
PCB	Printed Circuit Board
PCS	Physical Coding Sublayer
PLL	Phase Locked Loop
SERDES	Serializer/Deserializer

1. Introduction

LatticeECP3, LatticeECP2/M, and LatticeSCM SERDES integrate high-speed, differential Current Mode Logic (CML) input and output buffers. This offers significant advantages in switching speed while providing improved noise immunity and limited power dissipation. Additional advantages in current-mode design include reduced voltage swing operation and significant suppression of power supply noise since the supply current is constant.

The ECP5UM and ECP5UM5G SERDES offer the same high-speed, differential CML input buffers. The SERDES on these devices use H-Bridge Low Voltage Differential Signal (LVDS) output buffers. While the H-Bridge driver provides the same advantages of improved noise immunity, reduced voltage swing operation, and suppression of power supply noise, it significantly reduces the power dissipation on the output power supply. The H-Bridge output buffer on ECP5UM5G devices supports up to 5 Gbps operation.

The CML differential receivers and drivers incorporate various programmable features and interfaces to other CML and non-CML logic signals. Off-chip signal interface design and characteristics are the focus of this document. Detailed interface requirements to external high-speed devices with LVDS and LVPECL characteristics are discussed, as well as the transmission line interconnections between devices which are required because of high data rates. Practical considerations related to printed circuit boards are also discussed. For more detailed PCB recommendations, refer to High-Speed PCB Design Considerations (FPGA-TN-02178). While nominal resistor and capacitor values are shown throughout this document, optimal values vary in each application. HSPICE models with the interface examples are provided to tune user-specific applications.

2. SERDES Input/Output Buffer Overview

CML buffers are used as the common interface to the SERDES PCS. Internal input termination on the CML receiver is provided to simplify board level interface to different kinds of external output drivers. The on-chip AC coupling capacitors can be used to level shift the input signal. These capacitors can be optionally bypassed.

The SERDES output features a selection of different impedances on the driver to match the trace impedance on the board. The nominal 50 Ω impedance is commonly used on boards for high-speed lines. Matching impedance on the SERDES output driver and the board trace minimizes reflection noise.

A simplified schematic of the serial input and output buffers with CML output driver is shown in Figure 2.1. Output buffer with H-Bridge driver is shown in Figure 2.3.

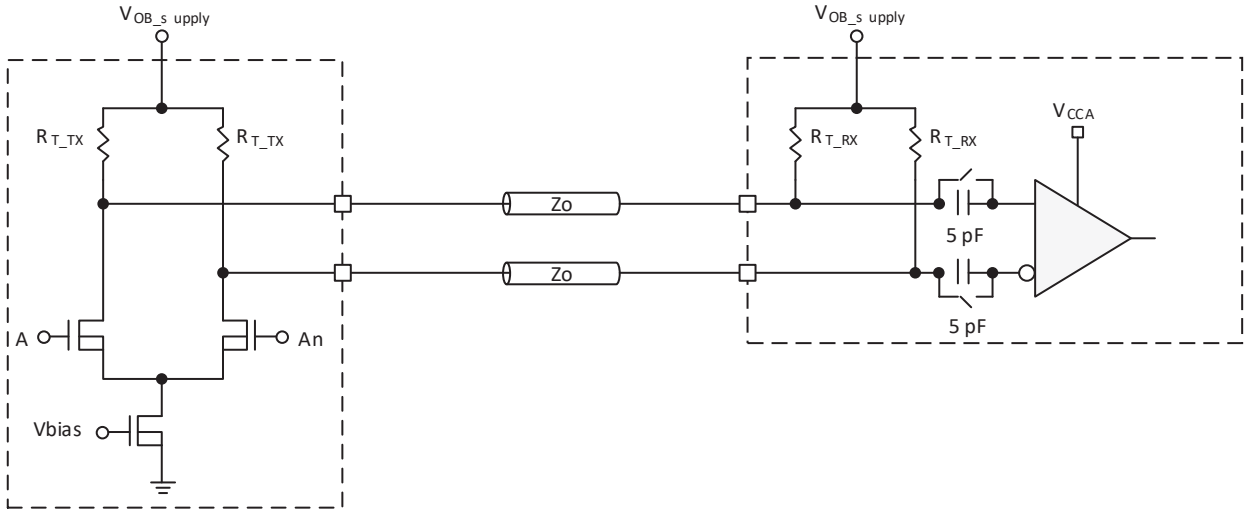


Figure 2.1. CML Input and Output Buffer Structure for LatticeECP3, LatticeECP2/M, and LatticeSCM

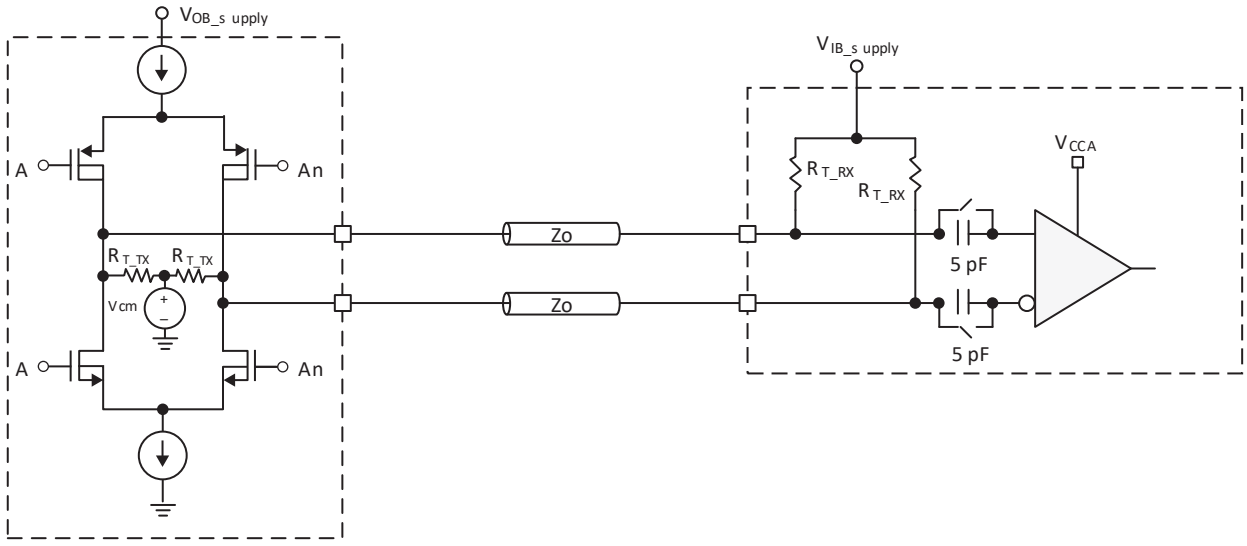


Figure 2.2. CML Input and H-Bridge Output Buffer Structure for ECP5UM, ECP5UM5G

Refer to Table 2.1 for the difference between device families on SERDES supplies, supply voltages, and other buffer parameters.

2.1. SERDES Input/Output Buffer Power Supplies

Generally, Lattice SERDES -based FPGA devices have many similarities. However, there are some differences that need to be highlighted and understood. Table 2.1 shows the difference between different families on the supplies used and the electrical signal levels on the SERDES inputs and outputs.

Table 2.1. Power Supplies and Input/Output Driver on Lattice SERDES -based Families

	Device Family	Supply Name	Nominal Value	Description
V_{OB_supply}	LatticeSCM	V_{DDOB}	1.2 V to 1.5 V	Output Buffer Supply and Voltage There is one pin per output channel.
	LatticeECP2M	V_{CCOB}	1.2 V to 1.5 V	
	LatticeECP3	V_{CCOB}	1.2 V to 1.5 V	
	ECP5UM	V_{CCHTX}	1.1 V	
	ECP5UM5G	V_{CCHTX}	1.2 V	
V_{IB_supply}[1]	LatticeSCM	V_{DDIB}	1.2 V to 1.5 V	Input Buffer Termination Supply and Voltage There is one pin per input channel.
	LatticeECP2M	V_{CCIB}	1.2 V to 1.5 V	
	LatticeECP3	V_{CCIB}	1.2 V to 1.5 V	
	ECP5UM	V_{CCHRX}	1.1 V	
	ECP5UM5G	V_{CCHRX}	1.2 V	
V_{CCAUX}	LatticeSCM	V_{DDAX25}	2.5 V	Auxiliary Supply and Voltage Used mostly on I/I Control and current reference circuits inside the SERDES block Note: VCCAUX on ECP3 shares same supply with VCCAUX in FPGA core
	LatticeECP2M	$V_{CCAUX33}$	3.3 V	
	LatticeECP3	V_{CCAUX}	3.3 V	
	ECP5UM	V_{CCAUXA}	2.5 V	
	ECP5UM5G	V_{CCAUXA}	2.5 V	
V_{CCA}	LatticeSCM	V_{CC12}	1.2 V	Analog Supply and Voltage Used on mixed signal circuits inside the SERDES block.
	LatticeECP2M	$V_{CCP}/V_{CCRX}/V_{CCTX}$	1.2 V	
	LatticeECP3	V_{CCA}	1.2 V	
	ECP5UM	V_{CCA}	1.1 V	
	ECP5UM5G	V_{CCA}	1.2 V	
R_{T_TX}	LatticeSCM	—	50/75/5K	Transmitter Buffer Impedance
	LatticeECP2M	—	50/75/5K	
	LatticeECP3	—	50/75/5K	
	ECP5UM	—	50/75/5K	
	ECP5UM5G	—	50/75/5K	
R_{T_RX}	LatticeSCM	—	50/75/5K	Receiver Termination
	LatticeECP2M	—	50/75/5K	
	LatticeECP3	—	50/75/5K	
	ECP5UM	—	50/75/5K	
	ECP5UM5G	—	50/75/5K	
V_{OD}	LatticeSCM	—	500 mV	Typical Differential Output Amplitude from Transmitter Outputs
	LatticeECP2M	—	500 mV	
	LatticeECP3	—	500 mV	
	ECP5UM	—	500 mV	
	ECP5UM5G	—	500 mV	

	Device Family	Supply Name	Nominal Value	Description
V_{OCM}	LatticeSCM	—	V_{DDOB} - 0.25 V	Differential Output Common Mode Voltage
	LatticeECP2M	—	V_{CCOB} - 0.25 V	
	LatticeECP3	—	V_{CCOB} - 0.25 V	
	ECP5UM	—	0.55 V	
	ECP5UM5G	—	0.55 V	
V_{ID}	LatticeSCM	—	80 mV min.	Minimum Differential Input Amplitude on Receiver Inputs
	LatticeECP2M	—	100 mV min.	
	LatticeECP3	—	150 mV min.	
	ECP5UM	—	150 mV min.	
	ECP5UM5G	—	150 mV min.	
V_{ICM}(DCC)	LatticeSCM	—	0.6 V to 1.2 V	Differential Input Common Mode Voltage Range, Internal DC Coupled
	LatticeECP2M	—	0.5 V to 1.2 V	
	LatticeECP3	—	0.6 V to 1.2 V	
	ECP5UM	—	0.6 V to 1.1 V	
	ECP5UM5G	—	0.6 V to 1.2 V	
V_{ICM}(ACC)	LatticeSCM	—	0 V to 1.5 V	Differential Input Common Mode Voltage Range, Internal AC Coupled
	LatticeECP2M	—	0 V to 1.5 V	
	LatticeECP3	—	0.1 V to V_{CCA} + 0.2 V	
	ECP5UM	—	0.1 V to V_{CCA} + 0.2 V	
	ECP5UM5G	—	0.1 V to V_{CCA} + 0.2 V	

Note:

1. This supply provides termination center-tap voltage on input signals. If external signal is AC coupled, this provides DC bias. It can be left high-impedance if externally DC coupled.

On all devices in the SERDES based families, each channel has its own supply for the receiver termination and transmitter output driver. This allows each Rx channel to terminate to a different voltage.

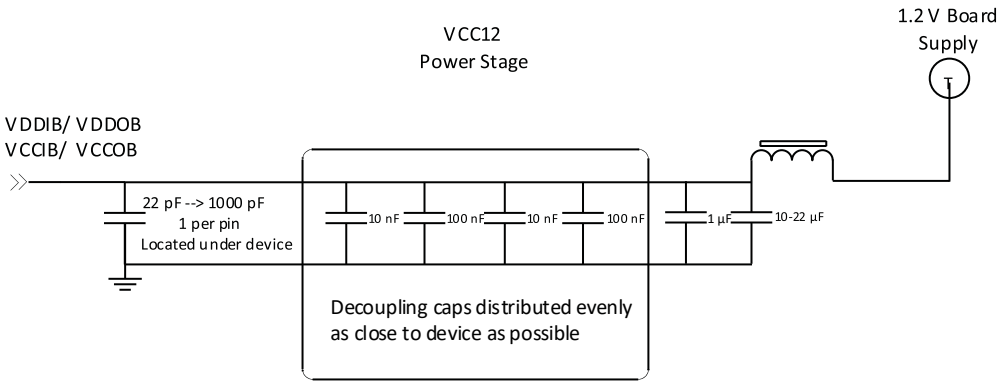
Lattice devices use several supplies for the analog circuitry blocks of the SERDES. All analog supply pins must be connected to a voltage supply regardless of whether the channel is used in the application. Unused channels can be powered off internally to conserve power. The analog supplies should be isolated on the PCB to deliver quiet, noise-free power. These supplies are V_{CC12} on LatticeSCM, V_{CCP}/V_{CCRX}/V_{CCTX} on LatticeECP2M, VCCA on LatticeECP3, ECP5UM, and ECP5UM5G.

There is a very stringent requirement often overlooked by designers to isolate noise generated by digital components. It is necessary to provide a low-noise supply for the sensitive analog portions of the SERDES devices. Noise due to variations in the power supply voltage can be coupled into the analog portion of the chip and may produce unwanted fluctuations in the sensitive stages of the device.

There are several power supplies associated with the SERDES /PCS of the device. All dedicated SERDES supply pins, excluding the input termination supply and output driver supply pins, must be connected regardless of the design. The input termination supply and output driver supply pins only need to be connected for the channels used in a design. In situations where only the Rx section is used, it is recommended that the associated output driver supply pins be connected to an appropriate power supply regardless that the Tx section is not being used. This strategy shields noise from the channel. Likewise, if only the Tx is used, the respective input termination supply pins shall be connected. Similarly, the HDIN and HDOUT pins can be left unconnected in designs not using particular channels.

In instances where PCB power distribution cannot be sufficiently bypassed, the designer might be tempted to use several different active devices, such as voltage regulators, to serve as the decoupling stages for these power supplies. Supplying DC power to each stage through a separate inductor or “choke” while also bypassing to ground effectively accomplishes the same result without the use of active components. In passive filter networks the choke offers a high impedance path to any errant signals or noise between stages while offering a very low resistance path to the DC power. This technique is appropriate for both Rx termination and Tx driver supplies.

Figure 2.3 show an example of how to isolate a 1.2 V power supply source that is also used in digital logic on the same board for the SERDES input termination and output driver supplies.



Note: The use of Passive-Filter Networks is **not recommended** for low-impedance power supplies such as VCC Core.

Figure 2.3. Passive Filter Network "Quiet Supply" Example

- High *Q*, minimum inductance decoupling caps
  - SMT or chip capacitors made of ceramic are best. Use several size caps in parallel (such as 1 µF, 0.1 µF, 0.01 µF, and so on). The reason for this is that each cap with its associated inductance has its own series resonant frequency. Therefore, it is best to have a wide range of capacitor values to provide an overall lower power supply impedance over the effective frequency range.
- Use high *Q* – low *R* Ferrite Bead
  - The downside of ferrite is that it changes inductance as the current or flux changes. In large currents, it can saturate. Understanding the frequency, AC and DC current requirements is important in choosing the correct inductor. A good choice is a bead from Murata, BLM41PG471SN1L.

Other options for power distribution systems should also be explored to gain an understanding of the sources of power supply noise and voltage ripple. Using the before-mentioned passive filter techniques are a good start to filter the ripple generated by the power supplies. The filter must sufficiently attenuate the low-frequency harmonics of the primary switching supply, so an understanding of what frequency needs to be cut-off by the post-supply filter is important. One recommendation is to build an LC passive-network that cuts off a decade below the primary frequency. Typically, high-frequency noise generated by supplies can be easily attenuated using capacitors placed after the inductor or ferrite bead post-filter as shown in Figure 2.3.

Both linear and switching voltage regulators have advantages and disadvantages when used in Lattice FPGA systems. Depending on the requirements of the system either may be a suitable choice. Switching regulators are a better choice when the input voltage is less than or much greater than the desired output, when multiple outputs are desired, and when power dissipation must be kept low. There is no argument that switching regulators are more efficient than low drop-out regulators (LDO). A switching regulator can exhibit 90% efficiency versus 36% for an LDO. However, a switching regulator may not always meet all the critical needs of the design. Switching Voltage Regulators have these advantages:

- High efficiency (reduces source power requirements and need for heat sinking)
- Capable of handling higher power densities
- Single or multiple output voltages, greater or less than the input voltage

They have these disadvantages:

- Greater output noise/ripple, especially at the switching frequency
- Slower transient recovery time

Switching regulators are well-suited for powering the FPGA core and I/O power supplies where high power requirements play a factor in the board power design. The high efficiency reduces heat and power concerns that linear regulators exhibit. However, the ripple generated by switching regulators is not desirable for use with sensitive analog power supplies. Using post-supply filter networks can attenuate the unwanted ripple. Typically, the added noise on the output is at the switching frequency. If this frequency is below the bandwidth of the SERDES or PLLs it can add jitter and reduce the signal integrity of the system.

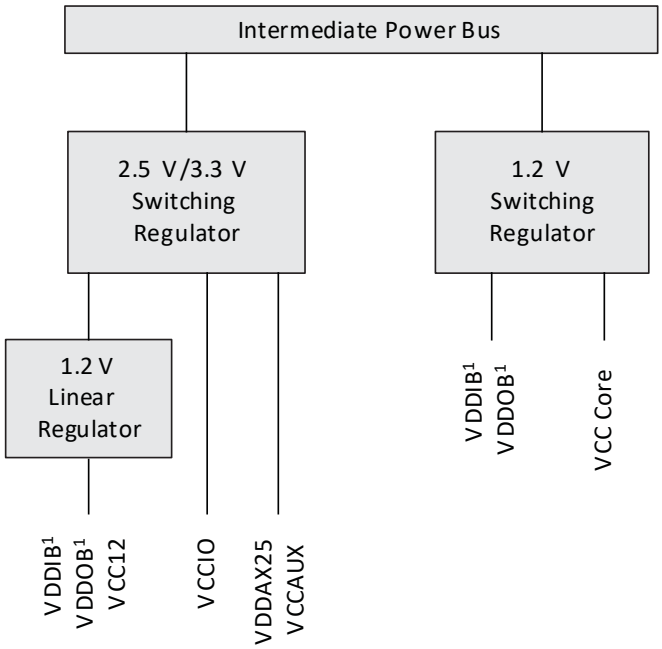
In general, linear regulators are a better choice when the input voltage is a few volts higher than the output but not closer than the regulator's dropout voltage, and when the load current is less than about 3 A. Linear Voltage Regulators have these advantages:

- Simple and small board application
- Low output ripple voltage
- Excellent line and load regulation
- Fast response time to load or line changes
- Low electromagnetic interference (EMI)

They have these disadvantages:

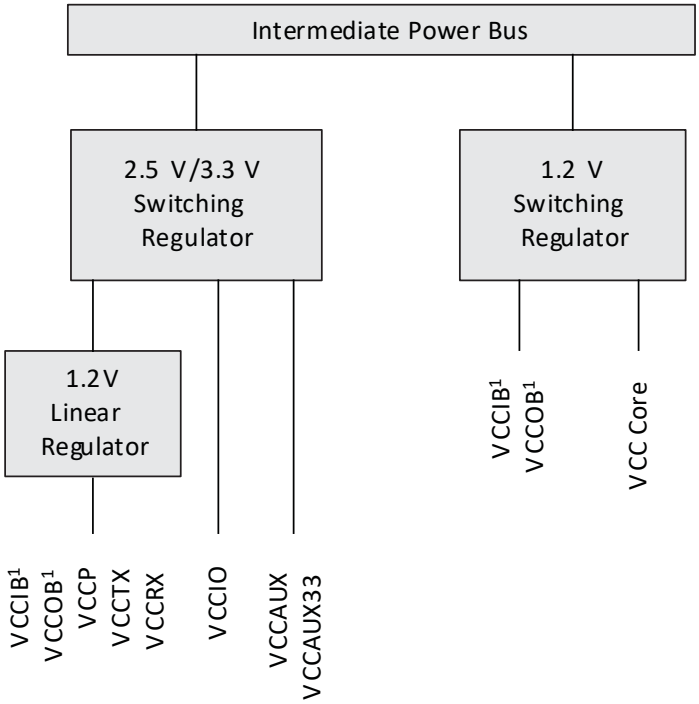
- Low efficiency, especially with higher input voltages
- Large space requirement if heatsink is needed

This type of regulation is desired for the quiet analog supplies used for the PLLs and SERDES. These regulators offer a good amount of noise rejection and generate no ripple. They work well to supply the lower power draw from the analog circuitry of the FPGA. Lattice strongly recommends using linear regulators to supply the analog SERDES power supplies.



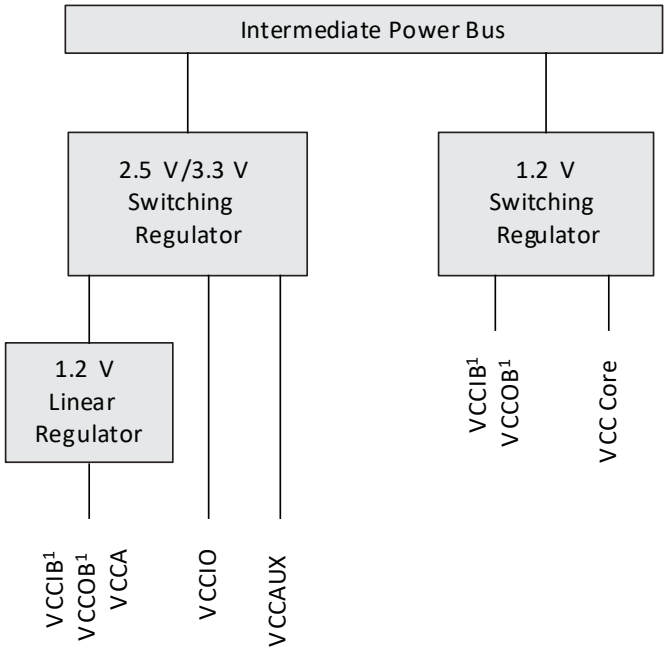
Note:
1. VDDIB and VDDOB should be passively filtered from either 1.2 V supply.

Figure 2.4. Combined Switching and Linear Regulator Power Scheme for LatticeSCM



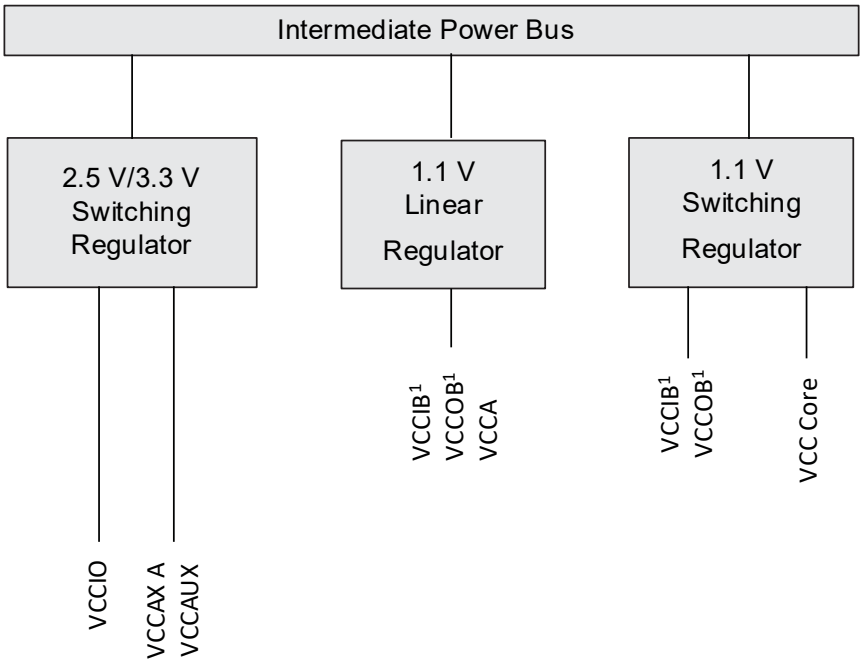
Note:
1. VCCIB and VCCOB should be passively filtered from either 1.2 V supply.

Figure 2.5. Combined Switching and Linear Regulator Power Scheme for LatticeECP2M



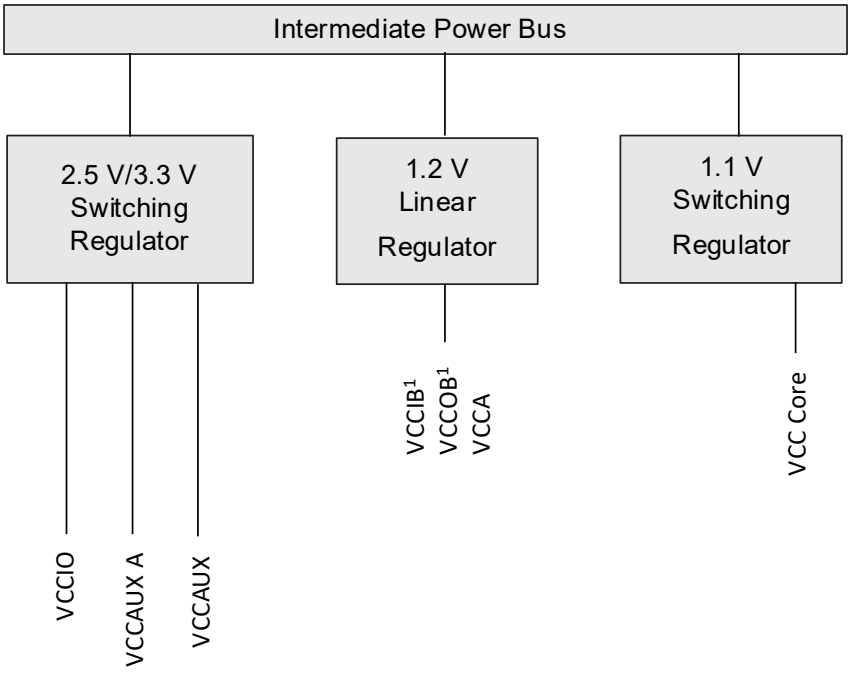
Note:
1. VCCIB and VCCOB should be passively filtered from either 1.2 V supply.

Figure 2.6. Combined Switching and Linear Regulator Power Scheme for LatticeECP3



Note:
1. VCCIB and VCCOB should be passively filtered from either 1.1 V supply.

Figure 2.7. Combined Switching and Linear Regulator Power Scheme for ECP5UM



Note:
1. VCCIB and VCCOB should be passively filtered.

Figure 2.8. Combined Switching and Linear Regulator Power Scheme for ECP5UM5G

Combining the use of a switching regulator with a linear regulator is a way to reduce board power dissipation. An example of this is shown in Figure 2.4 to Figure 2.8. In this design, a switching regulator provides the correct voltage levels while the use of the linear regulator filters the switching noise. Note that the correct power supply decoupling and filtering is needed. Switching regulators are most efficient when they're driving the loads for which they were designed. When the output is not heavily loaded linear regulator can be more efficient under these conditions. Using this combination of regulators is helpful to meet the requirements of high-performance FPGA designs that require distribution of multiple power supplies.

3. General FPGA Recommendations

In general, low noise analog power supply networks are a stringent requirement for the proper operation of embedded SERDES and other analog functions such as PLL. The noise due to variations in the power supply can be coupled into the supply for PLL, and would have the same effects as noise on the SERDES analog supplies. These PLLs should follow the suggested recommendations in Table 3.1, for providing clean power as mentioned for SERDES supplies in the LatticeSCM, LatticeECP2M and LatticeECP3 families.

ECP5UM and ECP5UM5G families do not have separate PLL supply pins, they use the VCC core supply voltage. There is an internal filter between the core supply and internal PLL supply to ensure digital switching noise is not coupled into the PLL.

Table 3.1. PLL Supplies per Device

Device	FPGA PLL Supply	Quiet Supply Voltage (Nominal)
LatticeSCM	VCC12	1.2 V
LatticeECP2M	VCCPLL_[L:R]	1.2 V
LatticeECP3	VCCPLL_[L:R]	3.3 V

4. PCB Design Considerations

Many existing documents provide guidance to avoid the pitfalls of PCB designs with SERDES and high-speed I/O. There are still a few underlying issues that often go misunderstood or overlooked. The interaction of an FPGA's Simultaneously Switching Outputs (SSO) can cause many system-level issues that lead to degradation of the overall SERDES performance.

Lattice FPGA I/O have enabled the building of many complex systems. These abundant and flexible FPGA I/O include many speed and signal interface features such as drive strength and termination options. SSO is noise due to multiple I/O pins switching at the same time. These changing currents induce voltages inadvertently affecting other sensitive stages of the device. LatticeSCM devices include many innovative methods to overcome specific device and package sensitivities to SSO and in-package crosstalk. This can mostly be corrected by minimizing the total inductance of return paths, similar to what has been done in Lattice package designs. PCB designs need to apply careful techniques to reduce the likelihood of PCB-related crosstalk and SSO noise that degrades system performance.

The leading cause of PCB-related SERDES crosstalk is FPGA outputs located in close proximity to the sensitive SERDES power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs, and to ensure that noise does not infiltrate into these analog supplies. Although coupling has been reduced in the device packages, the vias within the BGA field of the PCB can cause significant noise injection from any I/O pin adjacent to SERDES data, reference clock, and power pins as well as other critical I/O pins such as clock signals.

Many PCB designs can create cross-coupling of the FPGA I/O to the analog supply pins by via-to-via coupling. This coupled noise on the PCB can cause the SERDES performance to degrade dramatically. Enabling amplitude boost mode of the SERDES typically improves noise immunity for both the Rx and Tx portions of the SERDES, especially noted at rates above 2.7 Gbps.

The system designer can mitigate this problem by implementing differential signaling standards to and from the FPGA rather than using single-ended buffers. Where single-ended signals must be used, the PCB designer must pay attention to via and signal placement when in close proximity to the analog power supplies and avoid routing the single-ended buses near the high-speed SERDES channels. It is a better practice to use the I/O pins in closer proximity of SERDES data, reference clock, and analog power pins for static control signals or signals with lowdrive strength, slow-slew rate, and limited capacitive loading (terminated signaling also improves this situation). The suggested pins to avoid for this purpose, if possible, are shown in Table 4.1 for each LatticeSCM package. For LatticeECP2/M devices, see LatticeECP2/M Pin Assignment Recommendations (TN1159). LatticeECP3 devices have similar recommendations listed in LatticeECP3 Hardware Checklist (FPGA-TN-02183).

Table 4.1. LatticeSCM PCB Aggressor I/O Pins

Device	Package	Package Type	Aggressive I/O Pins[1]
SCM15	256 fpBGA	Wire-bond	E7
SCM15/SCM25	900 fpBGA	Wire-bond	F22[2]
SCM25/SCM40	1020 fpBGA	Flip Chip	D2, E2, F2, D31, E31, F31
SCM40/SCM80/SCM115	1152 fpBGA	Flip Chip	D2, D33, F14, F21, G14, G21,H13, H14, H21, H22
SCM80/SCM115	1704 fpBGA	Flip Chip	F27, G1, G2, G3, J17, J18, G40, G41, G42, K18, M9, N9, N10, N33, N34, M34

Notes:

1. I/O pins are potential PCB coupled noise sources to analog supplies and recommendations should be followed.
2. F22 is a dual function pin. When using SPI Flash, F22 is used to source the SPI Flash chip select and should not be connected to *soft ground*.

The best-case scenario is to drive these signals with a *soft ground*. Connecting an active output buffer and driving a low signal builds an effective *soft ground*. This pin should be connected to the ground plane of the PCB. This connection serves as a return path and helps create additional noise immunity. Pins are listed that possibly influence with the analog supplies on the board as well as pins that are adjacent to high-speed SERDES data pins that could get coupled on the PCB.

Additional recommendations include:

- Do not route the SERDES supply connections as traces. Rather, use planes or very wide bus structures on other non-adjacent layers to high-speed signal routing and keep them shielded by adjacent ground layers.
- Blind-vias are better than through-hole vias for making connection to the I/O. This limits the amount of coupling between vias. If through-hole vias are required, place high frequency decoupling capacitors directly beneath the device adjacent to the V_{CC12} power via as shown in Figure 4.1 in the example for LatticeSCM.
- Maintaining the greatest distance between single-ended I/O and the analog supplies is always required. It is always best to keep the analog supplies and the single-ended traces separated vertically in the PCB stack-up when working in close proximity on the board.

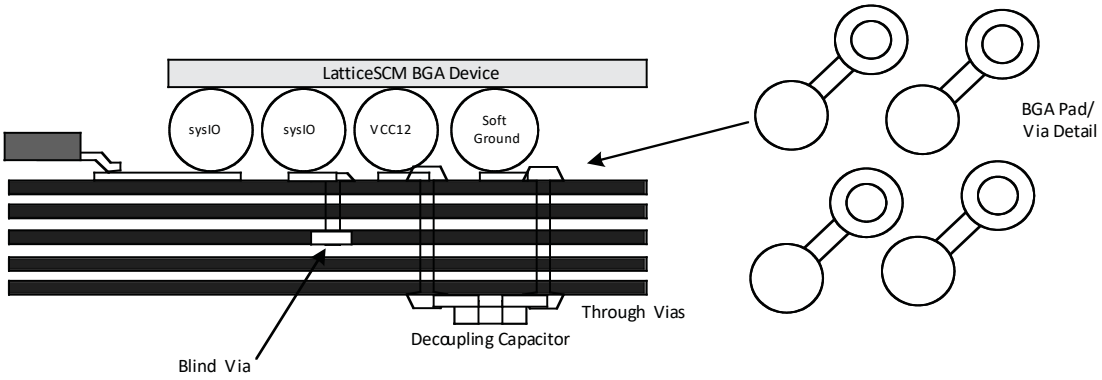


Figure 4.1. PCB Via Stack Up Detail for LatticeSCM

In Figure 4.1, coupling is caused by the mutual inductance occurring in the area between the I/O signal path and the V_{CC12} via. Blinding the signal via and reducing the stub minimizes the capacitive coupling effect. Following recommendations designed to minimize this effect reduces the coupling. I/O pins having close proximity to the V_{CC12} pins vary in different packages and packaging variations also influences noise immunity. The issues related to these locations are due to the way the pins escape or route away from the device. Determining the best escape route from the device's BGA field is critical to minimizing the effects of coupled noise on the board.

4.1. Best Practices for SERDES Power Supply PCB Routing

- When possible, do not use specified I/O directly adjacent to an analog power pin.
- Routing should also be kept away from analog power vias when escaping from the device.
- It is best practice to shield any routing traces from the analog power pin connections. This can be done with power and ground planes (ground planes preferred) above and below as well as ground shield routing on the same layer.
- Carefully place same layer shielding as to not create edge-coupling issues. Typically, 3 W spacing is required to prevent edge coupling.
- Consider keeping quiet SERDES supply connections on the first possible power layer closest to the device side where is can be shielded by a ground layer.
- High-speed I/O signals should escape on the signal layer non-adjacent to the analog supply.
- High-speed I/O signals should be routed after all SERDES and analog power is routed. If the quiet supply vias are blinded, this restriction can be relaxed as long as the quiet power plane is kept close to the device side of the board as possible.

4.2. Special Considerations to Reduce Tx Jitter and Increase Jitter Tolerance for the LatticeSCM

For wire-bond packages, it is also a good practice at any speed to limit the number of single-ended outputs simultaneously switching outputs in I/O banks adjacent to the SERDES channels. For the 256-ball fpBGA, this is I/O Bank 1 and for the 900-ball fpBGA packages, these are I/O Bank 1, Bank 2, and Bank 7. This becomes a priority as the SERDES rate increases.

At SERDES speeds above 3.2 Gbps in wire-bond packages, the single-ended outputs in Bank 1 should be limited to configuration signals (including up to 8 bit MPI interface connections for the 900-ball fpBGA). For Bank 2 and Bank 7, the number of single-ended outputs should be limited to 8 or less in the 900-ball fpBGA.

For the 256-ball fpBGA package use Bank 1 for:

- Differential I/O or static configuration and control signals
- Single ended inputs
- Only, if necessary, single ended outputs can be used but should be limited to a 4 mA drive with slewlim mode enabled

For the 900-ball fpBGA package, use Bank 1, Bank 2, and Bank7 for:

- MPI pins (8 bit only)
- Differential I/O or static configuration and control signals
- Single ended inputs
- Only, if necessary, single ended outputs can be used but should be limited to a 4 mA drive with slewlim enabled

It is less critical to limit the number of single-ended outputs in flip-chip packages. However, limiting the number of outputs, reducing drive-strength, enabling slew limited mode and reducing the capacitive loads in Bank 1, Bank 2, and Bank 7 also has a small effect on improving SERDES performance. At SERDES speeds greater than 3.2 Gbps this effect becomes larger.

5. SERDES Input/Output External Interfaces

The high speed of the serial SERDES I/O makes understanding the interface parameters especially important to you. Proper interpretation of the parameters is needed for successful integration within a system. Signal interconnection performance, reliability and integrity are closely tied to these characteristics and their variation limits. This section summarizes and discuss critical serial buffer interface parameters. Correctly specifying the buffer I/O is a complex process. Methods used include extensive SPICE simulation and laboratory measurements.

All interconnection circuits described in this section should use matched length pairs of 50 Ω transmission lines. Each should provide characteristic impedance termination of the line to provide maximum signal bandwidth. 50 Ω, an industry standard, provides maximum compatibility and suits present printed circuit board technology interconnections well for circuit pack and backplane applications. It is also consistent with 100 Ω balanced transmission line interfaces which are becoming popular for high bandwidth shielded pair cable connections. However, for ease of integration into 75 Ω impedance characteristic systems such as video, Lattice SERDES devices are optimized to terminate directly in both 50 Ω and 75 Ω applications.

5.1. External DC Coupling

The SERDES high-speed serial buffers are optimized to interface externally to other similar buffers. For some interfaces, a direct interconnection of Lattice SERDES buffers requires no external devices or components at the PCB level. The advantages of DC coupling include simplified board design and no DC wander issues. It is also useful in all coded-data streams including SONET and NRZ data applications. Systems with a need for wide bandwidth or where DC unbalanced code is used, can take advantage of DC coupling.

When using DC coupling interface, it is important to note the absolute voltage on the input pins does not exceed the voltage specified on the Data Sheet due to difference in electrical signaling levels of the interface standard. If signal level exceeds the Data Sheet specification, the external signal needs to be either attenuated, or level shifted.

When external DC couple is used, the on-chip input termination resistor to the input buffer termination power supply may create a load on the signal, if the termination supply voltage is different from the signal's common mode voltage, Vcm. This can help to level shift the signal if the signal by adjusting the termination supply voltage. Alternatively, the termination supply can be left unconnected, or connected to a capacitor. When the supply is not powered, the termination resistor becomes differential termination with center-tap at high Z, and it would follow the signal's Vcm. Different channel has its own termination supply, so the center-taps of each channel's resistor are not connected together.

5.2. External AC Coupling

In some high-speed applications, AC coupling is preferred for various reasons. In some interface standards, such as PCI Express, AC coupling is required on the transmitter. AC coupling is used to change the common-mode voltage level of an input signal driven from a source that is not compatible with the receiver specification on Lattice's SERDES. The AC coupling capacitor changes the DC component (common-mode voltage), while passing along the AC component (voltage swing), of the signal. The internal termination resistors shown in Figure 2.1 and Figure 2.2 to the input buffer termination power supply provides the DC bias of the AC coupling capacitor. This internal termination resistor can be turned off, and be implemented externally on the board and requires more external passive components.

AC coupling requires that the signal is transmitted with DC balanced line coding. DC balanced means the average number of transmitting 1s and 0s is the same. This is to avoid baseline wandering on the signal. Also, the line code should minimize the run-length of continuous input data (CID), consecutive same 1s or 0s over multiple bit time, to avoid charges after the AC coupling capacitor to leak away too much over the CID and distort the signal. The ANSI standard 8B10B line coding is a widely used coding which is DC balanced, and guaranteed to have CID run-length of less than 7.

All receiver channels in Lattice SERDES -based devices have selectable internal AC coupling capacitors. External AC coupling capacitors are used to ensure that the transmitted signal source meets the SERDES receiver input requirements as specified in Lattice's Data Sheet. Internal AC coupling capacitors further level shift the signal to its optimal operating voltage, with the internally generated biased Vcm on the signal. The use of external AC coupling capacitors and internal AC coupling capacitors are independently selected, and not excluding the other. Also to be noted is when the external Vcm is below Vicm(dc) minimum, internal AC couple must be used to level shift to the internal voltage.

The addition of external capacitors (Cext) for AC coupling requires some careful consideration. The designer should select a capacitor knowing the requirements of the system. It is important to minimize the pattern-dependent jitter associated with the low-frequency cutoff of the AC coupling network. When NRZ data containing long strings of identical 1s or 0s is applied to this high-pass filter, a voltage droop occurs, resulting in low-frequency, pattern-dependent jitter (PDJ).

The FPGA supports both internal AC coupling and DC coupling. When using the AC coupling mode with external off-chip series capacitors (Cext) refer to the values shown in Table 5.1.

Table 5.1. Off-chip AC Coupling Capacitor

Description	Min.	Max.	Units
8b/10b (XAUI)	20	—	nF
SONET	22	—	nF
PCI Express	100 (Gen 1 & 2)	220 (Gen 3+)	nF

5.3. Internal AC Coupling

As described above, an internal AC coupling capacitor is used to level shift the external signal it is internally generated Vcm, for optimal operation. When the external Vcm is lower than the required voltage, as specified on the Data Sheet, internal AC coupling must be used.

It is recommended to always use internal AC coupling whenever possible. The exceptions to this are when the signal is not using DC balanced line coding, the CID run-length is too long, or the data rate is too slow.

5.4. Interface to LVDS Device

LVDS, like CML, is intended for low-voltage differential signal point-to-point transmission. Many commercial LVDS devices provide internal 100 Ω input terminations. They are typically intended for use with 100-Ω characteristic impedance transmission line connections. Standard LVDS is specified with about 3 mA signal-current that translates to a nominal signal voltage of approximately 600 mVp-p (differential). Low power LVDS provides about 2 mA signal current. LVDS input and output parameters are shown in Table 5.2, as specified in the LVDS Standard.

Table 5.2. LVDS Specifications

Symbol	Parameter	Conditions	Min	Max	Units
Driver Specifications					
VOH	Output voltage high	Rload (diff) = 100 Ω	—	1475	mV
VOL	Output voltage low	Rload (diff) = 100 Ω	925	—	mV
VOD	Output differential voltage	Rload (diff) = 100 Ω	250	400	mV
Ro	Output impedance, single ended	Vcm = 1.0 V to 1.4 V	40	140	Ω
Receiver Specifications					
Vi	Input voltage range	—	0	2400	mV
Vidth	Input differential threshold	—	–100	+100	mV
Vhyst	Input differential hysteresis	—	25	—	mV
Rin	Receiver differential input impedance	—	90	110	Ω

Within common LVDS receivers, an internal or external input differential termination of 100 Ω is typically needed between the P and N input ports. This termination resistor is usually floating with respect to ground. In the SERDES CML receiver, the differential input termination resistor is center-tapped, and AC coupled to ground or left floating. VDDIB can also be connected to a power supply equal to the common-mode level required for proper operation of the output buffer. In a common LVDS-to-CML application, a simple direct interface can be used in many applications. The Lattice CML output drivers and input receivers are internally terminated to 50 Ω in this application. Figure 5.1 illustrates a recommended interface between Lattice CML buffers and commercial LVDS input and output buffers. This interface requires no external components utilizing the internal CML features. The simulation results of the interface are plotted in Figure 5.1.

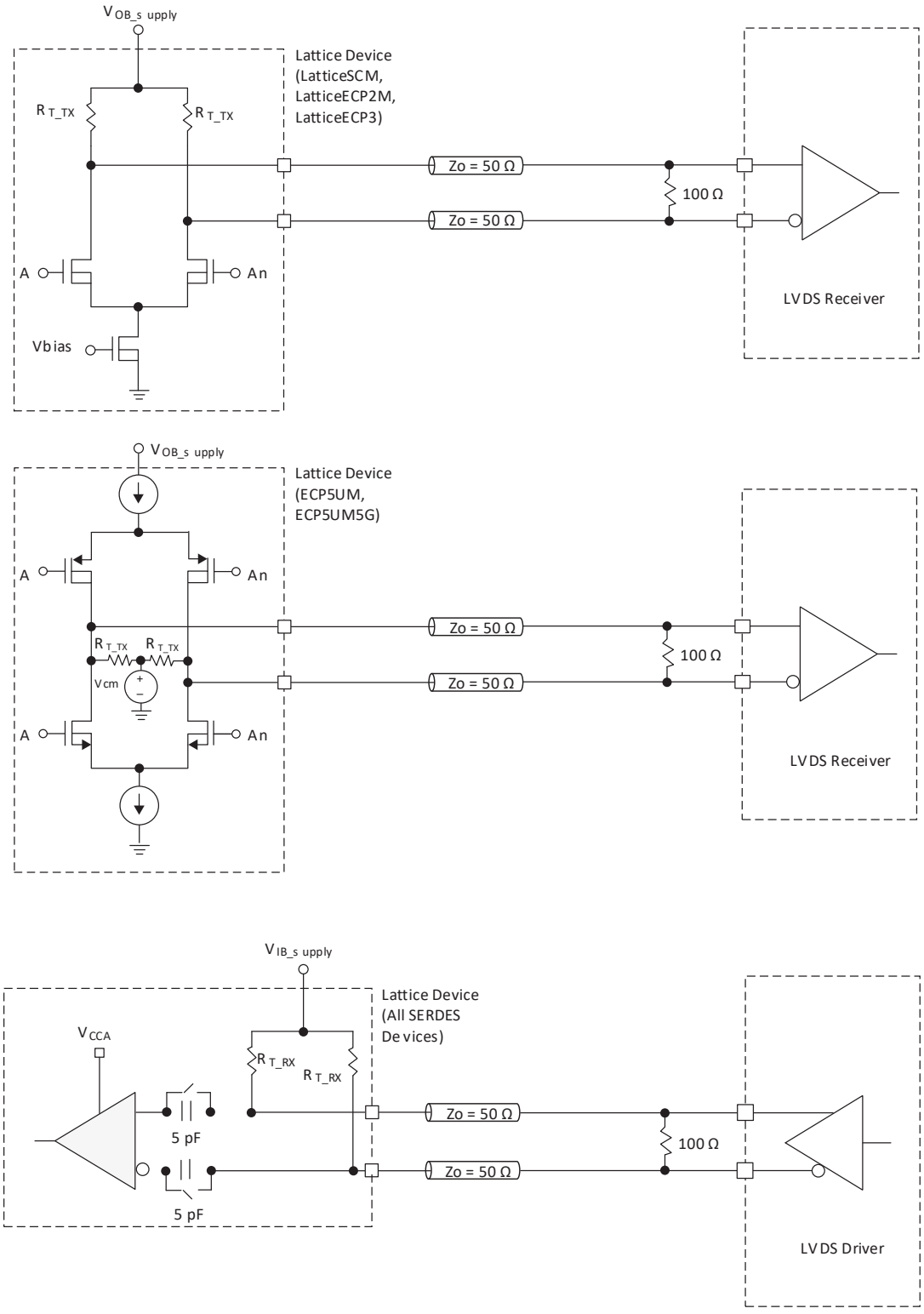


Figure 5.1. DC-Coupled to/from LVDS Interface Diagram

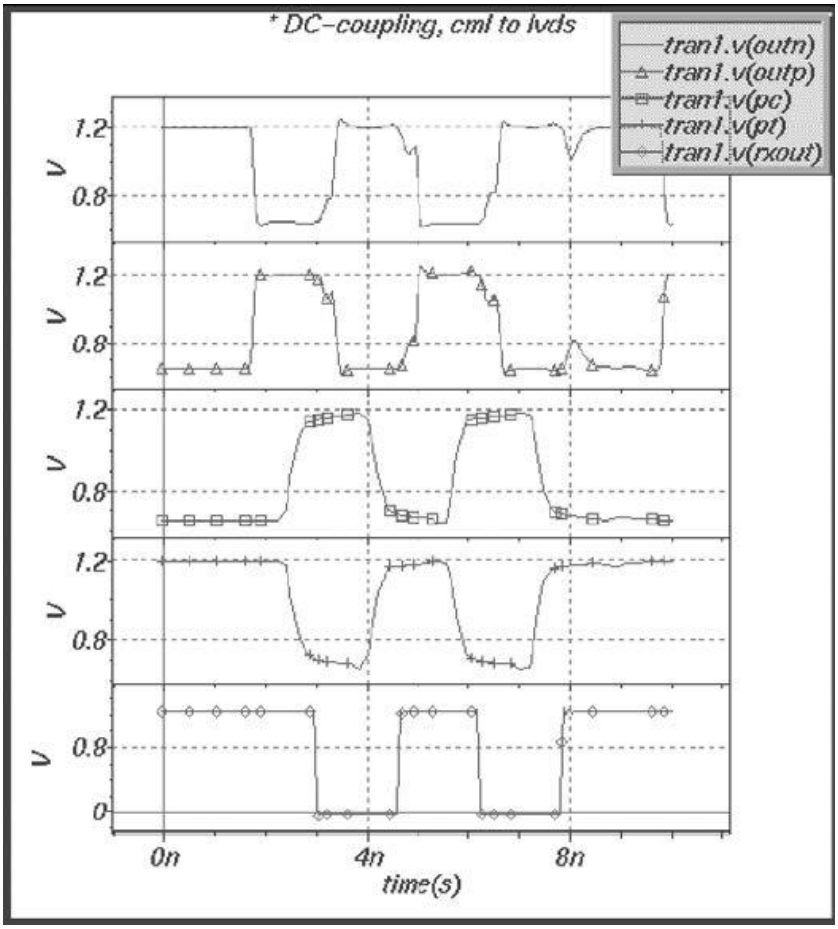


Figure 5.2. Lattice CML Driver to LVDS Receiver Simulation

Higher common mode noise tolerance may be achieved with alternate AC-coupled LVDS driver to SERDES receiver connection, as shown in Figure 5.3. This increases the receiver tolerance to common-mode input noise voltage and provide a higher tolerance range to common-mode and system and ground noise.

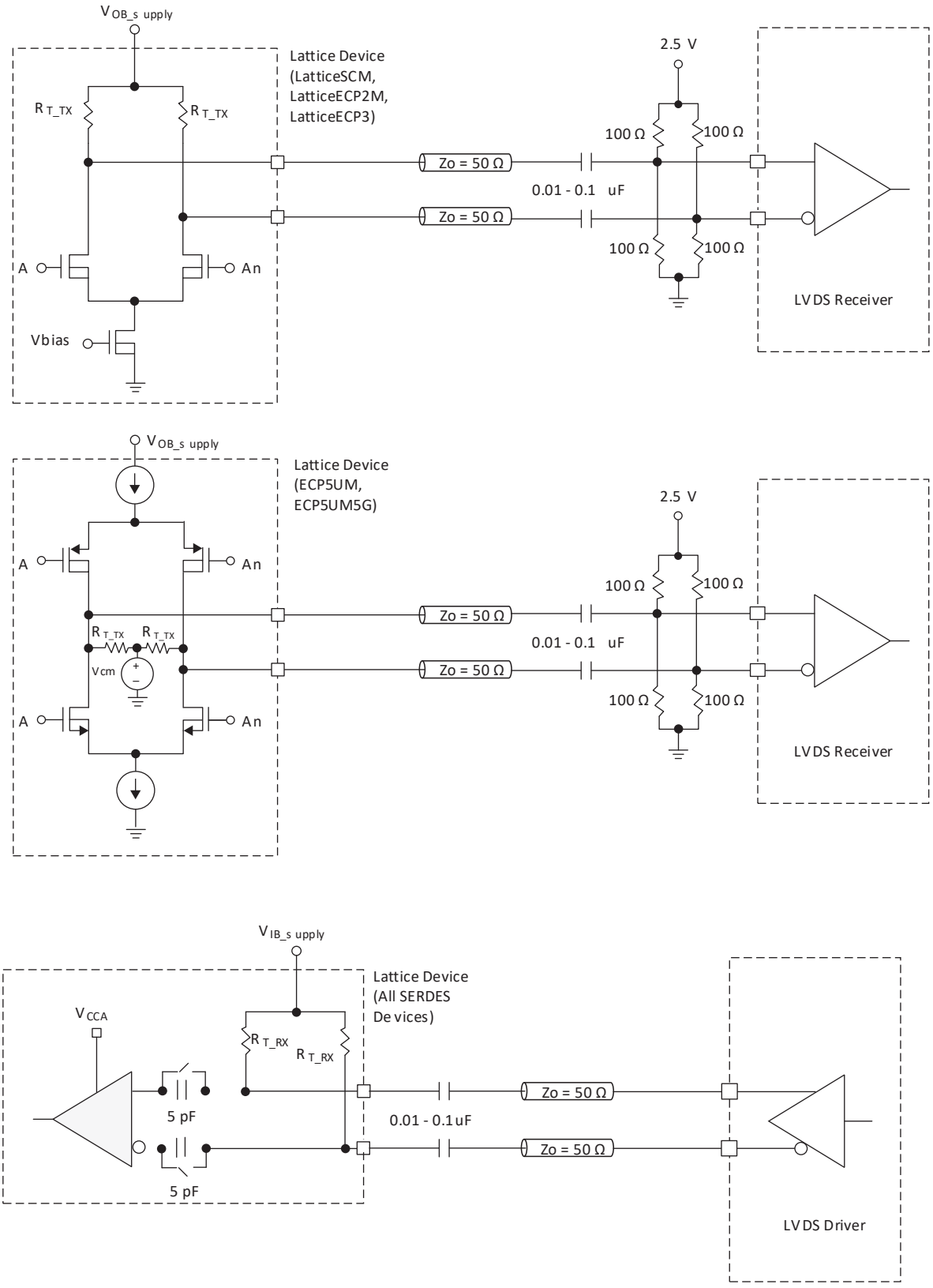


Figure 5.3. AC-Coupled to/from LVDS Interface Diagram

5.5. Interface to LVPECL Device

LVPECL is a differential I/O standard that requires a pair of signal lines for each channel. It is used in longer-haul electrical transmission. The differential transmission scheme is less susceptible to common-mode noise than single-ended transmission methods. LVPECL standards require external termination resistors to reduce signal reflection. The standard voltage swing for the differential pair is approximately 850 mV, and the typical LVPECL VCC is 3.3 V.

Table 5.3. Typical LVPECL Specifications

Symbol	Parameter	Conditions	Min	Max	Units
Voh	Output voltage high	Outputs terminated with 50 Ω to Vcco – 2.0 V	2215	2420	mV
Vol	Output voltage low	Outputs terminated with 50 Ω to Vcco – 2.0 V	1470	1680	mV
Vod	Output differential voltage	Outputs terminated with 50 Ω to Vcco – 2 .0 V	535	950	mV
Ro	Output impedance, single ended	Vcm =1.0 V to 1.4 V	3	10	Ω
Vi	Input voltage range, common mode	< 500 mVp-p > 500 mVp-p	1.1 1.3	3.1 3.1	V
Vin-diff	Input voltage range, differential mode	—	200	>2000	mVp-p
Iih	Input HIGH current	—	—	–150	µA
Iil	Input LOW current	—	–600	—	µA

Table 5.3 shows typical LVPECL specifications. The Vcm, common-mode voltage is around 2 V, which is higher than the allowable input common-mode voltage of the CML receiver. AC coupling is required to level shift the Vcm to the level CML needs.

An AC-coupled solution is shown in Figure 5.4. This scenario allows higher impedance termination at LVPECL Rx end, without causing signal distortion. Figure 5.5 shows the results of the simulation.

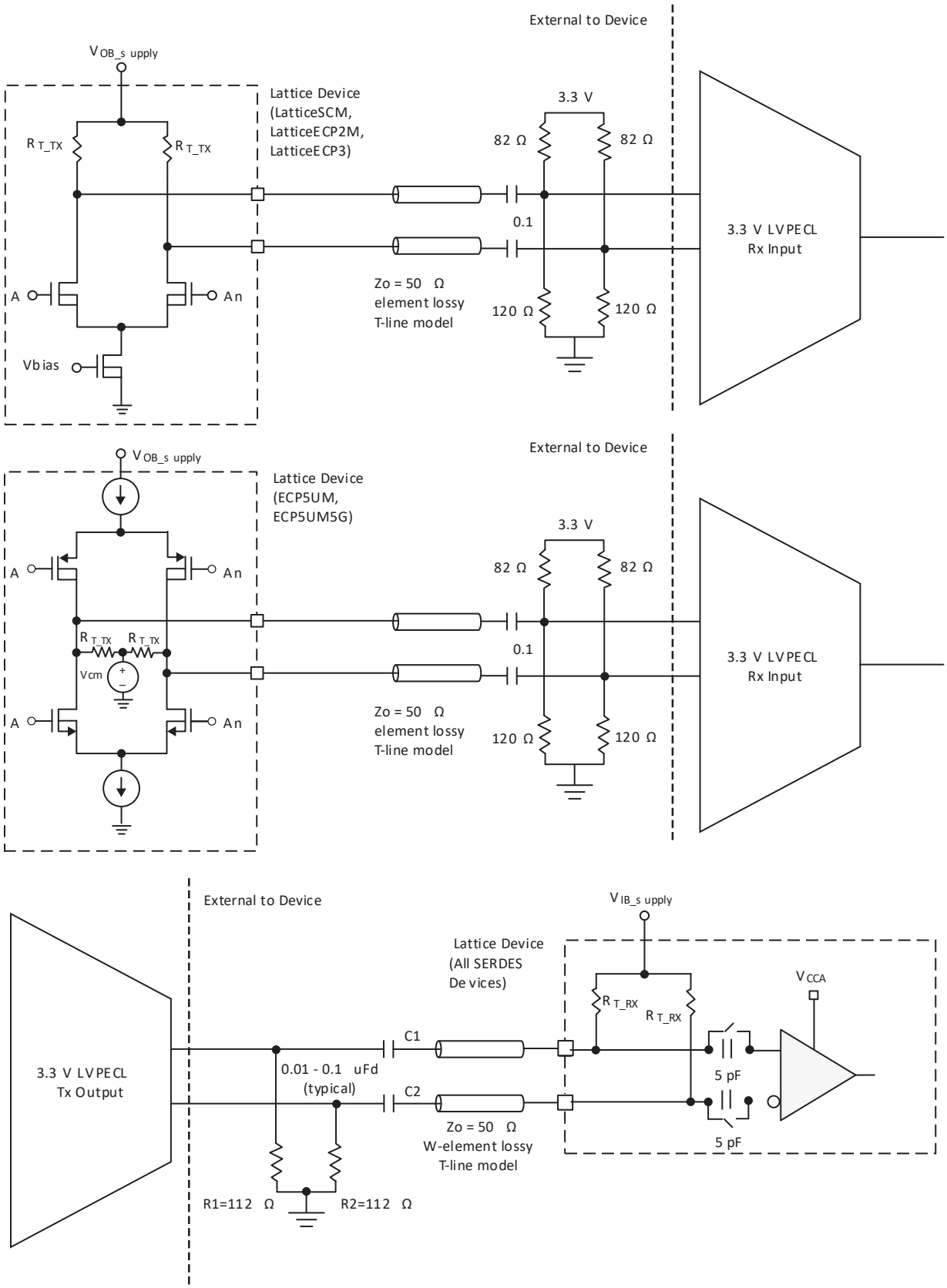


Figure 5.4. AC-Coupled to/from LVPECL Interface Diagram

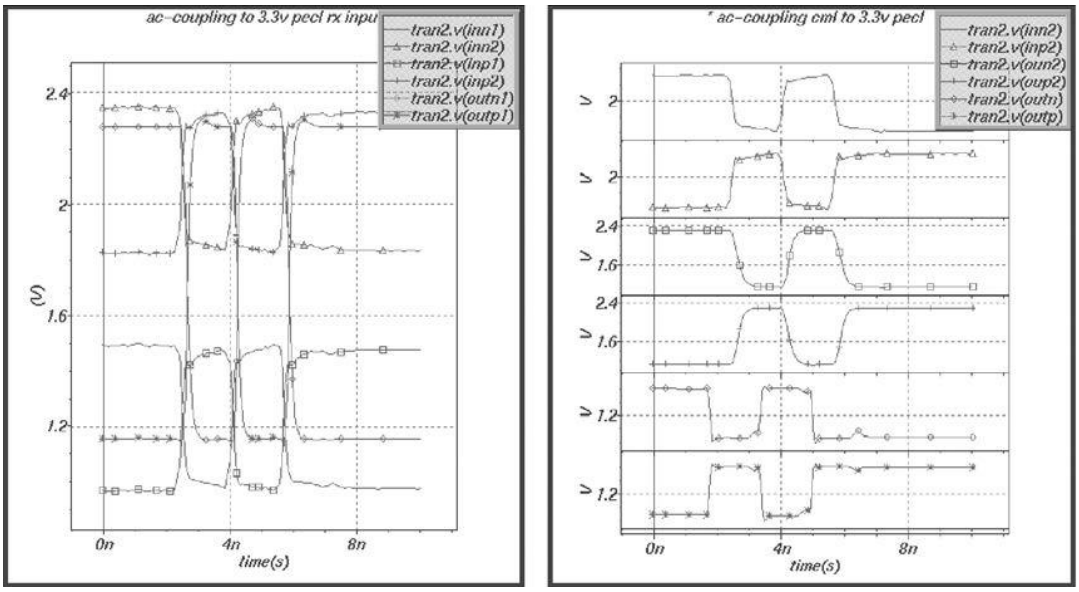


Figure 5.5. AC-Coupled CML to LVPECL Simulation

5.6. Interface to PCI Express Device

At the electrical level, PCI Express utilizes two uni-directional low voltage differential signaling (LVDS) pairs at 2.5 Gbps for each lane. Transmit and receive are separate differential pairs, for a total of four data wires per lane. The Lattice CML buffers interface well with LVDS, thus allowing interconnection to PCI Express buses. An input receiver with programmable equalization and output transmitters with programmable pre-emphasis permits optimization of the link. The PCI Express specification requires that the differential line must be common mode terminated at the receiving end. Each link requires a termination resistor at the far (receiver) end. The nominal resistor values used are 100 Ω. This is accomplished by using the embedded termination features of the CML inputs as shown in Figure 5.6. The specification requires AC coupling capacitors (CTX) on the transmit side of the link. This eliminates potential common-mode bias mismatches between transmit and receive devices. The capacitors must be added external to the Lattice CML outputs.

Table 5.4. Differential PCI Express Specifications

Symbol	Parameter	Min.	Nom.	Max.	Units	Comments	Location
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω	TX DC differential mode low impedance. ZTX-DIFF-DC is the small signal resistance of the transmitter measured at a DC operating point that is equivalent to that established by connecting a 100 Ω resistor from D+ and D- while the TX is driving a static logic one or logic zero.	Internal on chip
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω	RX DC differential mode impedance during all LTSSM states. When transmitting from a Fundamental Reset to Detect, (the initial state of the LTSSM), there is a 5 ms transition time before receiver termination values must be met on all un-configured lanes of a port.	Internal on chip
C_{TX}	AC Coupling Capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	External to Lattice device

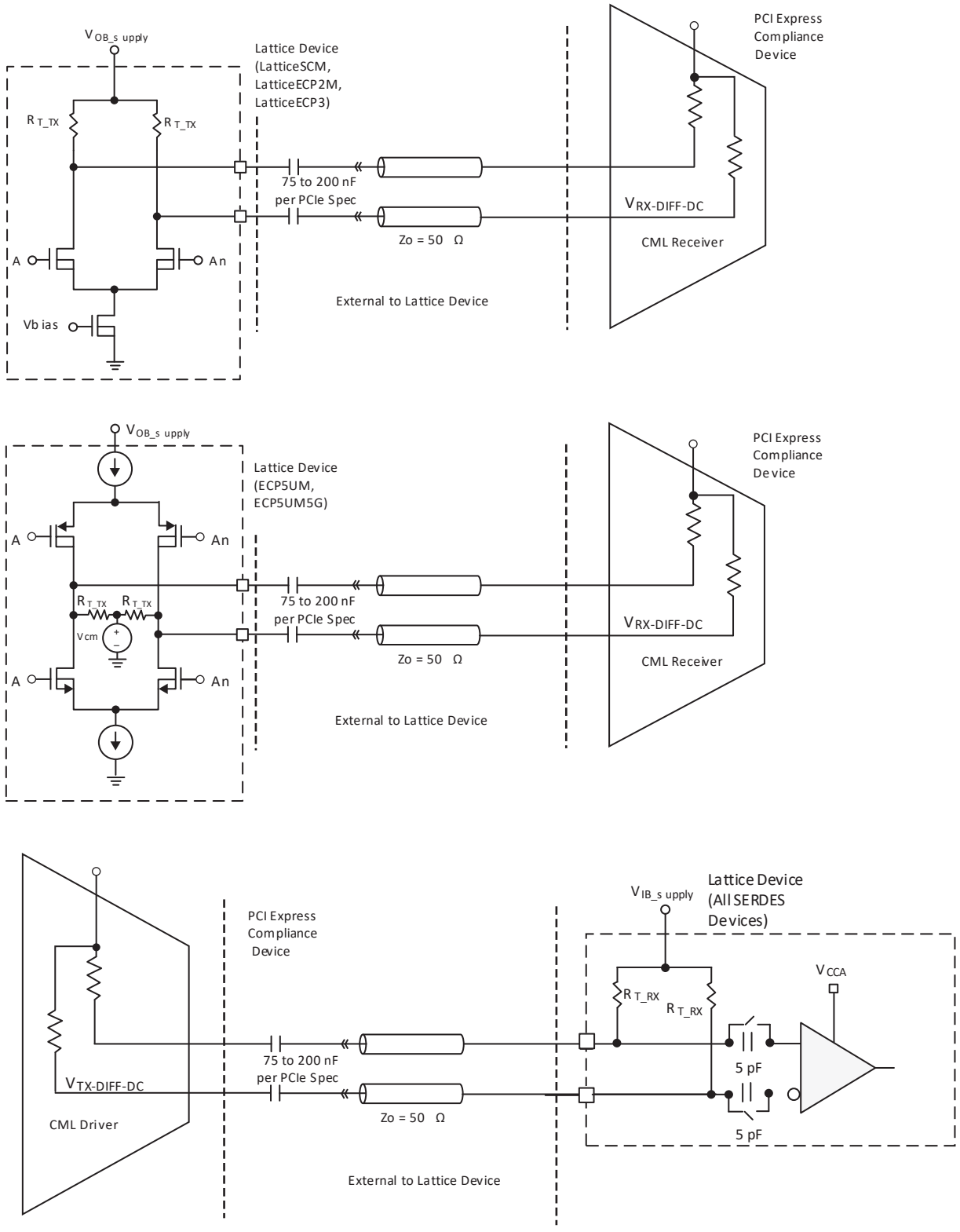


Figure 5.6. Connect to/from PCI Express Compliance Device Diagram

6. SERDES Reference Clock Interface

SERDES needs reference clock to create clocks to transmit and receive data. Reference clock is input to the TxPLL, and creates a high-speed bit clock for transmitter. Reference clock is also used to create bit clock at frequency close to the targeted data rate in the Clock Data Recovery (CDR) block, before the clock is used to sync and lock to the data at the received data rate.

There is one pair of differential reference clock pins in each block of SERDES. Each block of SERDES contains two or four channels of transceivers (Receive and Transmit channels), depending on device family. Refer to the individual product Data Sheet for details.

Each block of SERDES supports one TxPLL. Therefore, all transmit channels in the SERDES are sharing the high speed bitclock, or divided frequency of that bitclock. Some product families allow individual channels to share the high speed bitclock from a neighboring block of SERDES. Refer to the individual product SERDES Technical Note for information on the sharing and possible divider values.

Each block of SERDES also provides the option to select reference clock on the TxPLL, and each of individual CDR in the receive channel, from either the external reference clock pin, or routing the clock from the FPGA fabric. Although the option is available, it is strongly recommended not to use the fabric clock, especially on the TxPLL. When it is used, this clock must be routed on the primary clock tree, to ensure minimum jitter. Fabric switching noise often couples into clock signal, even when it is routed on primarily clock tree. This noise can be passed onto the high speed bitclock in TxPLL, causing the transmit data to be jittery, or if the jitter is high enough, causes the TxPLL not to clock.

Similarly, the routed clock with higher jitter can cause the CDR not to lock. Once the CDR can lock to the reference clock at the right frequency, it switches to lock to data, and the reference clock is not used for locking anymore (it is still used to detect CDR Loss of Lock).

All Lattice SERDES TxPLL cannot generate Spread Spectrum Clocking (SSC), but both the TxPLL and CDRs can tolerate SSC. The range of SSC supported is 30 kHz to 33 kHz spreading frequency, at 0% to –0.5% spreading.

When using SSC clock, the whole system is usually spreading together. Therefore, the clock is normally generated from one clock source with spreading capability, and distribute the clock to all other devices. There are some applications where the SERDES reference clock is created locally without SSC enabled, but the system has SSC enabled (transmitting data with SSC). When the SERDES-based FPGA is using this reference clock in the fabric to process the data, there is frequency difference between the received data, and the core logic. This needs to be buffered with FIFO that can accommodate the size of the packet in the user design.

Reference clock input buffers are different in various SERDES-based device families. Figure 6.1 to Figure 6.3 show the simplified block diagrams of the input buffers.

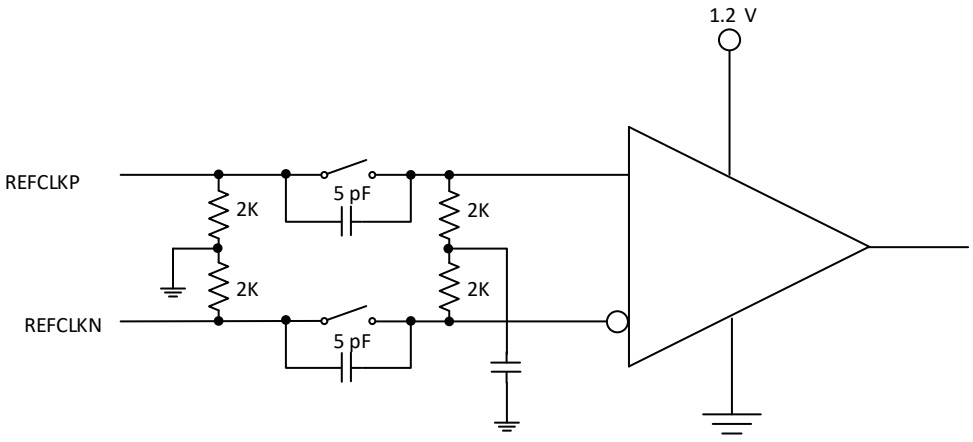


Figure 6.1. Differential Reference Clock Input Buffer for LatticeSCM Devices

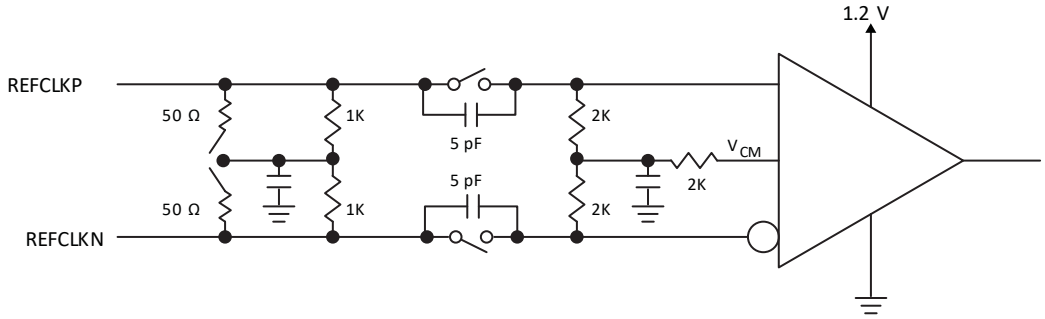


Figure 6.2. Differential Reference Clock Input Buffer for LatticeECP2M and LatticeECP3 Devices

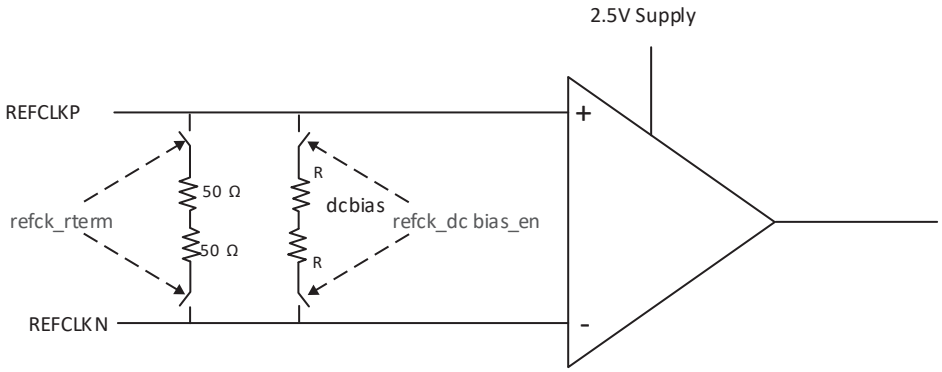


Figure 6.3. Differential Reference Clock Input Buffer for ECP5UM and ECP5UM5G

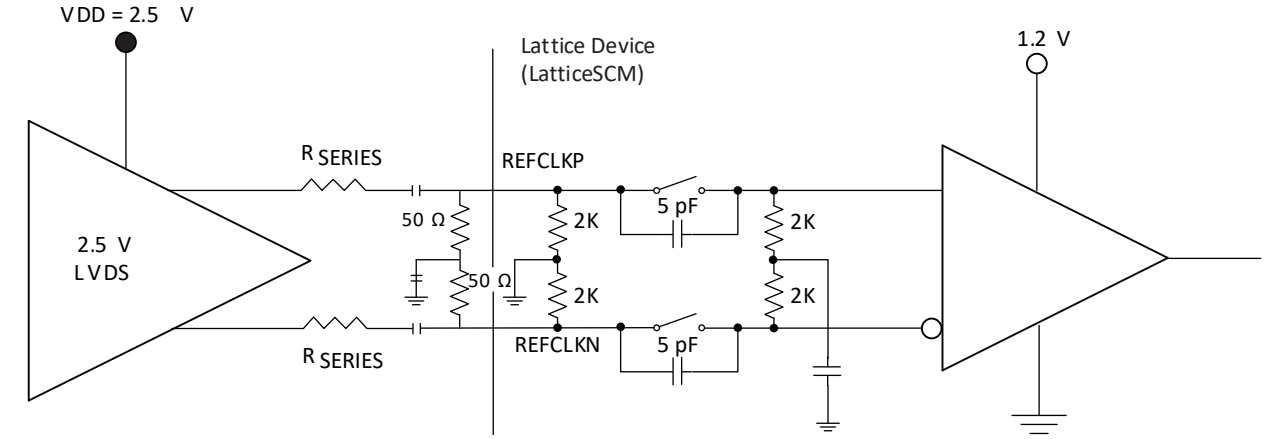
The following lists the differences between the product families:

- LatticeSCM, LatticeECP2M, LatticeECP3 families power the input differential buffer by V_{CCA} (1.2 V). ECP5UM and ECP5UM5G families are powered by V_{CCAUX1} (2.5 V).
  - The input electrical requirements vary due to the difference in power supply voltage. Refer to the respective product Data Sheets for details.
  - ECP5UM and ECPC5UM5G families do not support internal AC coupling capacitors.
  - The LatticeSCM does not have termination resistor on the input (only with higher impedance resistors to GND). The LatticeECP2M, LatticeECP3, ECP5UM, and ECP5UM5G all provide selectable 100 Ω differential termination between the P and N input pins.
  - When external AC coupling capacitors are used, DC bias on the pins can be supplied by internally generated Vcm on ECP5UM and ECP5UM5G families, or may be externally generated. For LatticeSCM, LatticeECP2M and LatticeECP3 families, Vcm can be supplied internally if internal AC coupling is disabled. Otherwise, it needs to be supplied externally.
  - There are special considerations when using LatticeSCM devices available in the 900-BGA wire-bonded package. The electrical performance of the input path to the reference clock input may show undesired qualities when observed by probing the device pins. These signal imperfections are imposed due to parasitic of the clock path that are intrinsic to the 900-ball fpBGA package. These reflections do not manifest inside the input buffer of the reference clock itself. HSPICE models are available for user evaluation and verification.

Most clock drivers used are based on LVDS or LVPECL standards. Because different reference clock input buffers are different in different SERDES-based product families, special considerations are being given for each of these interfaces.

6.1. Interface SERDES Reference Clock Input Buffer with LVDS Clock Driver

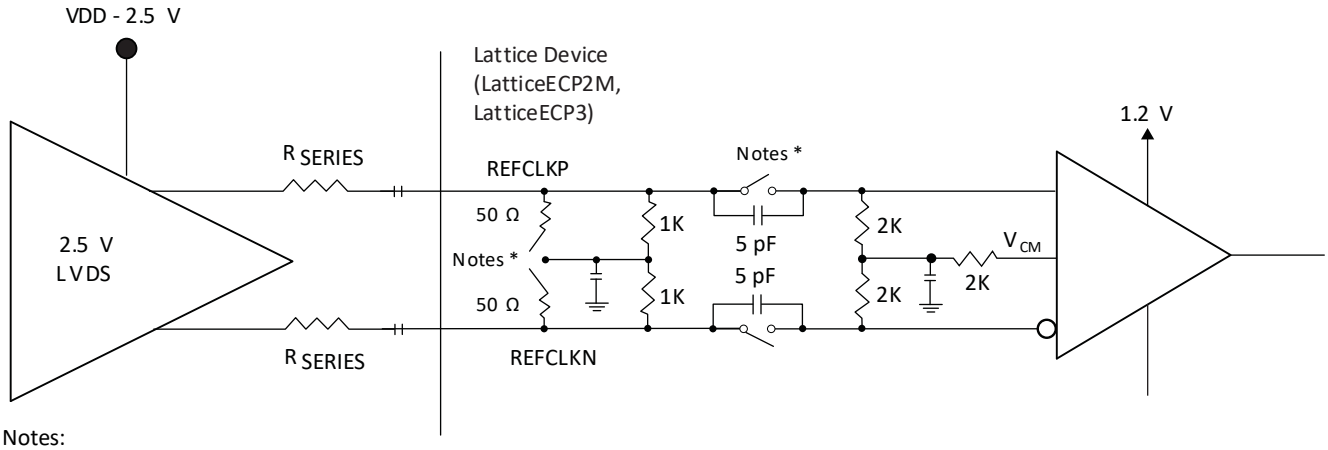
Figure 6.10 shows the interface between LVDS Clock Driver and the LatticeSCM Reference Clock Input buffer. Due to the low voltage input levels supported in LatticeSCM devices, the LVDS signal needs to be level shifted. Figure 6.4 shows level shift with external AC coupling, along with the differential termination that is required.



Notes:
- External AC coupling capacitors are required to level shift LVDS to LatticeSCM input levels.
- External 100 Ω differential termination is required, with center-tap highZ.
- RSERIES value may vary depending on driver characteristics.

Figure 6.4. LVDS Clock Driver to LatticeSCM RefClk Input Buffer

Figure 6.5 shows the interface between LVDS Clock Driver and the LatticeECP2M and LatticeECP3 Reference Clock Input buffer. Similar to LatticeSCM device, the LVDS signal needs to be level shifted. Because the internal 100 Ω differential termination does not provide DC bias voltage when internal AC coupling capacitors are used, it is required to bypass the internal AC coupling capacitor to provide that DC bias voltage.



Notes:
- External AC coupling capacitors are required to level shift LVDS to LatticeECP2M/LatticeECP3 input levels.
- External AC coupling capacitors should be bypassed, providing DC bias from VCM to the input pins.
- Internal differential 100 Ω termination should be enabled.
- RSERIES value may vary depending on driver characteristics.

Figure 6.5. LVDS Clock Driver to LatticeECP2M/ECP3 RefClk Input Buffer

Figure 6.6 shows the simplest interface between LVDS Clock Driver and the ECP5UM and ECP5UM5G Reference Clock Input buffer. Because the input electrical levels on the input buffer are compatible with LVDS25 signal levels, directly connecting between the devices is possible.

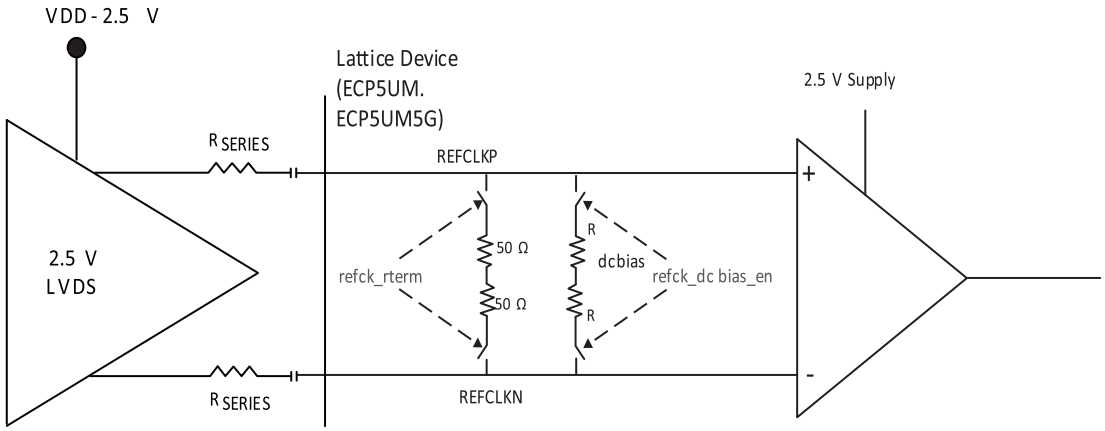
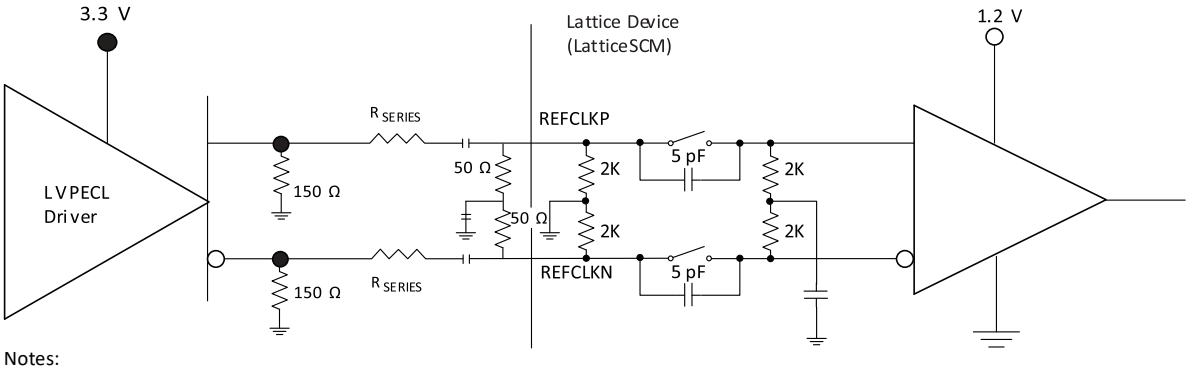


Figure 6.6. LVDS Clock Driver to ECP5UM and ECP5UM5G RefClk Input Buffer

6.2. Interface SERDES Reference Clock Input Buffer with LVPECL Clock Driver

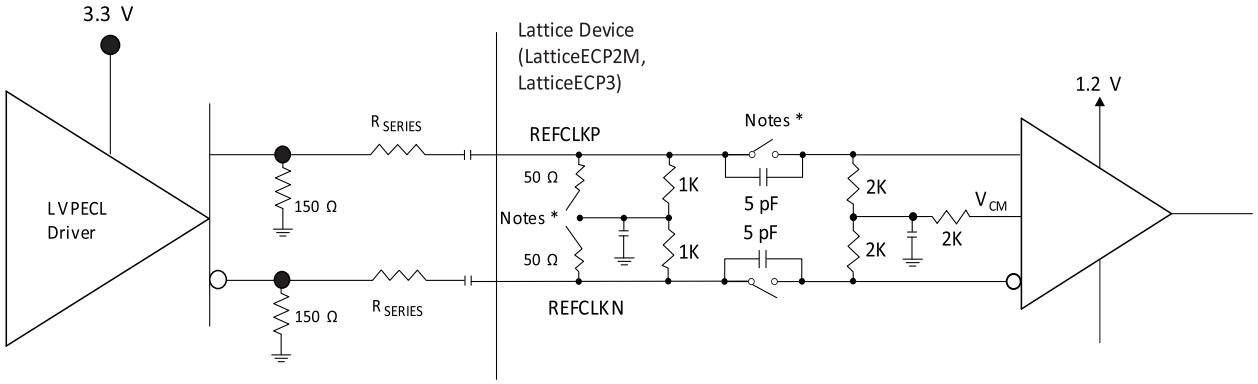
Same as interfacing to LVDS Clock Driver, LatticeSCM, LatticeECP2M and LatticeECP3 require level shift the LVPECL signal to meet the input electrical spec. Figure 6.7 and Figure 6.8 show the LVPECL connections.

For ECP5UM and ECP5G, similar external AC coupling capacitors are needed to level shift to the input electrical levels. Figure 6.9 shows the ECP5UM and ECP5UM5G connection.



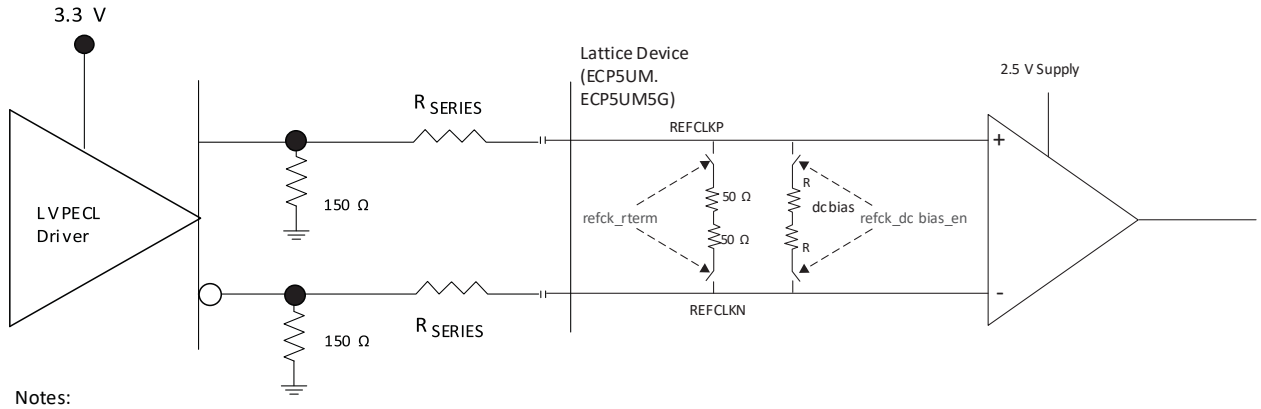
Notes:
- External AC coupling capacitors are required to level shift LVDS to LatticeSCM input levels.
- External 100 Ω differential termination is required, with center-tap highZ.
- RSERIES value may vary depending on driver characteristics.

Figure 6.7. LVPECL Clock Driver to LatticeSCM RefClk Input Buffer



Notes:
- External AC coupling capacitors are required to level shift LVPECL to LatticeECP2/LatticeECP3 input levels.
- Internal 100 Ω termination should be enabled. Internal rfclk_dcbias_en should be enabled.
- RSERIES value may vary dependng on driver characteristics.

Figure 6.8. LVPECL Clock Driver to LatticeECP2M/LatticeECP3 RefClk Input Buffer



Notes:
- External AC coupling capacitors are required to level shift LVPECL to ECP5UM/ECP5UM5G input levels.
- Internal 100 Ω termination should be enabled. Internal rfclk_dcbias_en should be enabled.
- RSERIES value may vary depending on driver characteristics.

Figure 6.9. LVPECL Clock Driver to ECP5UM and ECP5UM5G RefClk Input Buffer

With internal AC coupling capacitor enabled in LatticeSCM, LatticeECP2M, and LatticeECP3 devices, it is possible to connect LVPECL with single ended connection. This is done with resistor divider biasing the DC level of the inputs to the 1.2 V, and using external AC coupling capacitor on the input pins. The input buffers are set to be in DC coupling mode. These are shown in Figure 6.10 and Figure 6.11.

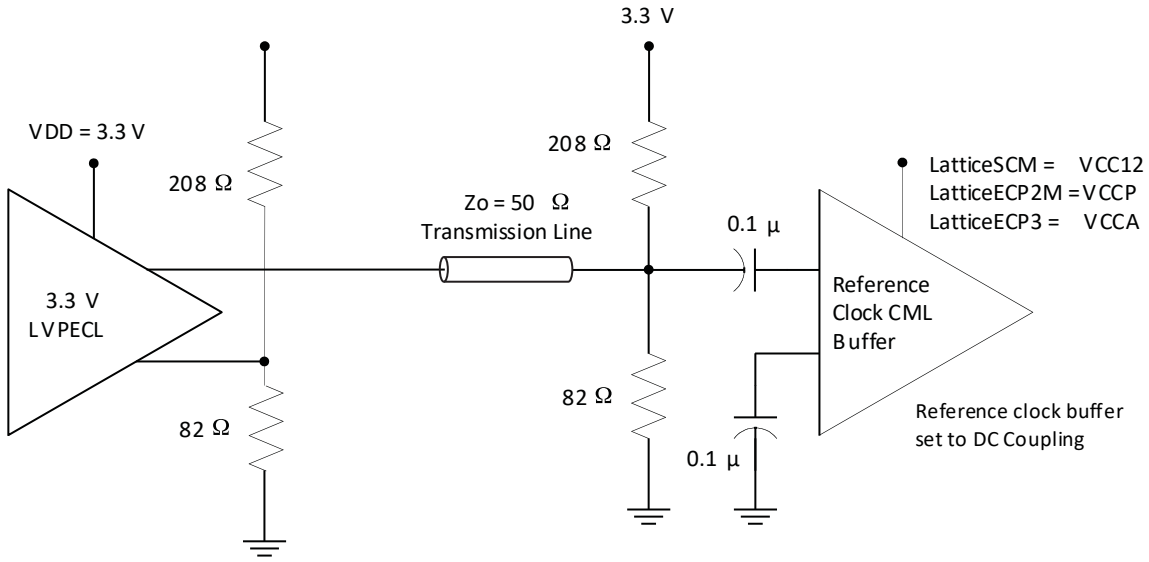


Figure 6.10. Single-Ended LVPECL Driving CML Reference Clock Buffer (AC, Receiver End Termination)

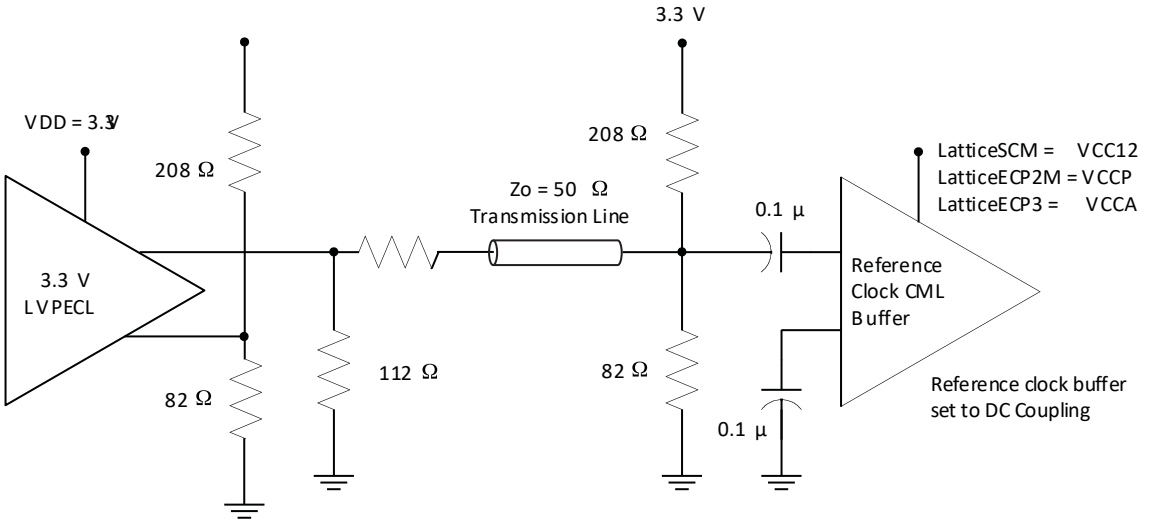


Figure 6.11. Single-Ended LVPECL Driving CML Reference Clock Buffer (AC, Source End Termination)

Simulation Usage Details

Analog simulation of interface circuits is a very useful part of the design process. Simple interfaces can be simulated using HSPICE models for the CML buffers available from Lattice. Two 50 Ω ideal transmission lines of matched length can be provided between the SERDES and the interconnected device, representing PCB traces. As shown throughout this document, a random 622 Mbps digital signal pattern was used in the simulation to drive the SERDES buffer and the resulting signal voltage waveforms can be predicted by simulation. Device package parasitic-elements can be included. Other parameters and conditions assumed were nominal IC processing parameters, nominal supply voltage and room temperature

Conclusion

This document discusses the general termination and interface interconnections of Lattice SERDES devices. The use of Current Mode Logic (CML) input and output buffer structures and their capabilities to interface with other CML and non-CML devices was also discussed. Lattice SERDES devices offer a variety of input and output terminations that offer a reduction in external components.

Appendix A. LatticeSCM Devices

An external calibration resistor is connected between the RESP pin and RESPN or between the RESP pins and board ground for packages not offering the dedicated RESPN pin. Each upper corner requires this resistor, so a maximum of two resistors are required per device. The value of the external resistor, 4.02 KΩ is an industry standard “EIA E96 series” value for 1% resistors. The circuitry also requires core VCC to be present and generates the VBIAS shown in Figure A.1.

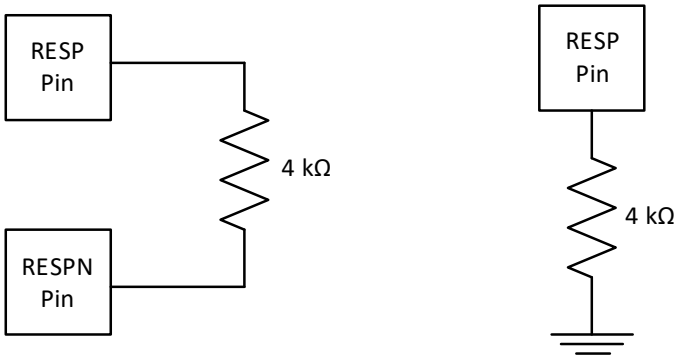


Figure A.1. RESP Connection

References

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- LatticeECP2M SERDES/PCS Usage Guide (FPGA-TN-02254)
- LatticeECP3 SERDES/PCS Usage Guide (FPGA-TN-02190)
- LatticeECP2/M Pin Assignment Recommendations (TN1159)
- LatticeECP3 Hardware Checklist (FPGA-TN-02183)
- Lattice Diamond FPGA design software
- Lattice Diamond Software User Guide
- Lattice Insights for Lattice Semiconductor training courses and learning plans

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, please refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 3.3, December 2025

Section	Change Summary
All	Minor editorial fixes.
SERDES Input/Output External Interfaces	Updated the 2nd bullet from *External 100 Ω termination should be enabled* to *Internal 100 Ω termination should be enabled* of Figure 6.8. LVPECL Clock Driver to LatticeECP2M/LatticeECP3 RefClk Input Buffer and Figure 6.9. LVPECL Clock Driver to ECP5UM and ECP5UM5G RefClk Input Buffer.

Revision 3.2, September 2024

Section	Change Summary
All	Minor editorial fixes
Abbreviations in This Document	Updated *Acronyms* to *Abbreviations*.
SERDES Input/Output Buffer Overview	Updated contents of subsection 2.1 SERDES Input/Output Buffer Power Supplies.
General FPGA Recommendations	Rephrased section content, *There is internal filter on the internal core supply voltage to ensure the digital switching noise is not coupled into the PLL function* to *There is an internal filter between the core supply and internal PLL supply to ensure digital switching noise is not coupled into the PLL*.
PCB Design Considerations	Rephrased introduction section content, *Many PCB designs include adjacent structures that can create cross-coupling of the FPGA I/O to the analog supply pins. The crosstalk created by via-to-via coupling can cause noise to attack the analog supplies. The noise aggressor is the culprit SSO pin potentially impacting the supplies and circumventing any provided PCB supply filtering. This coupled noise on the PCB from the aggressor can cause the SerDes performance to degrade dramatically. Enabling amplitude boost mode of the SerDes typically improves noise immunity for both the Rx and Tx portions of the SerDes, especially noted at rates above 2.7 Gbps* to *Many PCB designs can create cross-coupling of the FPGA I/O to the analog supply pins by via-to-via coupling. This coupled noise on the PCB can cause the SerDes performance to degrade dramatically. Enabling amplitude boost mode of the SerDes typically improves noise immunity for both the Rx and Tx portions of the SerDes, especially noted at rates above 2.7 Gbps*.

SERDES Input/Output External Interfaces	• Updated contents of subsection 5.2 External AC Coupling.
	• Updated Table 5.1. Off-chip AC Coupling Capacitor.
	  • Changed the PCI Express Min value from *75* to *100 (Gen 1 & 2)*.
	  • Changes the PCI Express Max value from *200* to *220 (Gen 3+)*.

Appendix A	Added this section.
References	Updated this section.
Technical Support Assistance	Added reference to the Lattice Answer Database on the Lattice website.

Revision 3.1, May 2021

Section	Change Summary
All	Changed SERDES to SerDes across the document.
Acronyms in This Document	Added this section.
Disclaimers	Added this section.
SerDes Input/Output Buffer Overview	Updated Figure 2.7 and Figure 2.8.

Revision 3.0, March 2018

Section	Change Summary
All	Changed document number from TN1114 to FPGA-TN-02077.
Introduction	Added paragraph to Introduction section.
SerDes Input/Output Buffer Overview	Revised section heading to SerDes Input/Output Buffer Overview. • General update was applied to this section. • Added Figure 2.2, Figure 2.7, and Figure 2.8. • Replaced Table 2.1.
General FPGA Recommendations	Updated General FPGA Recommendations. Changed device to Lattice SCM in Table 3.1.
PCB Design Considerations	Updated PCB Design Considerations. • Updated Table 4.1. • Updated Figure 4.1 caption. • Changed sub-heading to Special Considerations to Reduce Tx Jitter and Increase Jitter Tolerance for the LatticeSCM and added context information to this section.
SerDes Input/Output External Interfaces	Updated section heading to SerDes Input/Output External Interfaces. • Changed sub-headings to External DC Coupling, External AC Coupling and revised contents in these sections. • Added Internal AC Coupling section. • Changed sub-heading to Interface to LVDS Device. • Changed diagrams to Figure 5.1 and Figure 5.3. • Changed sub-heading to Interface to LVPECL Device. • Changed diagram to Figure 5.4. • Changed sub-heading to Interface to PCI Express Device. • Changed diagram to Figure 5.6.
SerDes Reference Clock Interface	Revised section heading to SerDes Reference Clock Interface. • General update was applied to this section. • Updated Figure 6.1 and Figure 6.2 captions. • Added Figure 6.3. • Provided list of differences between the product families. • Added Interface SerDes Reference Clock Input Buffer with LVDS Clock Driver section. • Added Figure 6.4, Figure 6.5, and Figure 6.6. • Added Interface SerDes Reference Clock Input Buffer with LVPECL Clock Driver section. • Added Figure 6.7, Figure 6.8, and Figure 6.9. • Updated Figure 6.10 and Figure 6.11.
References	Updated References information.
Technical Support Assistance	Updated Technical Support Assistance information.
Disclaimers	Added this section.

Revision 2.9, March 2014

Section	Change Summary
SerDes Input/Output External Interfaces	• Updated information in External DC Coupling and External AC Coupling sections. Updated Table 5.1, Off-Chip AC Coupling Capacitor. • Updated information in Interface to LVPECL Device External AC Coupling section. Updated typical LVPECL description. • Removed the DC-Coupled LVPECL to CML Interface Diagram and the Single-Ended PECL Driving CML Reference Clock Buffer (DC) figures.
SerDes Reference Clock Interface	• Updated the SerDes Reference Clock Interface section introduction. • Added footnote 5 to Figure 6.3, Reference Clock Buffer with External AC Coupling – LVPECL Clock Driver.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 2.8, September 2012

Section	Change Summary
All	Added power supply (VCCIB/OB) recommendation for RX only or Tx only usage.

Revision 2.7, August 2012

Section	Change Summary
All	Updated document with new corporate logo.
SerDes Reference Clock Interface	Updated Reference Clock Buffer with External AC Coupling diagram.

Revision 2.6, June 2011

Section	Change Summary
SerDes Reference Clock Interface	Updated Reference Clock Buffer with Internal DC Coupling figure.
SerDes Input/Output External Interfaces	Removed DC coupling figure (CML to LVPECL).

Revision 2.5, February 2010

Section	Change Summary
All	Updates to power supply diagrams and LVPECL termination scheme.

Revision 2.4, November 2009

Section	Change Summary
SerDes Reference Clock Interface	Added REFCLK DC coupling recommendation.

Revision 2.3, November 2009

Section	Change Summary
SerDes Reference Clock Interface	• Updated Reference Clock Buffer with Internal DC Coupling diagram. • Updated Reference Clock Buffer with Internal AC Coupling diagram.

Revision 2.2, April 2009

Section	Change Summary
All	Updated CML Reference Clock Input Buffer For LatticeECP2M and LatticeECP3 Devices diagram.

Revision 2.1, February 2009

Section	Change Summary
All	Added support for LatticeECP3 FPGA family.

Revision 2.0, December 2008

Section	Change Summary
All	LatticeECP2M VCOM typical range updated.

Revision 1.9, November 2008

Section	Change Summary
SerDes Input/Output Buffer Overview	Added a note to Passive Filter Network “Quiet Supply” Example figure.
All	Added new figures showing CML Ref Clock Input Buffers for LatticeSCM and LatticeECP2M.

Revision 1.8, August 2008

Section	Change Summary
All	LatticeECP2/M parameter names and values are corrected per data sheet.

Revision 1.7, June 2008

Section	Change Summary
PCB Design Considerations	• Added footnote to LatticeSCM PCB Aggressor I/O Pins table. • Added a reference to TN1159 for LatticeECP2/M pin assignment information.
SerDes Input/Output External Interfaces	Updated Differential LVPECL Driving CML Reference Clock Buffer (DC) figure and added a new figure after that (Figure 5.4 to illustrate CML buffers).

Revision 1.6, January 2008

Section	Change Summary
SerDes Input/Output External Interfaces	Updated PCI Express Device Interface section.

Revision 1.5, January 2008

Section	Change Summary
SerDes Reference Clock Interface	Updated Interfacing to Reference Clock CML Buffers section.

Revision 1.4, July 2007

Section	Change Summary
SerDes Reference Clock Interface	Updated Interfacing to Reference Clock CML Buffers section.

Revision 1.3, June 2007

Section	Change Summary
SerDes Input/Output Buffer Overview	Added footnote 1 to LatticeSC and LatticeECP2M SerDes Power Supplies table.

Revision 1.2, April 2007

Section	Change Summary
PCB Design Considerations	Added additional recommendations for PCB layout for LatticeSC.
SerDes Input/Output External Interfaces	PCI Express Application Termination figure updated.

Revision 1.1, December 2006

Section	Change Summary
SerDes Input/Output Buffer Overview	Added discussion about Switching Voltage Regulators and Linear Voltage Regulators text section.

Revision 1.0, July 2006

Section	Change Summary
All	Initial release.

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