# LatticeSC™ High-Speed Backplane Measurements

June 2006 Technical Note TN1118

## Introduction

The LatticeSC device contains multiple SerDes blocks arranged as quads. Each SerDes (SERializer/DESerializer) provides a serial high speed backplane transceiver interface and is capable of 3.8 GB/s performance.

This document illustrates SERDES high-speed backplane capabilities, through a series of laboratory tests. The Tyco HM-Zd Backplane Evaluation system[1] was used extensively in these tests. Two different configuration experiments are described:

- Eye-Diagram Experiment I — Shows LatticeSC performance over a standard reference backplane.
- Data-Rate Experiment — Shows LatticeSC data rate limits measured for 48 inch FR4 path lengths.

Bit-error rate and eye-diagram measurements are used to evaluate link performance and margins. Error-free performance is observed through various backplane connections and over different operating conditions, for test intervals of several minutes. The effects and benefits of transmitter pre-emphasis and amplitude adjustment are illustrated. Finally, some general application recommendations are made for high-speed backplane interconnection design.

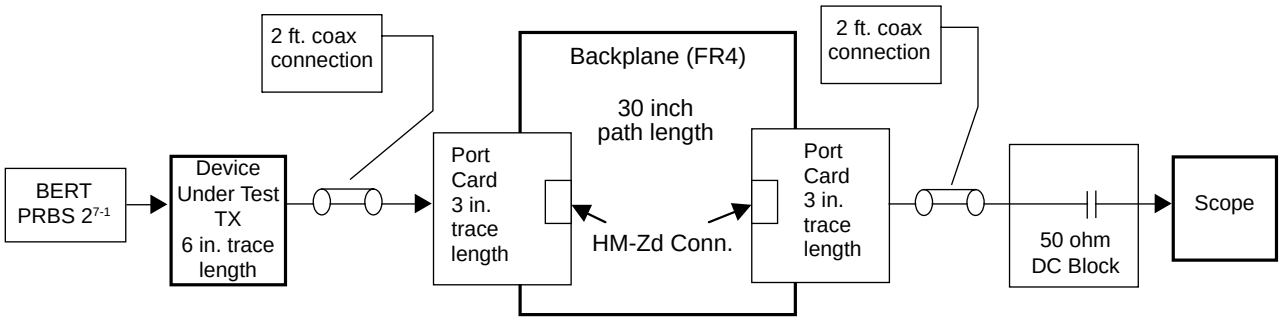
## Eye-Diagram Experiment I

Eye-diagram signal waveforms observed at the receive end of PCB interconnection paths were recorded. This measurement displays the effect of various system error contributions on received signal integrity. A series of such measurements made on a nominal device at 25ºC while driving through the Tyco test backplane[1] are described in this section.

### Test Equipment

– LatticeSC 900 Wirebond AC evaluation board
– Tyco Electronics XAUI backplane with two port cards[1]
– Agilent 81250 Parallel Bit Error Rate Tester
– Agilent E3648A power supplies
– Agilent 8133A clock source
– PicoSecond 5575A Bias-T
– Agilent 86100A DCA oscilloscope

***Figure 1. Eye-Diagram Test Setup***



## Test Setup

Figure 1 shows the test setup used to measure the data eye-openings discussed in this document. The TX signal comes directly from a high-speed serial output.

## LatticeSC Test Setup Parameters

– LatticeSC 900PBGAM plastic ball grid array (wire-bond)
– All power supplies set to Nominal Voltages
– Ambient Temperature = 25˚ C
– Data Pattern = PRBS 2^7-1
– Socketed Device
– Nominal Device

## PCB Specification

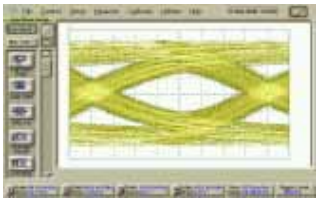
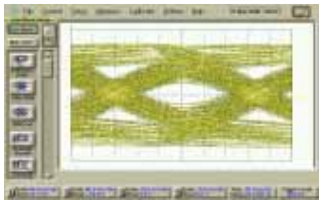
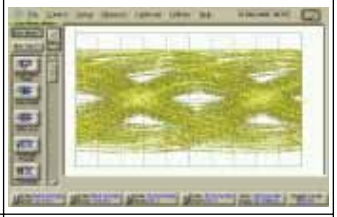
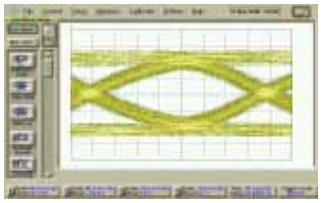
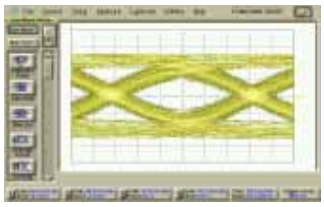
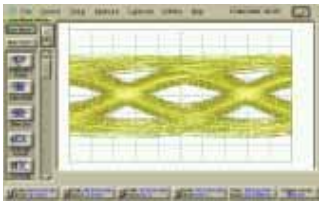
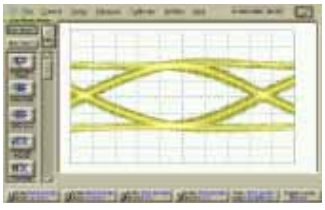
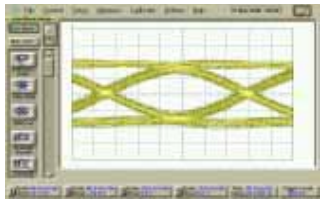
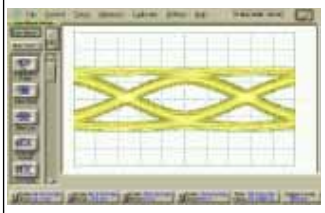
– The 3-inch PWB section (port card) is composed of 6 mil wide (1/2 oz. copper thickness) 100 Ohm differential impedance traces
– Backplane - 200 mils thick, 14 layers, Nelco 4000-6 FR4
– All signal layers are 10 mil wide (1/2 oz. copper thickness) traces designed for 100 Ohm differential impedance
– All signal layers buried and surrounded by GND planes
– Port Card - 93 mils thick, 14 layers, Nelco 4000-4 FR4
– Total trace length: 6” + 3” + 3” + 30” = 42 inches

## Typical Eye-diagram Measurements

A typical application might have a total PWB trace path length of 12 to 24 inches, between two interconnected devices. This section shows a series of eye-diagram measurements for a 42 inch path length. Receiver eye-diagram measurements can provide an excellent indication of expected link performance. Data rate and pre-emphasis levels were varied. Eye-opening time and amplitude are indicated below each waveform. All tests in this section were performed at room temperature and nominal supply voltage.

The LatticeSC high-speed outputs provide software programmed pre-emphasis parameters of 0% up to 48%. Pre-emphasis compensates for the high frequency losses that a typical physical interconnection system exhibits. Enabling pre-emphasis provides increased interconnection path length capability and/or increased eye-opening for a given path length. In general, pre-emphasis should only be enabled where needed, since there is a slight increase in power dissipation and EMC radiation associated with this feature.

***Figure 2. LatticeSC Differential Receiver Eye Patterns at 2.5, 3.125, and 3.8 GB/s Over a 42 inch Path Length***

| | **2.5 GB/s** | **3.125 GB/s** | **3.8 GB/s** |
|---|---|---|---|
| 16% Pre-emphasis (Default) |  |  |  |
| | 210 mV | 108 mV | 38 mV |
| 32% Pre-emphasis |  |  |  |
| | 260 mV | 153 mV | 90 mV |
| 48% Pre-emphasis |  |  |  |
| | 274 mV | 200 mV | 133 mV |

The eye opening amplitudes in Figure 2 can be compared to the 85 mV eye requirement specified in the LatticeSC data sheet. At data rates of 3.8 GB/s, where path losses are greater, 32% Pre-emphasis must be used to achieve a comfortable margin above the 85 mV required opening.

## Data-Rate Experiment

For the LatticeSC data rate experiment, BER testing was performed on multiple process varied Nominal and Corner devices across 30 inch backplane traces, at 0˚C and 105˚C Junction temperatures. The total PCB trace length for these tests was 48 inches, when port card and evaluation board traces are included. The test criterion used was the observation of 1E12 data bits received, using a PRBS 2^7-1 data pattern, with no bit-errors occurring. Detailed bit-error rate and jitter performance is beyond the scope of this application note. A detailed discussion of the LatticeSC jitter and error-rate performance can be found in Lattice Application Note TN1084.

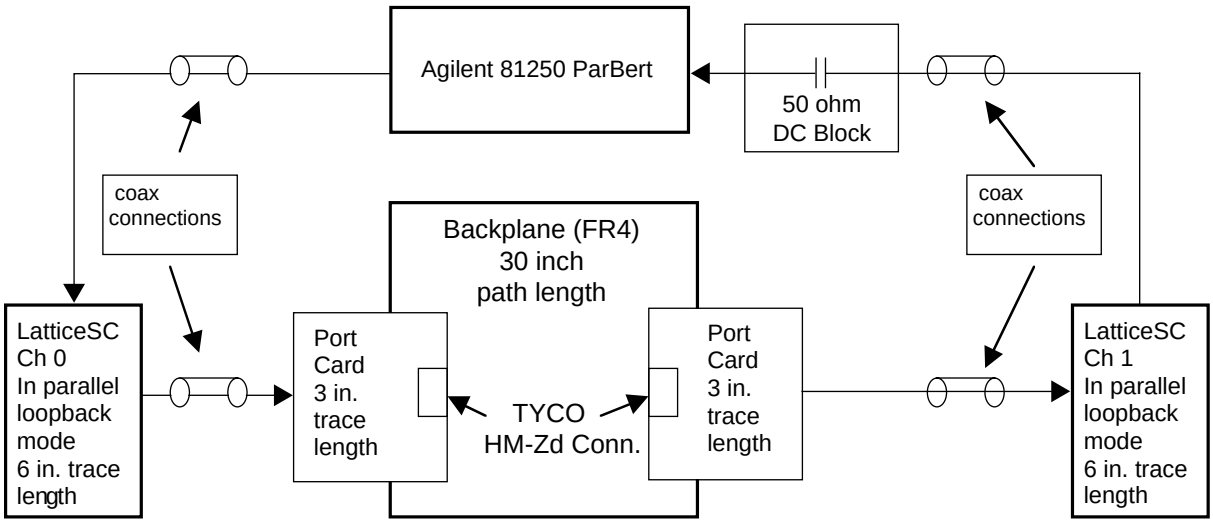
### Test Equipment

– LatticeSC 900 AC WB Evaluation Board
– Tyco Electronics XAUI backplane with two port cards[1]
– Agilent 81250 parallel Bit Error Rate Tester
– Agilent E3648A power supplies
– Agilent 8133A clock source
– Thermonics T-2500E thermostream
– PicoSecond 5575A Bias-T

### Test Setup

The test configuration used to verify error-free operation is shown in Figure 3. High-speed LatticeSC serial interface buffers are connected at both the TX and RX signal ends of the PCB signal path under test. Two separate SERDES channel in the LatticeSC devices were each placed in a parallel loopback mode of operation. The two unused channels were placed in a Near-End Serial Loop Back mode while running 2^7-1 data. The Agilent BERT was used to generate the data test pattern. Time matched 50 ohm coax cables used in the signal path were found to have minimal loss, as compared to PCB traces.

***Figure 3. Bit-Error Rate Test Setup***




### LatticeSCTest Setup Parameters

– LatticeSC 9000 PBGAM plastic ball grid array (wire-bond)
– Junction temperature = 0 to 105° C
– Data pattern = PRBS 2^7 - 1
– VDD12 Power Supplies = 1.14V to 1.26V
– Socketed Device
– Process Split Devices
– Pre-emphasis = 16%
– EQ = 6db

## PCB Specification

– The 3 inch PWB section (port card) is composed of 6 mil wide (1/2 oz. copper thickness) 100 Ohm differential impedance traces
– Backplane - 200 mils thick, 14 layers, Nelco 4000-6 FR4
– All signal layers are 10 mil wide (1/2 oz. copper thickness) traces designed for 100 Ohm differential impedance
– All signal layers buried and surrounded by GND planes
– Port Card - 93 mils thick, 14 layers, Nelco 4000-4 FR4

## Data Summary

Each device was tested over temperature and supply voltage variations. The maximum speed of operation was determined at each test condition. Results of the testing for the worst-case device are shown in Table 1.

***Table 1. LatticeSC Bit-Error Rate Test Results with 48 Inch PCB Connection***

| VCC12 | Pattern | Temp | Max. Speed |
|---|---|---|---|
| 1.26 | 2^7-1 | 0°C | 3.8 GB/s |
| 1.14 | 2^7-1 | 105°C | 3.7 GB/s |

Note: 6db equalization used on all tests.

Test criterion used for tests was 1E-12 maximum bit-error rate.

## Conclusion and Backplane Design Guidelines

The LatticeSC devices can support high-speed serial backplane interconnections over a broad range of data rates and connection path lengths. Measurement data presented in this document illustrates device performance over a typical backplane system, designed for high-speed serial interconnections. LatticeSC (per channel) programmable pre-emphasis levels allow applications to optimize each signal interface.

The effectiveness of using pre-emphasis to compensate for the high-frequency losses of longer path lengths was shown in Sections 1 and 2. Eye-diagram measurements were found to be a very good indication of backplane interconnection performance. The specified 85mV minimum eye-opening criterion for the LatticeSC was found to consistently predict error-free performance (less than 1E-12 error-rate) in all the measurements made.

High-speed interconnection performance in a system is dependent on many device, system and environment characteristics. For this reason it is not possible to specify performance limits that apply to all applications. Table 2 shows LatticeSC operating data rates for the slowest (process split) device over 48 inches of PCB under conditions specified in section 2.

***Table 2. LatticeSC Typical Frequency Limits with 48 inches of PCB***

| Device | Max Data Rate |
|---|---|
| LatticeSC-Process Split | 3.7 GB/s |

This table takes into account variations in device speed, temperature, and supply voltage. The data of Section 2 is consistent with this table, for a process split device, while operating over a 48 inch connection path, in the TYCO backplane test system. The maximum connection path length that an application can reliably use, is a complex system level question that the application designer must address.

The following suggestions are made, for LatticeSC applications, to help achieve best interconnection performance results:

- Careful selection of backplane connectors and other components touching the high-speed path, is critical. Each component should be electrically characterized through the frequency range of operation. Pay close attention to the parasitic reactance parameters of these components.
- Great care should be taken in the port card and backplane PCB design to follow good high-speed design practices. More detailed information is outlined in the Lattice Semiconductor High-Speed PCB Design Considerations TN 1033 technical note.
- For all backplane applications, use the 6db active EQ setting. The 12db active EQ setting has rarely been required to improve signal integrity for typical backplane applications.
- Use analog simulation tools extensively. Analog interconnection circuit simulation is a valuable tool at the system design level. SPICE models of interface and connection devices, which are available from most vendors, can be used to assess signal integrity issues, prior to building models. The LatticeSC HSPICE SerDes Design Kit includes includes system examples to help get you started.
- Early laboratory measurements of the longer and/or more critical interconnection paths should be made to reduce technical risk, prior to full system model design. Eye-diagram and bit-error rate measurements are recommended. LatticeSC SERDES I/O buffer HSPICE models are available.

## References

1. Tyco Electronics XAUI Z-Pack HM-Zd Backplane Evaluation Test System (this system was selected by 10GEC as the XAUI interoperability standard)High-Speed PCB Design Considerations, Lattice Technical Note TN1033
2. LatticeSC Data Sheets