Input Hysteresis in Lattice CPLD and FPGA Devices

September 2006 **Technical Note TN1112**

Introduction

In order to optimize speed in Lattice devices such as the ispMACH™ 4000 and MachXO™, device inputs are configurable with internal pull-up, pull-down, bus-hold latch or no bus maintenance. Typically, inputs can tolerate rise and fall times in the 50ns to 100ns range. When interfacing to slow input signals with input rise and fall time in hundreds of nanoseconds, external board design techniques are necessary to make the slow input signals immune to input noise that may be injected. This technical note suggests a few such techniques.

Input Circuit Techniques

Simple external circuitry along with the internal bus maintenance circuit can significantly improve slow rising and falling input noise immunity. Three common methods are described below.

Figure 1. Method 1: Input Series Resistor

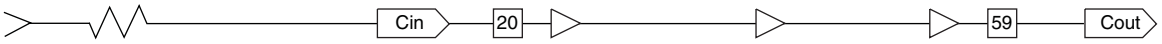


Figure 2. Method 2: Input and Feedback Resistor

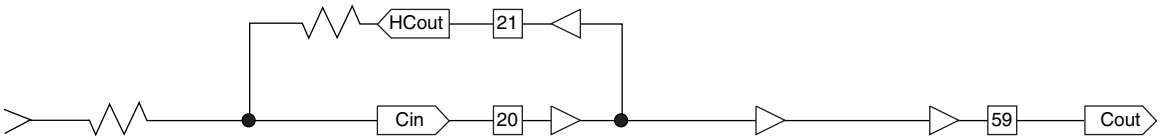
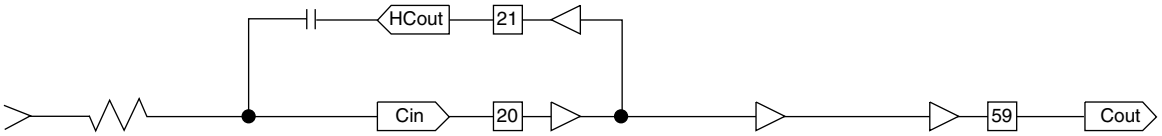


Figure 3. Method 3: Input Resistor and Feedback Capacitor



The following experimental data was collected to demonstrate the improvement that can be achieved with the different methods as compared to inputs without any external circuitry. The tables below highlight the maximum input rise (t_{RISE}) and fall (t_{FALL}) time of the results.

Test Device: MachXO
I/O Standard: LVCMOS 3.3V with input bus-hold latch turned on
Temperature: Room temperature

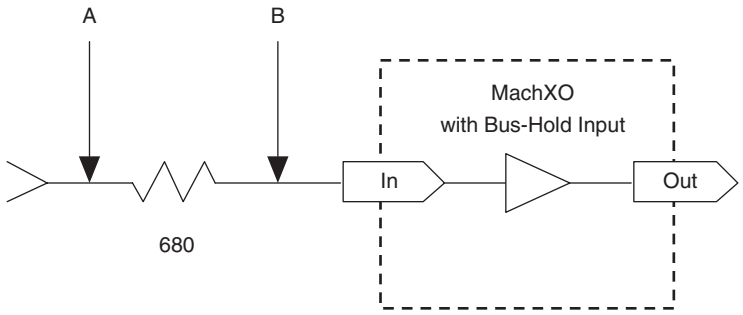
External Input Circuit	Input Series Resistor	t_{RISE}	t_{FALL}
None	—	<54ns	<56ns
Method 1	100Ω	65ns	63ns
	470Ω	500ns	470ns
	680Ω	>15ms	>15ms

Test Device: ispMACH 4128V
I/O Standard: LVCMOS 3.3V with input bus-hold latch turned on
Temperature: Room temperature

External Input Circuit	Input Series Resistor	Feedback Resistor or Capacitor	t_{RISE}	t_{FALL}
None	—	—	<100ns	<100ns
Method 1	100Ω	—	220ns	155ns
	1KΩ	—	2µs	1.5µs
	4.7KΩ	—	6µs	7µs
Method 2	100Ω	1KΩ	800ns	300ns
		560Ω	700ns	350ns
	1KΩ	10KΩ	5µs	1.9µs
Method 3	100Ω	33pF	700ns	350ns
		100pF	2µs	600ns
	1KΩ	33pF	5µs	1.5µs

The plots below are measured with MachXO. A 680Ω resistor is used in Method 1. The I/Os are configured as "bus-hold".

Figure 4. Test Setup



In the following figures, top trace represents outputs and bottom trace represents inputs. Persistence was set to 5 seconds for all waveforms.

Figure 5. Input Measured at Point A

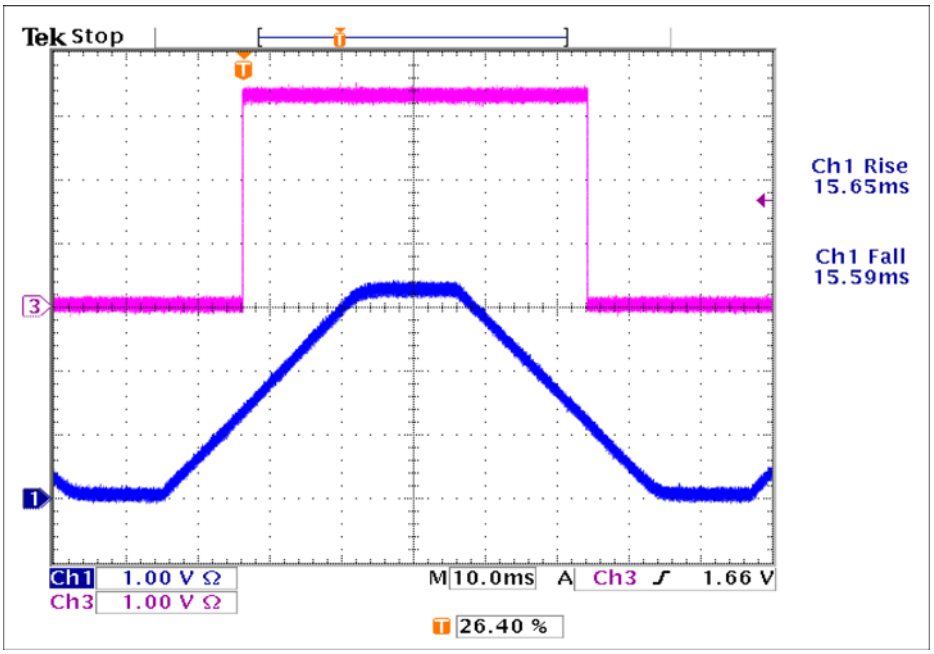
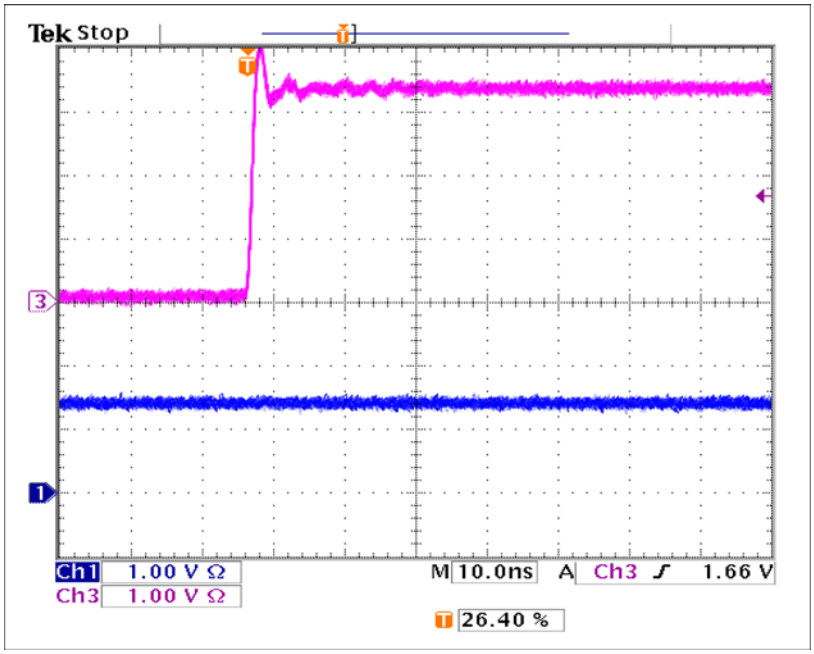


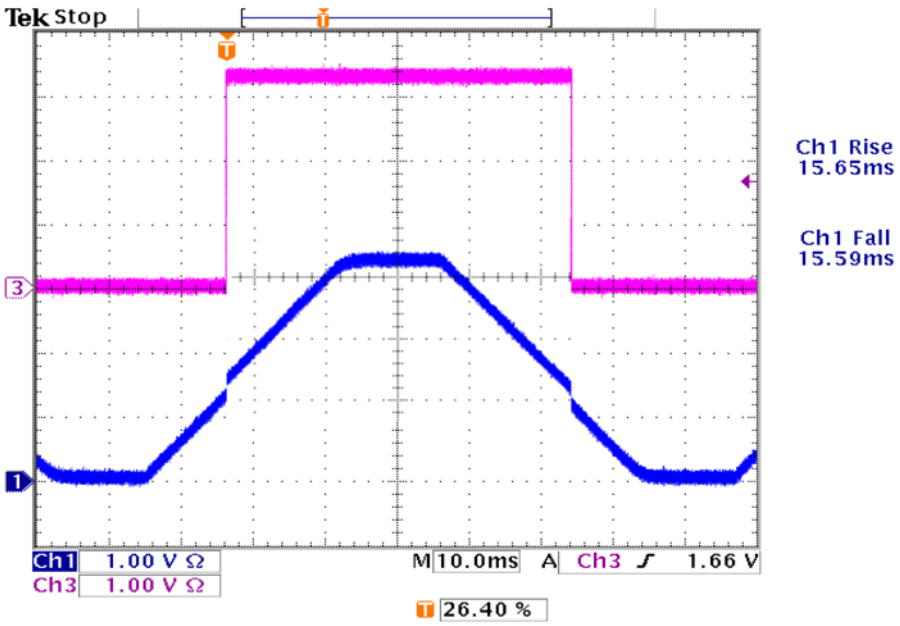
Figure 6. Zoomed View of Rising Edge of Figure 5



Input Hysteresis

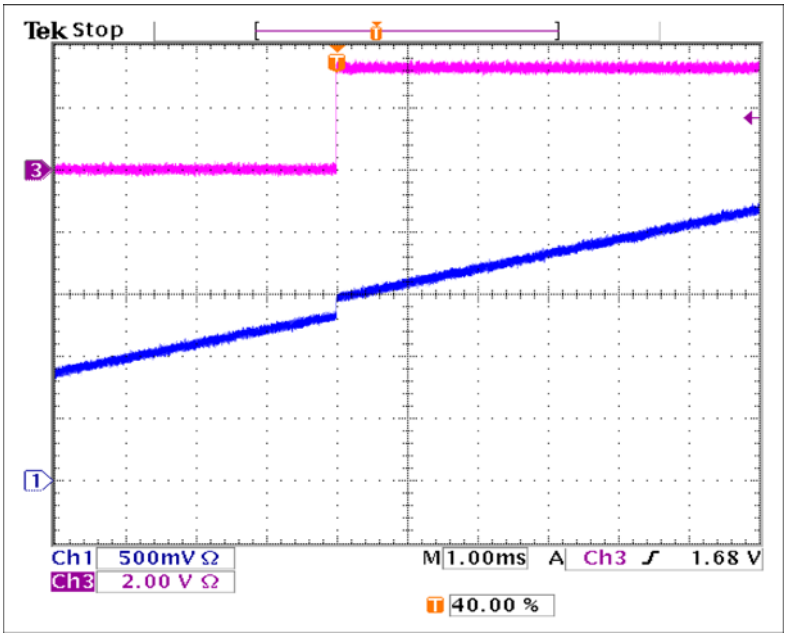
Figure 7 demonstrates the input signal with slow ramp rate virtually follow the ramp rate of MachXO output.

Figure 7. Input measured at Point B



Note “jump” at transition point.

Figure 8. Zoomed View of Rising Edge of Figure 7



Most digital circuitry is effectively linear in nature. The output normally swings from one extreme (VOL) to the other (VOH). At threshold level a smallest amount of noise will cause the output to swing widely from one extreme to the other.

With a fast slew rate input, the signal will stay around the threshold region for a short time. With a slower signal, which stays in the threshold region for a long time, the noise will have more time to reverse the signal direction.

Hysteresis is one common solution to this problem. Hysteresis means that the state of the output is not only dependent on the state of the input but, also, on the immediate past history of the input. A Schmitt trigger adds hysteresis to the input by creating different trip points for low-to-high and high-to-low transition. For the CPLDs and FPGAs that do not have the Schmitt trigger input, the bus-hold latch with an external resistor works in a similar manner.

The bus-hold input circuitry works by sinking a small amount of current when it's below the threshold and sourcing when it's above the threshold. This means that the input voltage tends to stay low when it's low and high when it's high. If all of the I/Os on a bus go high impedance, the bus will tend to stay in the same state until an output turns on.

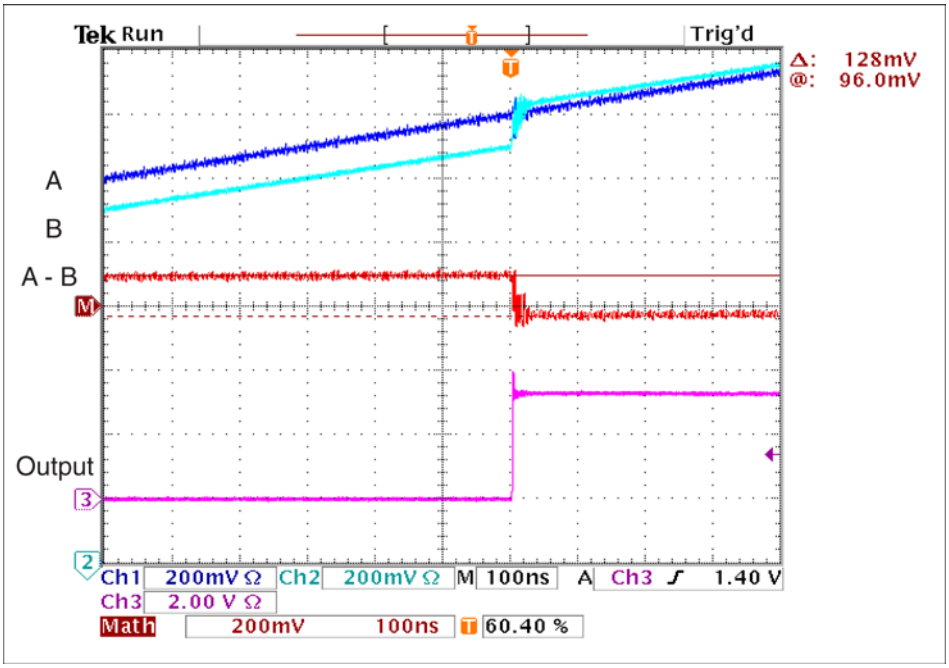
If a resistor is inserted in series with the input, the change in current will result in change in the voltage seen at the pin. This is what causes that jump. The optimum resistor value will cause enough ΔV to put the input well past the threshold region so that noise will not be able to cause unwanted switching, but will not be so large as to exacerbate the noise or slow the signal.

Refer to Figure 9 for discussion of the 'jump'.

The voltage jump is 128mV at the output (Ch3) transition point.

When the input is below the threshold, the voltage across the resistor is 96mV and -32mV after the transition. In other words, the input signal source must source 144µA (96mV/680Ω). When input A passes the threshold, the signal source sinks 47µA (-32mV/680Ω). At this point, any noise spike is unlikely to go back beyond the threshold.

Figure 9. Input Series Resistor and Hysteresis



Summary

As the data indicate, even with the very simple input series resistor used in Method 1 and the CPLD internal input bus-hold latch, maximum input rise and fall times will extend to hundreds of nanoseconds to microseconds.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
April 2006	01.0	Initial release.
September 2006	01.1	Waveforms updated. Detailed explanation added.