Introduction

This application note discusses the states of the Power Manager II ispPAC®-POWR1220AT8 device's output pins — Open drain logic outputs (OUT5-OUT20), HVOUT, and Trim DAC — during power-up, reset, and JTAG programming, as well as the states of these pins on a device that has not yet been programmed by the user. An understanding of this aspect of the device's operation is the key to designing systems that sequence supplies on in a dependable fashion. Suggested methods for interfacing to the enable pin of DC/DC converters and for performing in-system programming are also covered in this application note.

Power-on Reset

The ispPAC-POWR1220AT8 contains on-chip power-on reset circuitry to ensure that all parts of the device start up reliably, regardless of the speed at which the VCC supply to the device reaches 3.3V. The device enters power-on reset when VCC is approximately 0.8V. VCC must reach a voltage greater than 2.5V for the device to exit power-on reset. During power-on reset, the output pins will go to the states shown in Table 7-1. After the device exits power-on reset, any brownouts that cause the VCC supply to dip below 2.5V will cause another power-on reset event to occur.

Table 7-1. Output States During Power-On Reset

Output Type	Power-on Reset State
OUT5-OUT20	High Impedance
HVOUT, Charge Pump Mode (as-shipped)	Pull-down
HVOUT, Open Drain Logic Output Mode	High Impedance
Trim DAC	High Impedance

The ispPAC-POWR1220AT8 has a bi-directional reset pin (RESETb) whose main purpose is to synchronize the startup of multiple Power Manager devices. This pin can also be used to indicate when the device is in power-on reset. Figure 7-1 shows an equivalent circuit for this pin; it is an open-drain output with a built-in pullup resistance to VCCD. External pullup resistors to VCCD may be used but are not necessary. No capacitors should be connected to this pin because they will degrade the slew rate of the reset waveform. Unlike conventional active-low reset pins, RESETb should never be connected directly to the VCC supply.

Figures 7-2-7-5 illustrate the power-on reset behavior associated with logic outputs OUT5-20 and HVOUT pins that have been programmed to operate as open drain logic outputs. 2k Ohm pullup resistors to the VCCD pin were used on both the RESETb and logic output pins in all of the plots.

Figure 7-1. RESETb Pin Equivalent Circuit
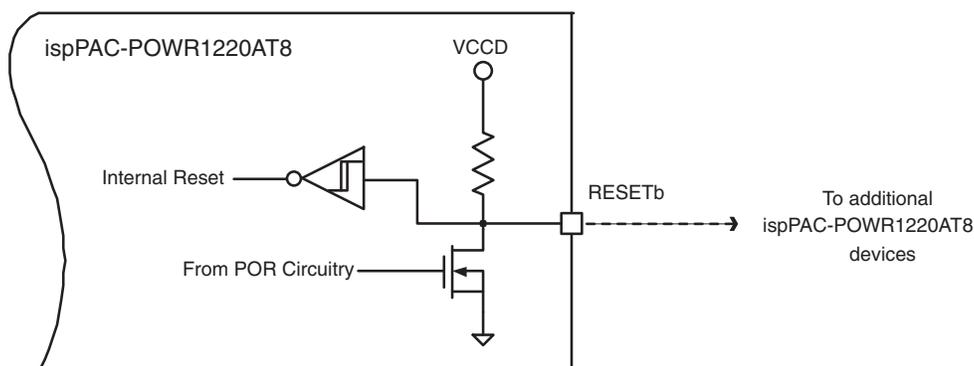
Figures 7-2 and 7-3 show an open drain logic output pin that has been programmed to behave as a registered output. The difference between these two plots is that in Figure 7-2, the output has been programmed to reset to a low level, whereas in Figure 7-3, it has been programmed to reset high. The power supply goes from zero to 3.3V in 20 milliseconds. The waveforms in Figures 7-2 and 7-3 are typical of VCC supplies that take more than a millisecond to reach 3.3V.

Figure 7-2. Startup with Slow Supply; Output Resets Low
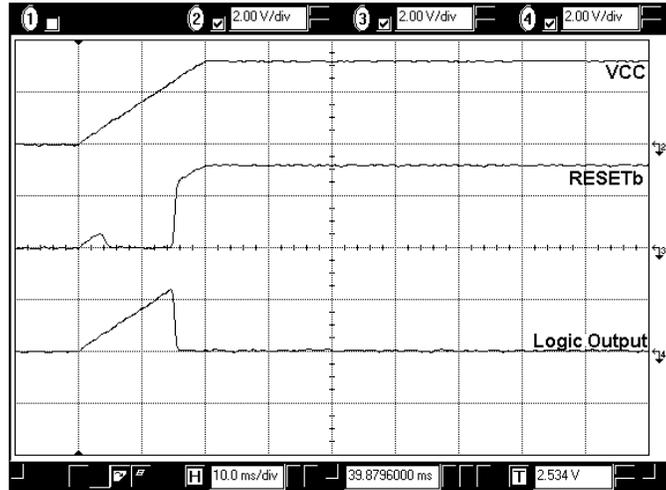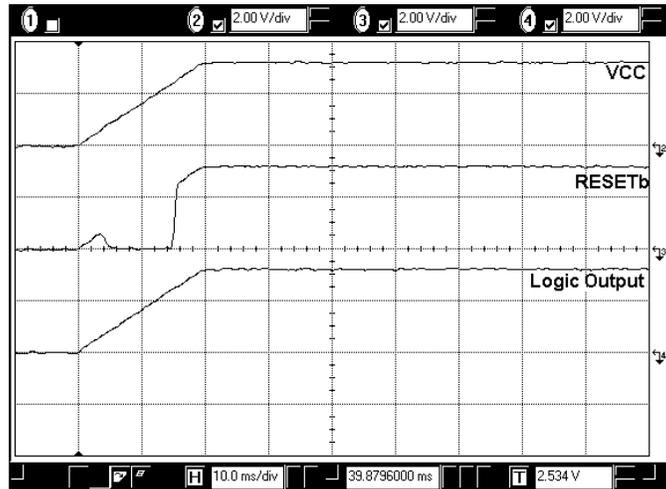

Figure 7-3. Startup with Slow Supply; Output Resets High

The behavior in both cases is identical until the time that VCC reaches 2.5V. RESETb pulls down starting at a VCC voltage of 0.8V; the RESETb output thus follows VCC up until this point. The open drain logic output retains its high impedance state until VCC reaches 2.5V; the voltage observed at the open drain logic output thus follows VCC to 2.5V. When VCC reaches 2.5V, power-on reset ends. From that point on, RESETb goes to a high level, and the logic outputs assume their programmed macrocell reset levels.

Figures 7-4 and 7-5 show the waveforms observed when the same device and setup that were examined in Figures 7-2 and 7-3 are powered from a supply that goes from 0 to 3.3V in 100 microseconds. Despite the faster power-up rate, RESETb still indicates that power-on reset starts when VCC reaches 0.8V. At this faster power-up rate, however, the time at which power-on reset ends is dominated by the time that it takes for the logic circuitry inside the ispPAC-POWR1220AT8 device to initialize, rather than occurring when VCC crosses 2.5V. Regardless of

the VCC supply ramp rate, the low-to-high transition of RESETb indicates that the logic circuitry is ready to operate, and the outputs can be observed going to their programmed states.

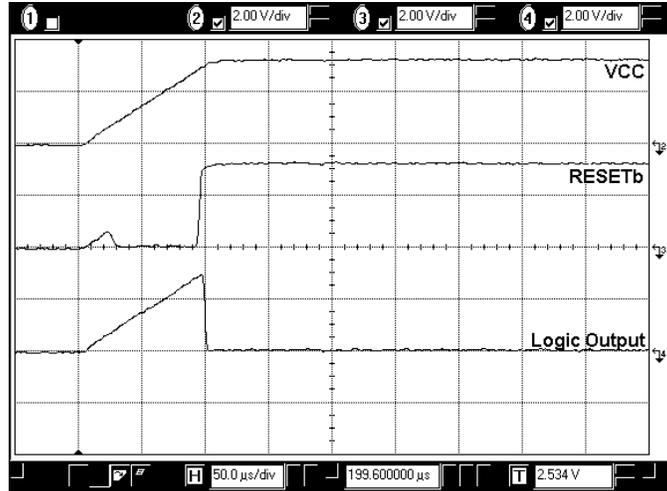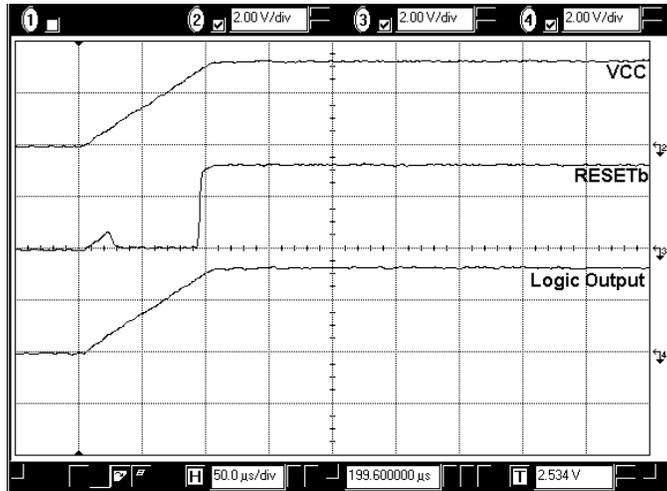*Figure 7-4. Startup with Fast Supply; Output Resets Low*

Figure 7-5. Startup with Fast Supply; Output Resets High

HVOUT pins that have been programmed for charge pump operation pull down during power-on reset regardless of the reset levels programmed into their associated macrocells. This is a safety feature that ensures that the external MOSFETs that these pins control will be off when the ispPAC-POWR1220AT8 begins its power supply sequencing operations.

A delayed reset signal, called AGOOD in PAC-Designer®, becomes true approximately 1.75 milliseconds after RESETb goes high. AGOOD is an indication that the VMON comparators and Trim DACs have successfully completed the auto-zeroing function that they perform every time that the ispPAC-POWR1220AT8 device is powered up or reset. Since the logic circuitry becomes available before the TrimDACs and VMONs, PAC-Designer's LogiBuilder interface automatically inserts a "Wait for AGOOD" instruction at the beginning of each new sequence as a convenience. The user is given the freedom to insert new steps before the "Wait for AGOOD" instruction because sequencing tasks that depend purely on digital inputs can be performed before AGOOD becomes true.

The Trim DAC outputs maintain a high impedance state during the entire power-up cycle. When AGOOD becomes true, Trim DACs programmed for E^2 fixed mode go to their programmed voltages. Trim DACs programmed for I^2C control go to their E^2 programmed bipolar zero voltage, and their associated I^2C registers default to a value of 80H.

Trim DACs programmed for closed loop trim mode go to their bipolar zero voltages and then adjust as needed to get the supply being trimmed to the desired voltage.

User-initiated Resets

The user may reset the ispPAC-POWR1220AT8 via I^{2}C or JTAG. Resetting by pulling the RESETb pin to ground is not recommended because of switch contact bounce issues. The reset behavior of the ispPAC-POWR1220AT8 involves the analog circuitry, all output pin drivers, and the I^{2}C registers, as well as the PLD; it is analogous to cycling power on the device VCC supply. The output pins will go to the states defined in Table 7-2 during a reset event.

Table 7-2. Output States During Reset

Output Pin	Reset State
OUT 5-OUT20	High-Z
HVOUT 1-4, FET Driver (as-shipped)	Discharge
HVOUT 1-4, Open-Drain	High-Z
TRIM DAC	High-Z

At the conclusion of the reset event, the RESETb pin goes high. The OUT5-OUT20 pins, as well the HVOUT pins go to their programmed levels at this time. AGOOD becomes true approximately 1.75 milliseconds after RESETb goes high. The VMON comparators and Trim DACs become operational when AGOOD becomes true.

Behavior During JTAG Programming

During JTAG programming, the RESETb pin goes to a low value, and the output pins go to the states defined in Table 7-3.

Table 7-3. Output States During JTAG Programming

Output Type	State During JTAG Programming
OUT5-OUT20	High Impedance
HVOUT	Pull-down
Trim DAC	High Impedance

HVOUT pins that were programmed for open drain logic operation temporarily change to FET driver mode during programming and pull down. This behavior ensures that any MOSFETs driven by these pins will stay off during programming. If the HVOUT pins are being used as open drain logic outputs, then it is recommended that power be supplied only to the ispPAC-POWR1220AT8 during in-system programming. Strategies for doing this are covered in a later section of this application note.

Shipped State of New Parts

ispPAC-POWR1220AT8 devices are programmed during factory testing with a sequence known as the "as-shipped" state. The output pins of devices in the as-shipped state will assume the states defined in Table 7-4 once power-on reset is completed. The I^{2}C address of devices in the as-shipped state is 0. Note that the device on an ispPAC-POWR1220AT8 evaluation board may come with a sequence programmed by the board assembler for testing purposes, and that this sequence may differ from the as-shipped state.

Table 7-4. Output Functions of Device As-Shipped from Lattice Semiconductor

Output Pin	As-Shipped State
OUT5-20	High-Z
HVOUT 1-4	Discharge (FET driver mode)
TRIM DAC	280 mV
MCLK	High-Z (Standalone clocking mode)
PLDCLK	Enabled

Ensuring Reliable Operation at Power-up

Power supply systems using the ispPAC-POWR1220AT8 should be designed such that a high impedance state on a given logic output disables the supply controlled by that pin. Supplies with negative enable logic-that is, ones in which pulling the enable pin to ground turns the supply on-can often be connected directly to the open drain output pins without any additional components. For supplies with positive enable logic, the circuit in Figure 7-6 should be used. In both cases, the DC/DC converter data sheet should be checked to see whether its enable input has a built-in pullup resistor or whether an external resistor must be used. Tables 7-5 and 7-6 list the values that should be used in the LogiBuilder OUTPUT instructions and the reset levels that should be selected in the "PINS" window for supplies with positive and negative enable logic, respectively.

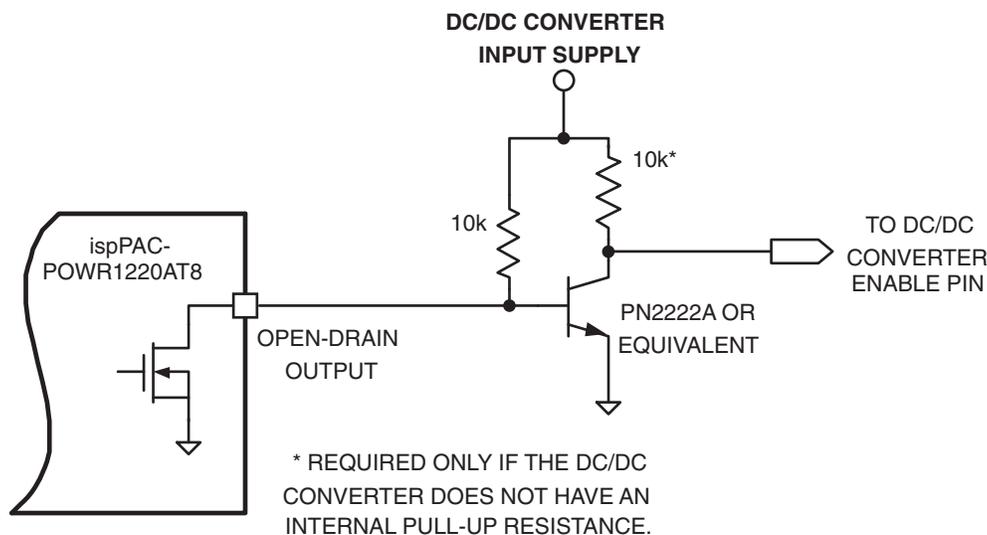*Figure 7-6. Interfacing to Supplies with Positive Enable Edge*

Table 7-5. Controlling Positive Logic Supplies

Interface Method	"PINS" Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Use Inverter Circuit (Figure 7-6)	HIGH	0 (Deassert)	1 (Assert)

Table 7-6. Controlling Negative Logic Supplies

Interface Method	"PINS" Window Reset Level	LogiBuilder OUTPUT Value to Turn Supply ON	LogiBuilder OUTPUT Value to Turn Supply OFF
Connect Directly to Open-Drain Output	HIGH	0 (Deassert)	1 (Assert)

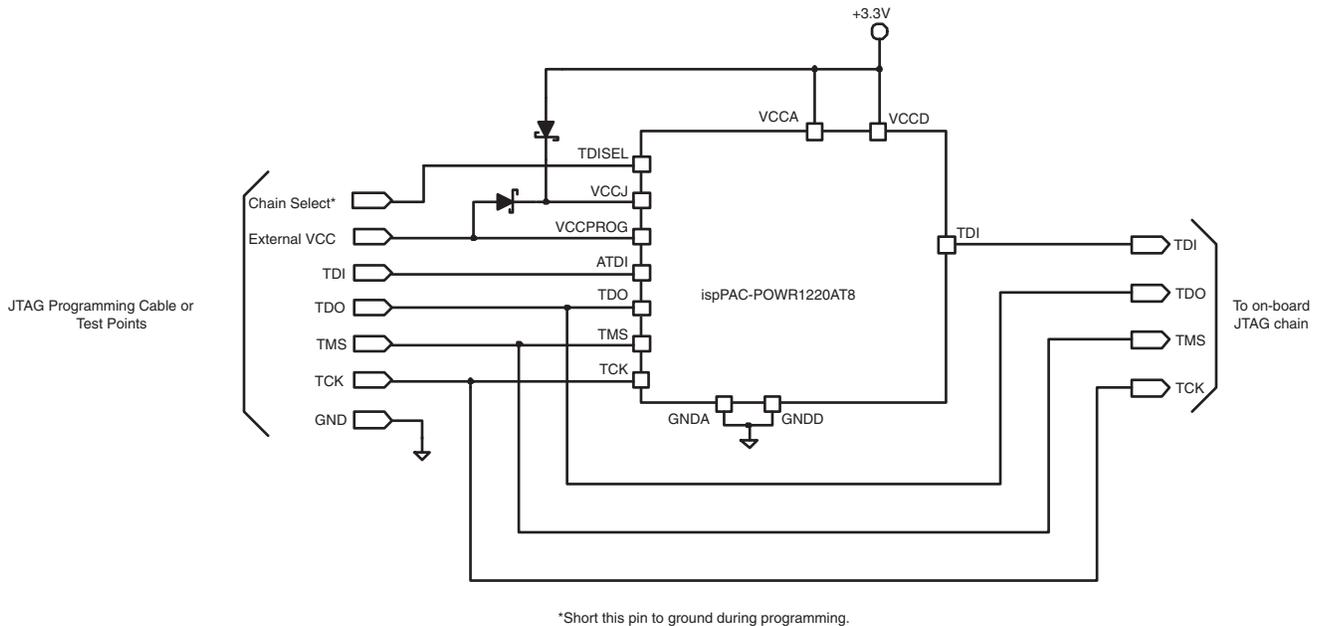# In-System Programming with the ispPAC-POWR1220AT8

If none of the HVOUT pins are being used as open drain outputs and the design guidelines presented in the previous section have been followed, all power supplies controlled by the ispPAC-POWR1220AT8 will be disabled during in-system programming. All MOSFET switches controlled by HVOUTs will be open during this time, regardless of the existing or new configuration of the device. However, if any of the HVOUTs are being used as open drain logic outputs, the circuitry controlled by these outputs should be shut down during in-system programming or the parts of the ispPAC-POWR1220AT8 not needed for JTAG programming must be shut down.

The ispPAC-POWR1220AT8 has multiple power supply pins to allow various parts of the device to be selectively powered up or shut down. The VCCPROG pin is an auxiliary means of supplying power to the circuitry associated with programming and erasing of the $E^2CMOS^®$ memory. Separate pins power the JTAG interface (VCCJ), the PLD (VCCD), and the analog blocks (VCCA). If only VCCJ and VCCPROG are powered, the device can be programmed via JTAG, but the PLD, the analog circuitry, and all of the output drivers will be disabled. During normal operation, as power a supply sequencer, power should not be applied to VCCPROG as VCCD supplies power to both the PLD and to the E^2CMOS memory.

Although there are several ways to program the device in-system, a simple, yet reliable strategy is to disable the PLD and output drivers by applying 3.3V only to VCCPROG and VCCJ while leaving the other VCC pins unpowered. The HVOUT pins, as well as OUT5-OUT20 and the Trim DAC outputs, will be in a high impedance state when the device is powered in this manner. As an additional precaution, it is recommended that the supplies sequenced by the ispPAC-POWR1220AT8 device be powered down as well.

The best way to connect and power VCCJ and VCCPROG depends on whether the JTAG interface needs to be used during normal sequencing operations. If the JTAG interface will be used solely as a programming mechanism, VCCJ and VCCPROG can be connected together and only powered during programming via the JTAG connector or pogo pins. On the other hand, if the JTAG interface needs to be used at times other than programming, some way must be provided to allow power to reach VCCJ. Figure 7-7 shows how this can be done with Schottky steering diodes. Alternatively, a jumper could be used.

Figure 7-7. Using Steering Diodes to Route Power to VCCJ

*Short this pin to ground during programming.

The circuit in Figure 7-7 also demonstrates the use of the alternate TDI selection feature of the ispPAC-POWR1220AT8. During JTAG programming, power is supplied through the "External VCC" connection. This powers VCCPROG and VCCJ through one of the diodes. TDISEL is pulled low by shorting the "Chain Select" input to

ground in order to select the ATDI pin as the active JTAG input. During normal operation, the 3.3 Volt supply is active; this powers VCCD, VCCA, and VCCJ through the other steering diode. TDISEL is allowed to float during this mode of operation; the internal pullup to VCCJ that is associated with this pin causes TDI (the on-board JTAG chain) to be selected.

The JTAG connections at the right side of Figure 7-7 can connect to a microcontroller or some other JTAG wave-form-generating device and to other JTAG compliant devices. The device that generates the JTAG waveforms sent into TDI can make use of non-programming JTAG features of the ispPAC-POWR1220AT8, such as the ability to set input IN1, the ability to issue resets, and the ability to place the ispPAC-POWR1220AT8 into JTAG bypass mode in order to address devices elsewhere in the chain. In order for this circuit to work reliably, it is important that the circuitry on the on-board JTAG chain not have internal protection diodes to VCC that could clamp the TDO, TMS, and TCK signals when these devices are powered down. Also, the on-board JTAG chain must not issue any instructions that would put the ispPAC-POWR1220AT8 into programming mode, as this would defeat the purpose of the circuit.

Capacitive Loading on Outputs

In certain applications, the outputs of the Power Manager device are used to enable the soft-start feature of a DC-DC converter. This presents a capacitive load to the outputs of the Power Manager. During the power-up cycle of the Power Manager, the open-drain outputs will transition from active low to high-z. Likewise, the HVOUT pins will transition from active low to discharge (or high-z depending on the configuration) during the power-up cycle. If the soft-start capacitors have any charge stored during this time, excessive currents will flow through the open-drain outputs to ground. These currents can result in an unreliable start-up of the Power Manager. Furthermore, during normal operation setting an output low can also result in a discharge current that exceeds the maximum current limits in the data sheet.

To ensure reliable Power Manager start-up and to limit the current surge it is required to add a series resistor when a capacitive load is connected to an output as shown in Figure 7-8. The value of R1 should be such that when C1 is discharged by the open-drain output the current is less than the $I_{SINKMAXTOTAL}$ limit in the data sheet. The $I_{SINKMAXTOTAL}$ is for any single output and is found in the Absolute Maximum Ratings Table of the data sheet. If multiple outputs have capacitive loads the $I_{SINKTOTAL}$ Max should also be considered in setting a value for the series resistors. The $I_{SINKTOTAL}$ number is found in the Digital Specifications table of the data sheet and applies to all outputs combined.

Figure 7-8. Limiting Capacitive Load Currents to Less than $I_{SINKMAXTOTAL}$
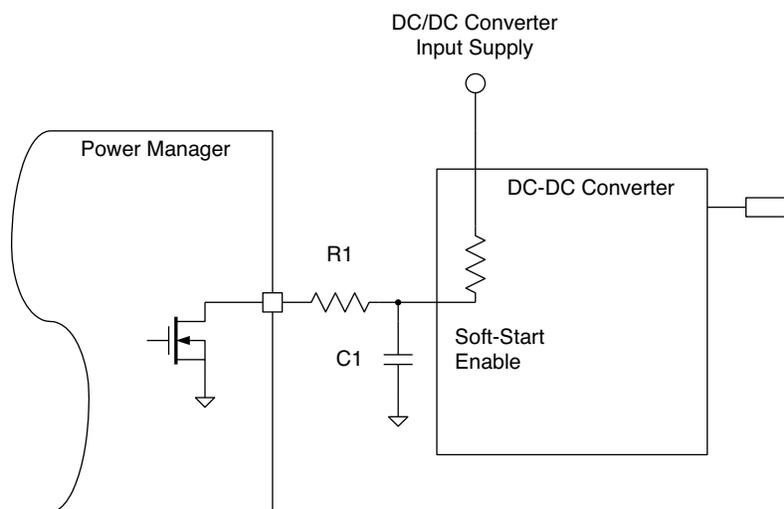
Summary

The startup characteristics of the open drain logic outputs (OUT5-OUT20), the HVOUT pins, and the Trim DACs as a function of the power-on reset condition have been described. The behavior of these outputs has also been

defined during user-issued resets and during JTAG programming. The programmed state in which new devices are shipped from the factory (the "as-shipped" state) has been described.

To ensure reliable startup of power supplies, the ispPAC-POWR1220AT8's logic outputs should be set up so that a logic low activates the supplies. Supplies that use positive enable logic require a simple one-transistor inverter to interface to the ispPAC-POWR1220AT8's open drain logic outputs.

Strategies to perform in-system programming by applying power only to VCCJ and VCCPROG are strongly suggested. An example was presented showing a system in which the ispPAC-POWR1220AT8s JTAG interface is shared between a JTAG programmer and an on-board JTAG chain that uses the device's non-programming JTAG capabilities.

When outputs are driving a capacitive load a series resistor is required to insure the discharge current is below the current limits in the data sheet.

Related Literature

- ispPAC-POWR1220AT8 Data Sheet

- AN6068, Programming the ispPAC-POWR1220AT8 in a JTAG Chain Using the ATDI Pin

Technical Support Assistance

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Revision History

Date	Version	Change Summary
March 2006	01.0	Initial release.
April 2011	01.1	Updated to address capacitive loading on the outputs.