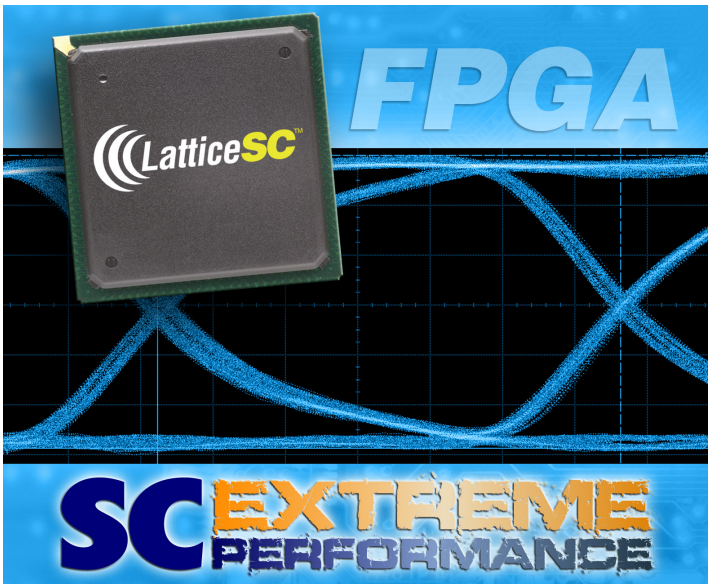
LatticeSC FPGA Family

Innovation, Integration, and PURESPEED™

The LatticeSC™ (System Chip) family of FPGAs combines a high-performance FPGA fabric, 3.8Gbps SERDES and PCS, high-performance I/Os, large embedded RAM, and embedded ASIC blocks in a single industry-leading architecture. This FPGA family is fabricated on a state-of-the-art Fujitsu 90nm technology to provide the highest performance FPGA in the industry.

This family of devices includes specific features to meet the needs of today's high-speed connectivity-based system designs. These features include SERDES, the industry's most advanced embedded PCS (Physical Coding sub-layer), up to 7.8Mb of Embedded Block RAM (EBR), and dedicated I/O logic to support source synchronous I/O standards such as RapidIO, HyperTransport™, SPI4.2, SFI4, and XGMII. A plethora of hierarchical clock routing and clock management resources are provided to support the precise programmable logic timing needed in today's high-end system designs. High-speed I/O with bandwidths up to 2Gbps per pin make this family ideal for high throughput systems. And for low-cost system-level integration, the LatticeSC family offers up to 12 embedded structured ASIC blocks per device with a variety of pre-engineered IP blocks.

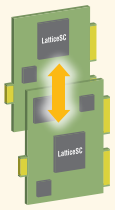


Key Features and Benefits

- **High Performance FPGA Fabric**
  - Industry's fastest FPGA core performance
  - 15K to 115K four-input Look-up Tables (LUT4s)
  - 139 to 942 I/Os
  - 700MHz global clock; 1GHz edge clocks

High-Speed Connectivity Solutions

- **Backplane / High Speed Serial**
  - Integrated high-speed SERDES
  - Supports SONET, GbE, XAUI, PCI Express, Fibre Channel, SFI-5 and more
  - More SERDES channels for greater flexibility and easier customization



- **Chip-to-chip / Chip-to-memory**
  - Lattice PURESPEED I/O technology enables connectivity to virtually any digital device
  - Each PURESPEED I/O buffer supports up to 2Gbps
  - Supports parallel I/O standards, from 2Gbps LVDS to PCI/PCI-X
  - Dedicated interface logic seamlessly handles SDR/DDR/QDR memories

- **Networking Datapath**
  - Ideal for bridging ASSPs
  - LatticeSC devices include: high-speed logic, embedded RAM, fast clocking schemes, and ample routing for maximum utilization

- **High Speed SERDES and flexiPCS™**
  - 4 to 32 SERDES per device @ 600Mbps to 3.8Gbps
  - Tx pre-emphasis and Rx equalization
  - Low power (105mW per channel)
  - Embedded Physical Coding Sublayer (PCS) supports: PCI Express, GbE, XAUI, SONET, and other packet protocols

- **PURESPEED™ Technology: 2Gbps Parallel I/O**
  - Input Delay (INDEL) and Adaptive Input Logic (AIL) dynamically aligns data for robust high performance source synchronous I/O support
  - Supports generic DDR up to 2Gbps; generic SDR up to 1Gbps; DDR memories up to 800Mbps
  - Comprehensive standards support: LVCMOS, LVTTL, PCI, PCI-X, LVDS, HyperTransport, HSTL, SSTL, with programmable On Die Termination (ODT) options

- **Memory Intensive FPGA**
  - 1Mb to 7.8Mb Embedded Block RAM @ 500MHz
  - Additional Distributed RAM: 240K to 1.8Mbits

- **sysCLOCK™ PLLs and DLLs**
  - Eight PLLs per device and twelve DLLs per device
  - Spread spectrum support on PLLs

- **Masked Array for Cost Optimization (MACO™)**
  - On-chip structured ASIC blocks provide pre-engineered IP at lower power and cost

- **System Level Support**
  - IEEE Standard 1149.1 boundary scan
  - IEEE Standard 1532 in-system configuration
  - Embedded PowerPC microprocessor interface
  - Embedded system bus

LatticeSC Architecture

Architecture Overview

The LatticeSC family of FPGAs combines a high-performance FPGA fabric, high-speed SERDES, structured ASIC blocks, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated on Fujitsu's 90nm CMOS process technology to provide one of the highest performance FPGAs in the industry.

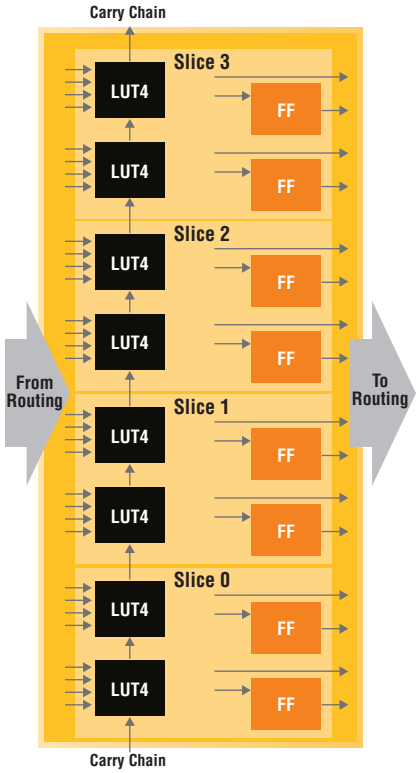
Lattice offers the most advanced portfolio of innovative packaging solutions available today. With up to 942 I/Os and 32 SERDES channels in a device, the LatticeSC family is offered in wire-bonded BGA and Flip Chip packages to 1704 balls.

Programmable Function Unit Blocks (PFU)

The core of LatticeSC devices consists of Programmable Functional Units (PFUs). The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions.

- **Four Slices per PFU**
- **Slices can be Concatenated for Longer Functions**
- **PFUs can be Concatenated for Complex Functions**

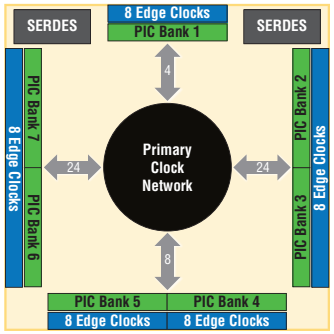
PFU Block Diagram



Extreme Clocking Performance

To support an internal fabric capable of 500MHz performance, LatticeSC devices have three distinct clock networks for use in distributing high-performance clocks within the device: primary clocks; secondary clocks; and edge clocks. In addition, the LatticeSC is the only FPGA that combines, on one device, multiple programmable PLLs and DLLs for clock multiplying, dividing and phase shifting.

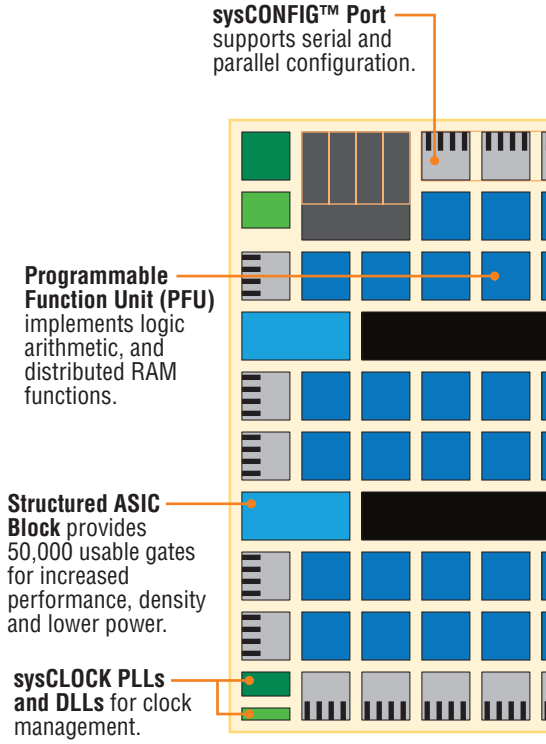
Edge and Primary Clocks



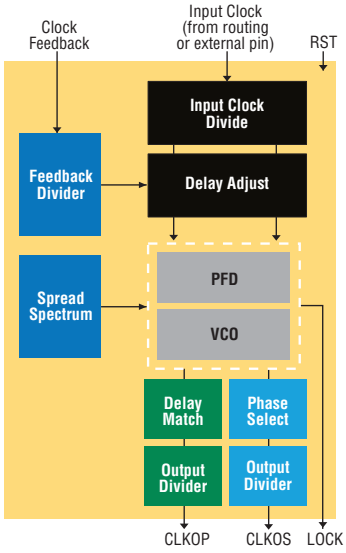
sysCLOCK PLLs & DLLs for Tight Timing Control

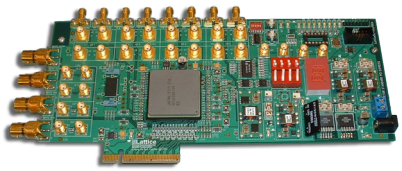
- **PLLs Feature:**
  - Output 1.56MHz to 1GHz
  - VCO 100MHz to 1GHz
  - Input 15MHz to 1GHz
  - Low output jitter
  - Dynamic reconfiguration of loop parameters
  - Programmable M, N dividers (1x–64x)
  - Spread Spectrum generation support
- **DLLs Feature:**
  - Output 1.56MHz to 700MHz
  - Input 100MHz to 700MHz
  - Output dividers (½, ¼)
  - Digital control for use with INDEL
  - Duty cycle correction
- **Addtional Clocking Features**
  - Phase matched clock dividers
  - Dynamic clock switching

LatticeSC Block Diagram

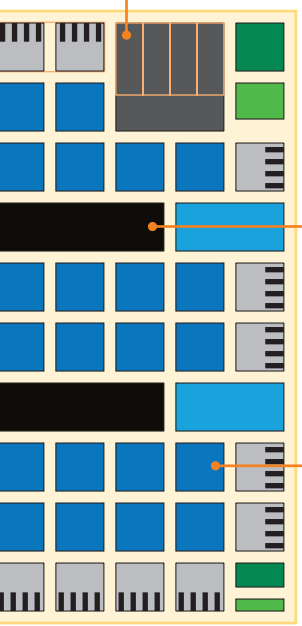


sysCLOCK PLL Block Diagram





LatticeSC evaluation boards provide a platform to fully evaluate the benefits of Extreme Performance in a lab setting.



SERDES and flexiPCS

Lattice pioneered the concept of combining SERDES and optimized PCS on a programmable device.

- **Up to 32 Channels per Device**
- **Speeds from 600Mbps up to 3.8Gbps**
- **High Rx Jitter Tolerance (0.8UI @ 3.125Gbps)**
- **Low Tx Jitter (0.25UI @ 3.125Gbps)**
- **Receiver Programmable Coupling (AC or DC)**
- **Channel Bonding on a Single Device and/or between Devices**
- **Tx Pre-emphasis and Rx Equalization for Improved BER over Long FR-4 Trace Lengths (>60")**
- **Very Low Power (105mW/Ch Typical @ 3.125Gbps)**
- **PCS Compliant to a Number of Current and Emerging Standards**

Lattice's innovative flexiPCS technology provides embedded multi-protocol Physical Coding Sublayer (PCS) functionality in LatticeSC FPGAs.

sysMEM™ Embedded Block Memory

Each 18Kb sysMEM block can implement single port, true dual port, pseudo dual port or FIFO memories. Dedicated FIFO support logic allows the LatticeSC devices to efficiently implement FIFOs without consuming LUTs or routing resources for flag generation.

- **1Mb to 7.8Mb of Block Memory per Device**
- **500MHz Operation**
- **Configurable Width/Depth**
- **Bus Size Matching**
- **RAM Initialization & ROM Operation**
- **Memory Cascading**

Flexible sysMEM Blocks

Memory Mode	Configurations	
Single Port	16,384 x 1 8,192 x 2 4,096 x 4	2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4	2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4	2,048 x 9 1,024 x 18 512 x 36
FIFO	16,384 x 1 8,192 x 2 4,096 x 4	2,048 x 9 1,024 x 18 512 x 36

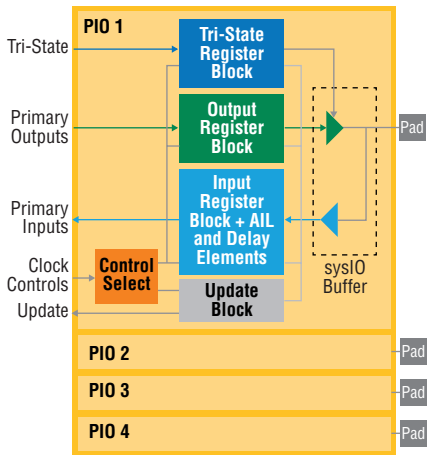
PURESPEED

Extreme Performance I/O Technology

Programmable I/O Cells

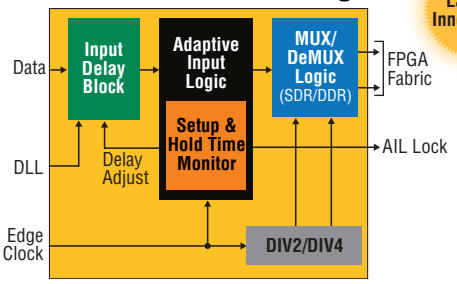
Each Programmable I/O Cell (PIC) contains four programmable I/Os (PIOs) connected to their respective buffer which are then connected to the device pads. The PIO contains innovative capabilities to allow the support of speeds up to 2Gbps. These include dedicated shift and DDR logic and adaptive input logic. The dedicated resources simplify the design of robust interfaces. In addition each pin features digitally controlled on-chip output impedance and input termination.

Programmable I/O Cell (PIC) Block DiAgram



INDEL and AIL Block Diagram

Lattice Innovation



MACO Masked Array for Cost Reduction

MACO Overview

Think of MACO blocks as structured ASICs embedded in an FPGA fabric. MACO technology is based on a unique library of cells created with Fujitsu's 90nm CMOS process technology and optimized for speed, power and area. Each MACO block is equivalent to approximately 50,000 ASIC gates. Lattice provides a set of pre-engineered standard-compliant MACO functions on each LatticeSCM™ device, reducing your design effort and time-to-market. Once you purchase a LatticeSCM device, no additional IP license fees are required.

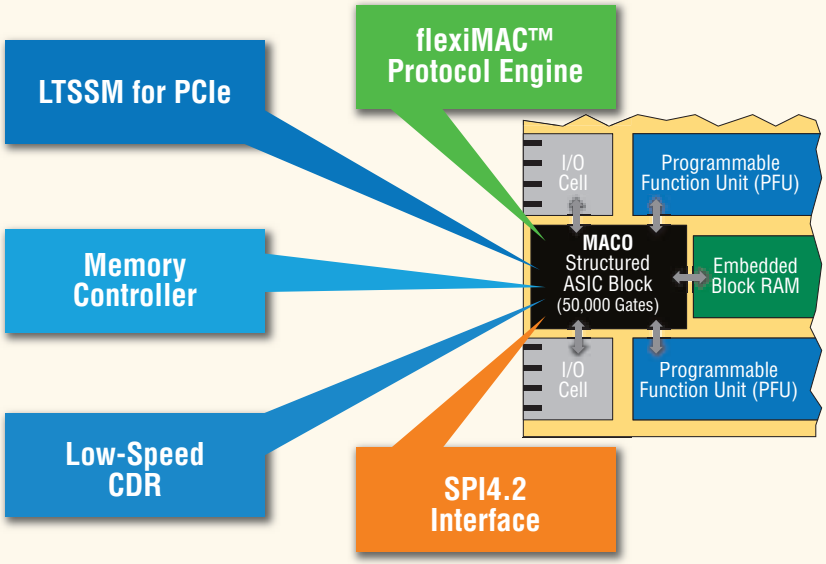
A MACO core occupies only 10% of the area of an equivalent FPGA implementation. With multiple MACO blocks per device, this results in a substantial cost savings to the designer, both by lowering the development cost and saving significant silicon area. Because MACO is a cell-based technology, it typically offers twice the performance while consuming less than half the power of a standard implementation using FPGA gates. All MACO blocks are easily configured using IPexpress in Lattice's ispLEVER® design tool.

MACO for System Level Connectivity

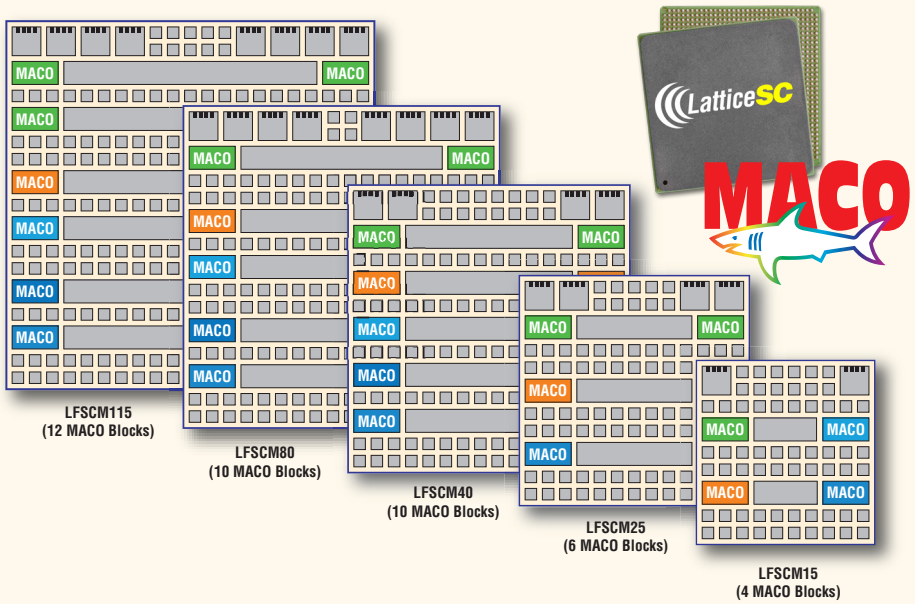
MACO blocks are an integral part of the LatticeSCM connectivity solution. In applications such as Ethernet and PCIe, the MACO blocks function seamlessly with the embedded PCS layer and SERDES in the LatticeSCM device to provide the industry's most integrated FPGA solution for modern serial protocols. Additional MACO blocks handle standards driven interfaces to ASSPs such as network processors, traffic managers, and memory devices through SPI4.2, DDR I/II, QDR II and RLDRAM

LatticeSCM The Industry's Most Compact SPI4 to XAUI Bridge

5 MACO Blocks Available Today!



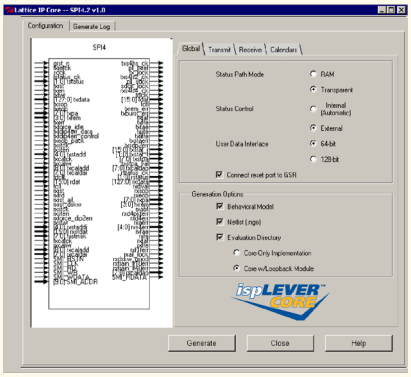
LatticeSCM Devices are Loaded with up to 12 MACO Blocks!



IPexpress Tool

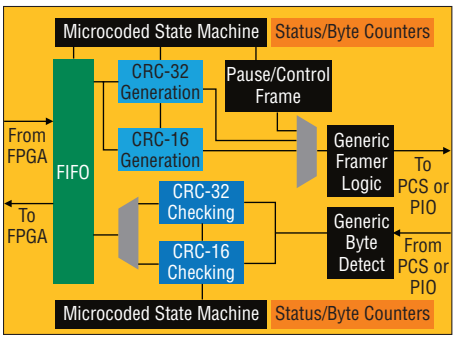
Lattice's IPexpress™ tool greatly simplifies the MACO design process. The IPexpress design flow enables users to fully parameterize MACO blocks in real-time. Designers can then instantiate the user-configured IP and complete the design process, including full timing simulation and bitstream generation.

IPexpress USER CONFIGURABLE



MACO Blocks in Detail

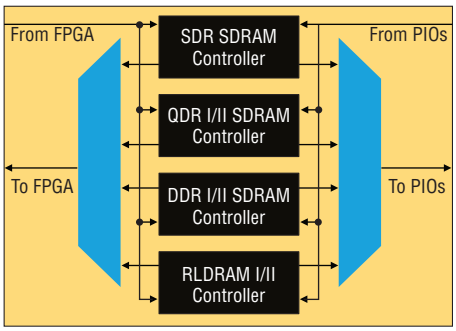
flexiMAC Protocol Engine – Configurable at design time for:



PCI Express
- Appends/Strips Sequence Number and LCRC to/from TLP
- Stores Transaction Layer Protocols (TLPs) for DLL Retry
- Provides Data Link Layer Packets (DLLPs)
- Data Link Control & Management State Machine
- Data Integrity Checks (LCRC)

Ethernet
- Collapses Multiple DLLPs
- 1GbE or 10GbE MAC Function
- Flexible Packet Framer and Parser
- Seamlessly Connects with SERDES/PCS
- Provides Multi-Protocol Functionality
- Complete Layer 1/2 Solution

Memory Controller – Configurable at design time for:



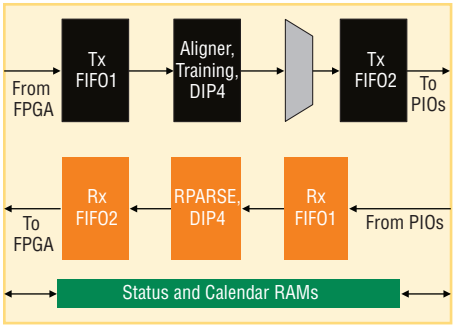
DDR II (333MHz/ 667Mbps)
- Data Path Widths of 8-72 Bits
- Programmable Address Widths
- Burst Length of 4 or 8
- 2 Chip Selects
- Programmable Timing Parameters
- True and Complementary DQS

RLDRAM II (400MHz/800Mbps)
- CIO and SIO Devices
- Burst Lengths of 2, 4 or 8

- Supports Cascading
- Cyclic Bank Access
- Programmable Data Path Widths
- Supports Data Mask

QDR II (250MHz/500Mbps)
QDR II+ (375MHz/750Mbps)
- Programmable Data and Address Widths
- Programmable Burst Sizes
- Supports Read and Write Interleaving

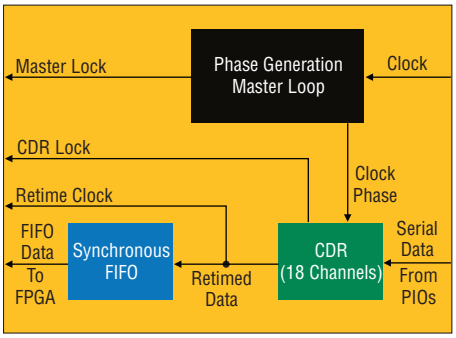
SPI4.2



- Fully Compliant With OIF-SPI4-02.0 Specification
- Up to 256 Logical Ports
- Static and Dynamic Alignment Modes
- Up to 1 Gbps Dynamic Phase Alignment
- Up to 700Mbps Static Alignment
- Additional Quarter Rate Mode for Sub-10G Traffic

- Programmable Burst Modes to Support Intel Requirements
- Optional User Defined Status Path
- Lowest Power Solution Available!

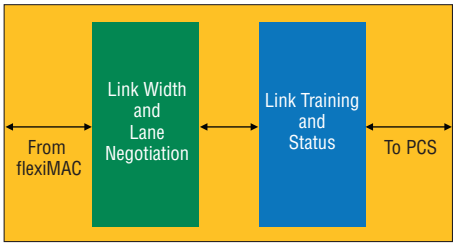
Low Speed CDR (available on the SC40, SC80 and SC115)



- Used for Retiming Slow Speed Data Streams from 100 - 550 Mbps
- Jitter Tolerance of 0.85UI
- No Additional Logic Required (FIFOs are Built-in)
- Supports 18 Data Channels
- Includes Synchronous Mode for 36-bit AIL-like Channels

- Supports Pathological Signals
- Multi-rate Support on a Single Pin!

LTSSM for PCIe



- Integral Part of PCI Express Solution
- PHY Framing
- Link Training & Status State Machine
- Link Width & Lane Negotiation
- Checking of Violations of the Link Initialization and Training Protocols

- Disables the Scrambling Function Upon Being Notified by the Data Link Layer

Lattice Diamond Design Software

Lattice Diamond® design software offers leading-edge design and implementation tools optimized for Lattice FPGA architectures. Diamond is the next generation replacement for ispLEVER® featuring design exploration, ease of use, improved design flow, and numerous other enhancements. The combination of new and enhanced features allows users to complete designs faster, easier, and with better results than ever before.

Intellectual Property

Lattice offers an expanding portfolio of IP cores (LatticeCORE™) to support the easy integration of commonly used functions. IP cores targeted to the LatticeSC FPGA family include:

- PCI Express
- Serial RapidIO
- SPI4.2
- 10GbE MAC
- PCI Master/Target
- PCI Target
- DDR1/DDR2
- SC-DMA
- Multimedia Cores
- Triple Speed Ethernet MAC
- Soft Error Detection
- SGMII
- OBSAI
- CPRI
- XAUI to SPI4 Bridge
- Encryption (AES/DES/3DES)
- HiGig™/HiGig+™/MAC
- Microcontrollers/Microprocessors

For additional IP cores, go to www.latticesemi.com/ip.

LatticeSC Device Selection Guide

Parameter	LFSC15	LFSC25	LFSC40	LFSC80	LFSC115
Logic Resources – LUTs (K)	15	25	40	80	115
sysMEM EBR RAM Blocks (18Kb / Block)	56	104	216	308	424
Embedded Memory (Mbits)	1.03	1.92	3.98	5.68	7.8
Max. Distributed Memory (Mbits)	0.24	0.41	0.65	1.28	1.84
Max. # of SERDES Channels (3.8Gbps)	8	16	16	32	32
DLLs	12	12	12	12	12
PLLs	8	8	8	8	8
MACO Blocks (50K ASIC Gates Each)	4	6	10	10	12
Packages	**I/O / Full-Duplex SERDES Channels**				
256-ball fpBGA (17 x 17 mm)	139 / 4				
900-ball fpBGA (31 x 31 mm)	300 / 8	378 / 8			
1020-ball fcBGA (33 x 33 mm)		476 / 16	562 / 16		
1152-ball fcBGA (35 x 35 mm)			604 / 16	660 / 16	660 / 16
1704-ball fcBGA (42.5 x 42.5 mm)				904 / 32	942 / 32

Pre-Engineered Embedded IP Blocks Available in the LatticeSCM Family

IP Blocks	LFSCM15	LFSCM25	LFSCM40	LFSCM80	LFSCM15
flexiMAC Blocks PCI Express Mode; 10GbE Mode; 1GbE Mode	1	2	2	2	4
SPI4.2 Blocks	1	2	2	2	2
Memory Controller Blocks DDR/DDR2 DRAM Controller; QDR II/II+ SRAM Mode; RLDRAM I; RLDRAM II CIO/SIO	1	2	2	2	2
Low Speed CDR Blocks	0	0	2	2	2
PCI Express LTSSM Blocks	1	0	2	2	2

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