Lattice® Semiconductor Corporation

SPI Serial Flash Programming Using ispJTAG in LatticeSC Devices

January 2008 Technical Note TN1100

Introduction

LatticeSC™ FPGAs allow direct programming of the SPI Serial Flash via the ispJTAG™ interface. The ispJTAG communicates to the 4-wire interface to the SPI Flash 4-wire interface. The ispJTAG is free to read or write the SPI Serial Flash while the FPGA is executing user code. This allows the user to perform functions such as background configuration updates.

Programming Procedures

In order to program the SPI Serial Flash via ispJTAG, the FPGA MODE [3:0] pins of the LatticeSC must be set to program using SPI configuration modes. Refer to Lattice technical note number TN1080, *LatticeSC sysCONFIG Usage Guide* for hardware information and specifications.

Programming the SPI Serial Flash with ispVM® System and an ispDOWNLOAD® cable provides a simple solution for the user. The software sends the appropriate JTAG instruction to the ispJTAG port, allowing the bitstream to pass through the FPGA, providing the proper handshaking for the SPI Flash device and writing the user bitstream into the Flash.

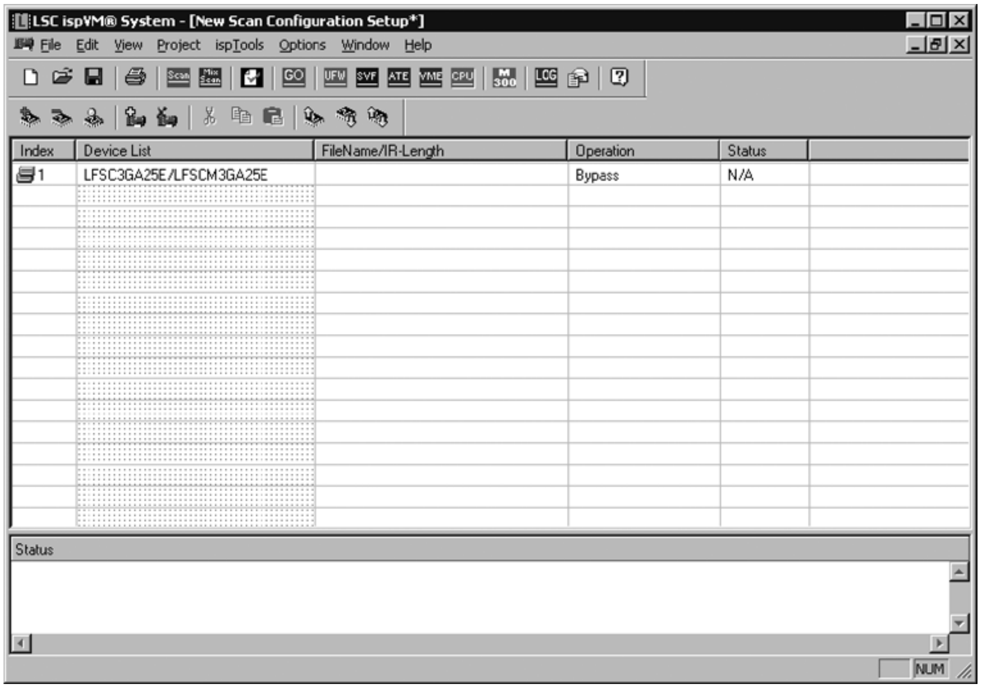
Once programming of the SPI Serial Flash is complete the FPGA configures itself by reading the Flash. The Flash memory is read transparent to the user so that it is no different than programming any other serial boot device.

ispVM Flash Programming Tutorial

The following instructions describe the process of selecting the FPGA, selecting the SPI Serial Flash, and programming the SPI Serial Flash. The screen shots are from ispVM System version 15.4.4.

1. Connect the ispDOWNLOAD Cable to the appropriate header and apply power to the board.
2. Start the ispVM System software.
3. From the main window, click on the **Scan** button located on the toolbar. The LatticeSC device should be detected automatically (if it is not detected, check the ispJTAG connections and make sure the board is powered up). The resulting screen should be similar to Figure 1.

Figure 1. Main Window Scan Complete



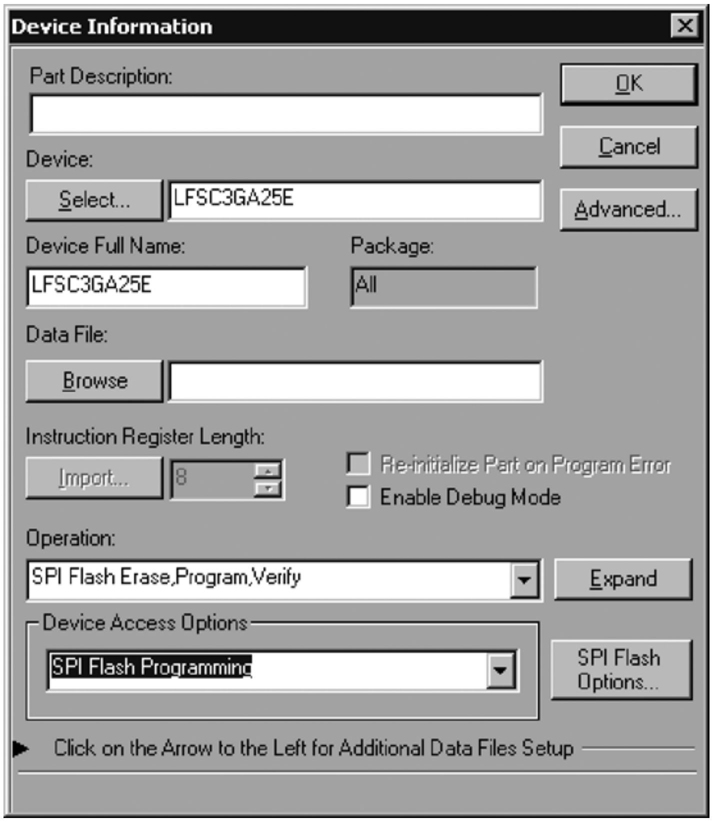
LSC ispVM® System - [New Scan Configuration Setup*]

Index	Device List	FileName/IR-Length	Operation	Status
1	LFSC3GA25E/LFSCM3GA25E		Bypass	N/A

Status

4. Double-click the number in the **Index** column and select the appropriate device to open the **Device Information** window, shown in Figure 2.

Figure 2. Device Information Window



Device Information

Part Description:

Device: LFSC3GA25E

Device Full Name: LFSC3GA25E

Package: All

Data File:

Instruction Register Length: 8

□ Re-initialize Part on Program Error

□ Enable Debug Mode

Operation: SPI Flash Erase,Program,Verify

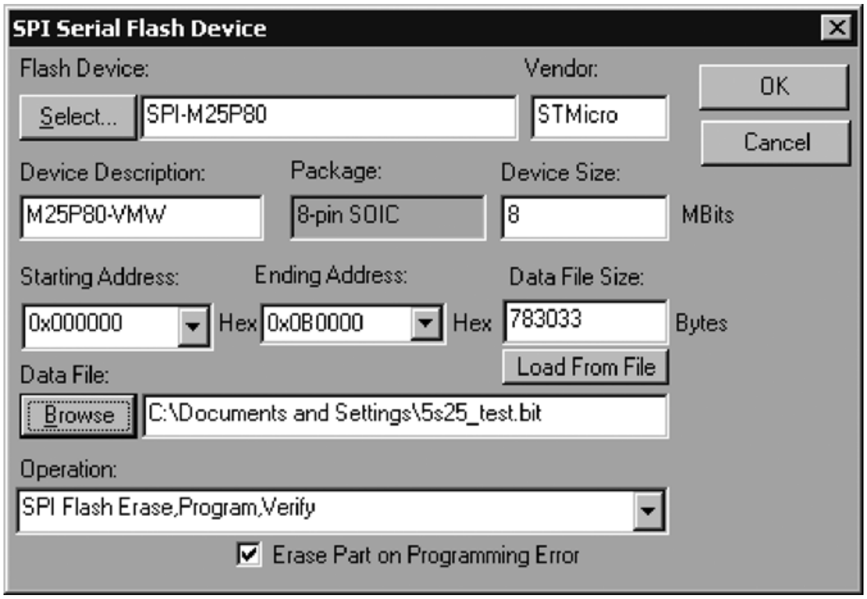
Device Access Options: SPI Flash Programming

▶ Click on the Arrow to the Left for Additional Data Files Setup

a. Under **Device Access Options**, select **SPI Flash Programming**.

b. Select the **SPI Serial Flash Options** button and the dialog shown in Figure 3 will be displayed.

Figure 3. SPI Serial Flash Device Dialog



SPI Serial Flash Device

Flash Device: SPI-M25P80

Vendor: STMicro

Device Description: M25P80-VMW

Package: 8-pin SOIC

Device Size: 8 MBits

Starting Address: 0x000000 Hex

Ending Address: 0x0B0000 Hex

Data File Size: 783033 Bytes

Data File: C:\Documents and Settings\5s25_test.bit

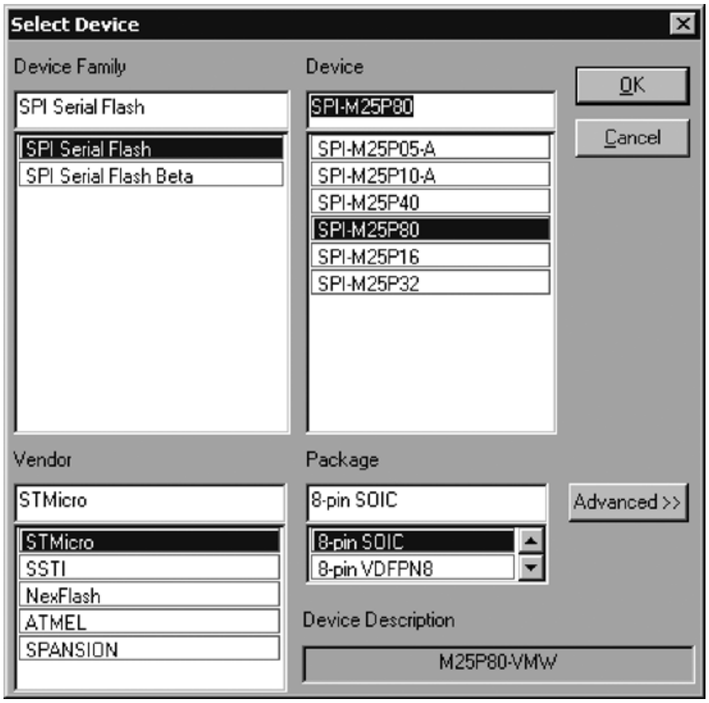
Operation: SPI Flash Erase,Program,Verify

☑ Erase Part on Programming Error

c. Under **Data File**, select **Browse** and select the LatticeSC bitstream to be programmed into the SPI Serial Flash device. This can be a prom image file(.mcs or .eco) or a bitstream file. Click the **OK** button.

d. Click on the **Select** button to select the target SPI Serial Flash device. The SPI Serial Flash Select Device dialog shown in Figure 4 will be displayed.

Figure 4. Select SPI Serial Flash Device Dialog



Select Device

Device Family: SPI Serial Flash

- SPI Serial Flash
- SPI Serial Flash Beta

Device: SPI-M25P80

- SPI-M25P05-A
- SPI-M25P10-A
- SPI-M25P40
- SPI-M25P80
- SPI-M25P16
- SPI-M25P32

Vendor: STMicro

- STMicro
- SSTI
- NexFlash
- ATMEL
- SPANSION

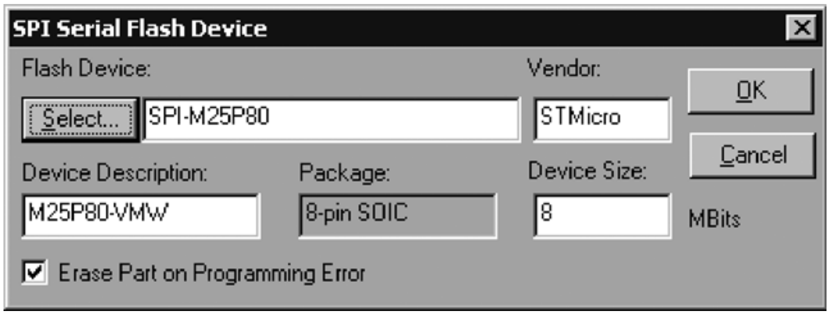
Package: 8-pin SOIC

- 8-pin SOIC
- 8-pin VDFPN8

Device Description: M25P80-VMW

e. Select the target SPI Serial Flash device and click the **OK** button. The SPI Serial Flash Device dialog shown in Figure 5 will be displayed.

Figure 5. SPI Flash Device Dialog



SPI Serial Flash Device

Flash Device: SPI-M25P80

Vendor: STMicro

Device Description: M25P80-VMW

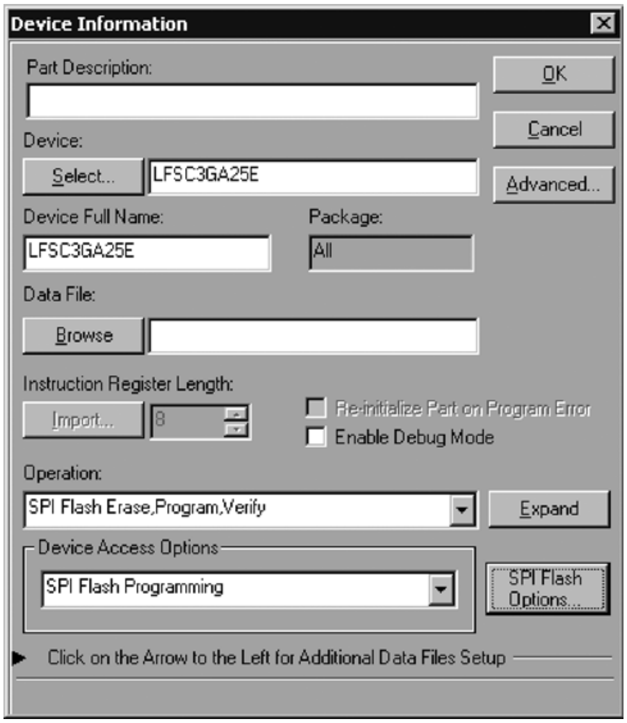
Package: 8-pin SOIC

Device Size: 8 MBits

☑ Erase Part on Programming Error

f. Click the **OK** button. The Device Information dialog shown in Figure 6 will be displayed.

Figure 6. SPI Serial Flash Device Information Dialog



Device Information

Part Description:

Device: LFSC3GA25E

Device Full Name: LFSC3GA25E

Package: All

Data File:

Instruction Register Length: 8

☐ Re-initialize Part on Program Error

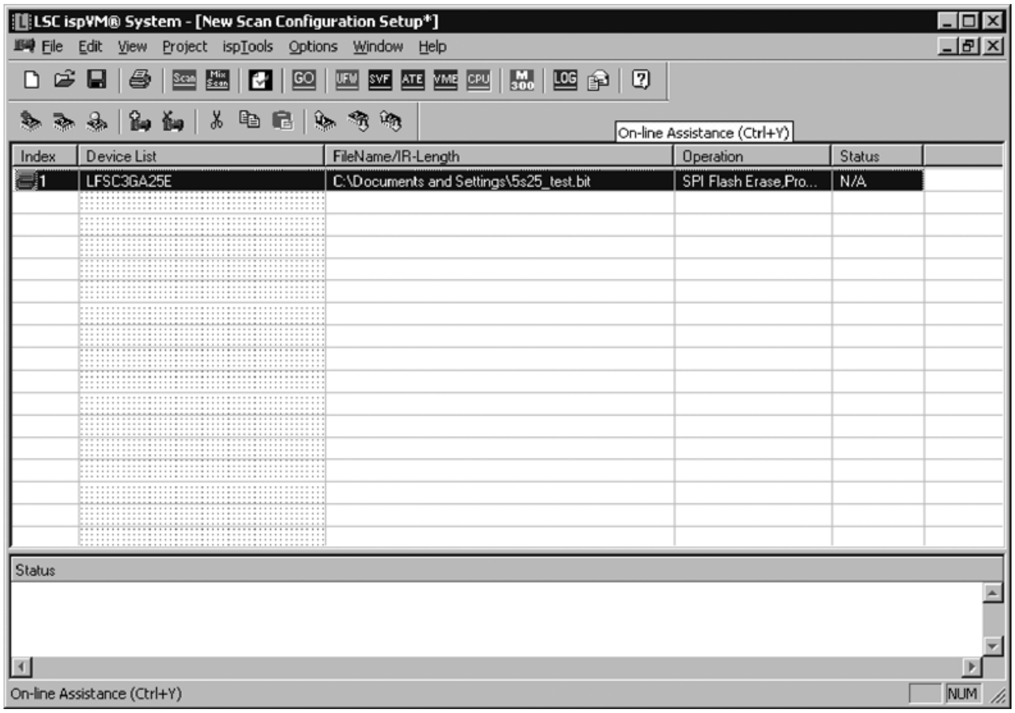
☐ Enable Debug Mode

Operation: SPI Flash Erase,Program,Verify

Device Access Options: SPI Flash Programming

▶ Click on the Arrow to the Left for Additional Data Files Setup

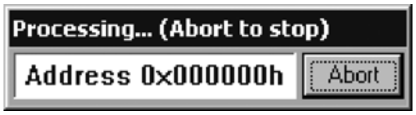
Figure 7. Main Window, SPI Programming


LSC ispVM® System - [New Scan Configuration Setup*]
File Edit View Project ispTools Options Window Help
Scan
Mix Scan
GO
UFM
SVF
ATE
VME
CPU
LOG
On-line Assistance (Ctrl+Y)
Status
On-line Assistance (Ctrl+Y)
NUM

Index	Device List	FileName/IR-Length	Operation	Status
1	LFSC3GA25E	C:\Documents and Settings\5s25_test.bit	SPI Flash Erase,Pro...	N/A

5. From the toolbar, select **GO**. Figure 8 shows the response of ispVM while programming the Flash.

Figure 8. Runtime Message while Programming SPI Flash



Address 0x000000h

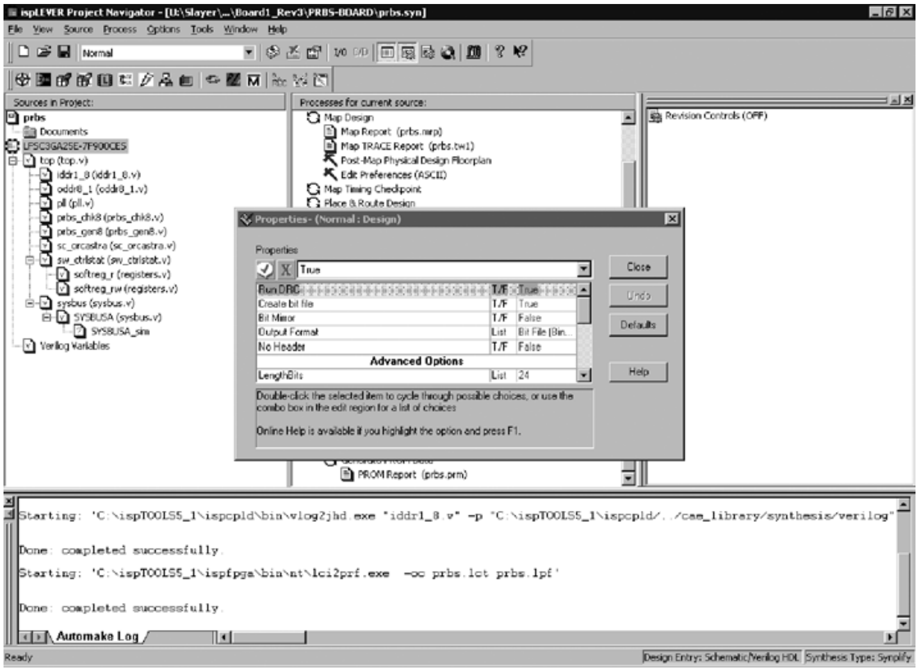
Using Multiple Configuration Bitstreams

LatticeSC devices can access several bitstream images stored in one or more Flash memories. When the FPGA device is initially configured using SPI memory, the start address is assumed to be 0x00000000. If multiple images need to be accessed, bitstream configurations with an alternate starting address are stored in a 32-bit register in the configuration memory of the LatticeSC device. If the device is reconfigured without initialization, the starting address specified in SPI_RECONFIG_START_ADDRESS[31:0] will be shifted in. This allows for multiple configuration images to be stored in the same SPI Flash memory or memories if multiple devices are used.

The start address will be latched upon the DONE signal going high so that it does not change during the re-configuration of the device. The memory cells storing the data can be rewritten, providing a new starting address, but the address used for the current configuration sequence does not change. This eliminates the need to preserve the memory contents of the design as needed when doing partial reconfigurations.

The first step in generating a configuration to be loaded from a non-zero address is to program the prior bitstream with a specific address. This is accomplished by using the Bitstream Generator utility in the ispLEVER® software. For example, if the user wishes to read an image from Flash stored at start address 0x030000, the user should set SPI_RECONFIG_START_ADDRESS =0x030000 in the prior bitstream. This address is specified by the ispLEVER Project Navigator GUI by right-clicking Bitstream Generation=>Properties=> SPI_RECONFIG_START_ADDRESS, and entering the desired start address. Bitstreams can also be compressed by the software which will minimize memory storage of the images.

Figure 9. ispLEVER Bitstream Generation Window



Properties

True

Run DRC	T/F	True
Create bit file	T/F	True
Bit Mirror	T/F	False
Output Format	List	Bit File (Bin...
No Header	T/F	False
Advanced Options		
LengthBits	List	24

Double-click the selected item to cycle through possible choices, or use the combo box in the edit region for a list of choices

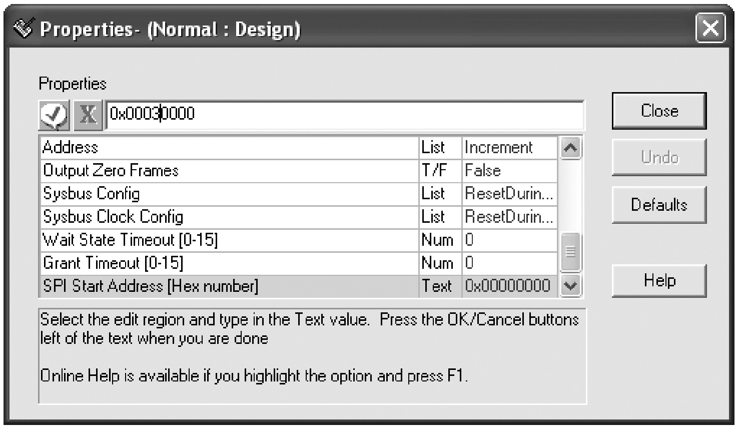
Online Help is available if you highlight the option and press F1.

```
Starting: 'C:\ispTOOLS5_1\ispcpld\bin\vlog2jhd.exe "iddr1_8.v" -p "C:\ispTOOLS5_1\ispcpld/../cae_library/synthesis/verilog"

Done: completed successfully.
Starting: 'C:\ispTOOLS5_1\ispfpga\bin\nt\lci2prf.exe  -oc prbs.lct prbs.lpf'

Done: completed successfully.
```

Figure 10. Changing the SPI Flash Start Address Index



Properties

0x00030000

Address	List	Increment
Output Zero Frames	T/F	False
Sysbus Config	List	ResetDurin...
Sysbus Clock Config	List	ResetDurin...
Wait State Timeout [0-15]	Num	0
Grant Timeout [0-15]	Num	0
SPI Start Address [Hex number]	Text	0x00000000

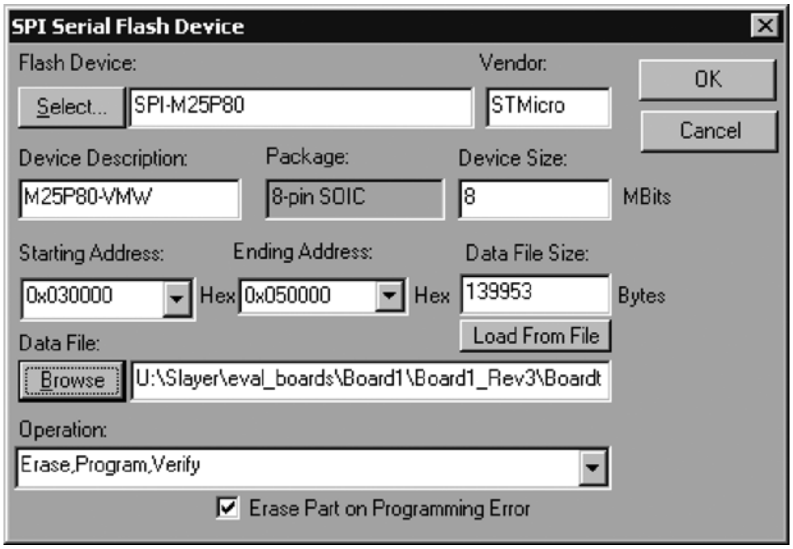
Select the edit region and type in the Text value. Press the OK/Cancel buttons left of the text when you are done

Online Help is available if you highlight the option and press F1.

This initial bitstream should be loaded into the Flash device using ispVM as mentioned in the earlier tutorial. This will be the design loaded at power-up.

At this point, ispVM can be used to write the second bitstream to the non-zero start address. This is accomplished by following steps 1 to 4 of the ispVM Flash Programming Tutorial in this document. After following these initial steps, the user must assign the load address of the bitstream by selecting the desired Data File (.bit or .rbt) and then selecting the specific Starting Address. This is shown in Figure 11.

Figure 11. Non-Zero Starting Address Flash Programming



SPI Serial Flash Device

Flash Device: SPI-M25P80

Vendor: STMicro

Device Description: M25P80-VMW

Package: 8-pin SOIC

Device Size: 8 MBits

Starting Address: 0x030000 Hex

Ending Address: 0x050000 Hex

Data File Size: 139953 Bytes

Data File: U:\Slayer\eval_boards\Board1\Board1_Rev3\Boardt

Operation: Erase,Program,Verify

☑ Erase Part on Programming Error

Continue the remaining steps to write the bitstream to the Flash. These steps can be repeated to load multiple images to one or more cascaded Flash devices. Cascaded Flash devices are discussed further in Lattice technical note number TN1080, *LatticeSC sysCONFIG Usage Guide.*

Conclusion

The LatticeSC family of devices can be combined with low-cost, third-party serial Flash. System designs can take advantage of a very cost-effective system solution. In addition to cost savings, the design also benefits from the space conscious 8-pin package. This new capability, in addition to traditional configuration methods, is fully supported by the latest Lattice design tools.

For more information on Lattice products, visit the Lattice web site at www.latticesemi.com.

References

- Lattice Technical Note TN1080, *LatticeSC sysCONFIG Usage Guide*
- ispLEVER Software Documentation
- ispVM Software Documentation

Technical Support Assistance

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Revision History

Date	Version	Change Summary
February 2006	01.0	Initial release.
January 2008	01.1	Removed Generating Split Bitstream Files for Multiple SPI Flash Programming text section.
		Added Changing the SPI Flash Start Address Index screen shot.