

## Introduction

One requirement for designers using FPGA devices is the ability to determine the power considerations and consumption for a particular device used on a board. This technical note provides users with detailed power considerations, such as sequencing, along with an explanation of how to use the Power Calculator available in the ispLEVER<sup>®</sup> software tool to calculate power consumption of LatticeSC<sup>™</sup> devices. General guidelines to reduce power consumption are also discussed.

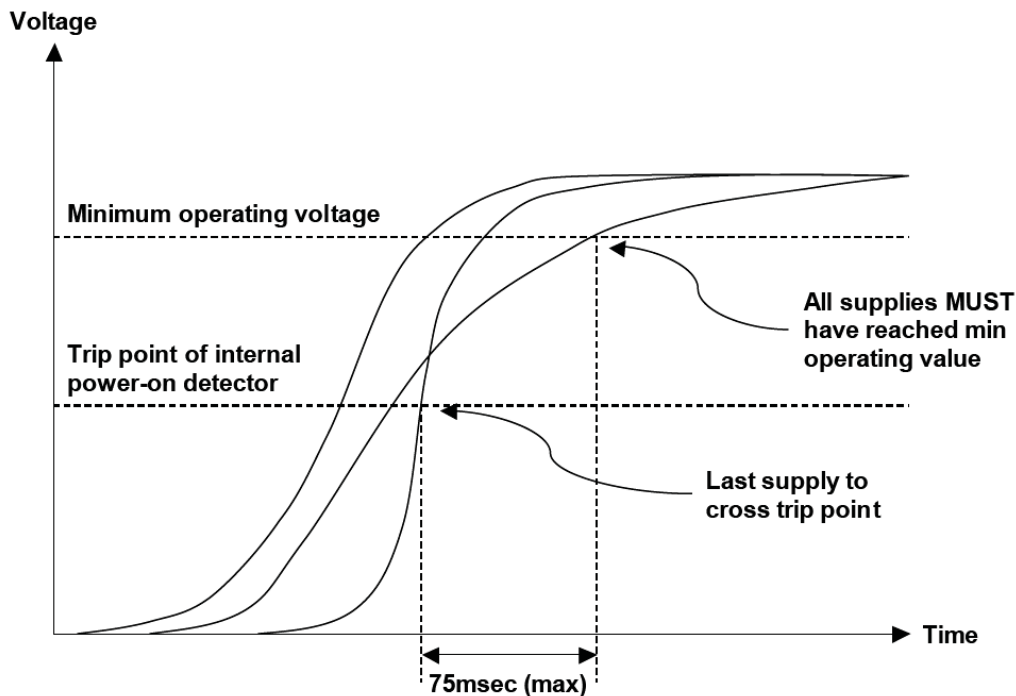
## Power Supply Sequencing

### Power-Up Sequencing

When using LatticeSC devices in hot-socketing applications where input signals may be at a higher level than the  $V_{CCIO}$  of the bank, high power supply currents and high input pin currents may flow unless the following power-up conditions are met:

- All power supplies in the following group must reach their minimum operating value within 75 msec after the time that the last power supply in the group crosses the trip point of the internal power-up detector:  $V_{CC}$ ,  $V_{CC12}$ ,  $V_{CCAUX}$ ,  $V_{CCJ}$ ,  $V_{CCIO1}$ ,  $V_{CCIO2}$ ,  $V_{CCIO3}$ ,  $V_{CCIO4}$ ,  $V_{CCIO5}$ ,  $V_{CCIO6}$  and  $V_{CCIO7}$ .

**Figure 8-1. Power Sequencing for LatticeSC Devices**



Note that the SERDES power supplies are NOT included in this group of power supplies that must come up within 75 msec.

If this requirement is not met and input signals are higher than  $V_{CCIO}$ , high power supply currents (which could be hundreds of mA) and high input pin currents will flow. This can affect connected buses.

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In a non-hot-socketing application, the outputs of the driving device will usually be powered from the same supply as the LatticeSC  $V_{CCIO}$ , so the input signals will usually be less than or equal to  $V_{CCIO}$ .

All of the voltages in the group above are monitored by the LatticeSC device and therefore must be powered up initially. They should not be left undriven or tied to ground.

After initialization is complete, if  $V_{CC}$ ,  $V_{CC12}$ ,  $V_{CCAUX}$  or  $V_{CCIO1}$  drops below the power-down trip point, the device will reset. However,  $V_{CCJ}$  and any of  $V_{CCIO[7:2]}$  can be removed without resetting the device after initialization is complete.

The minimum and maximum trip points for each power supply are listed in Table 8-1. The important values are minimum trip point for power-up and maximum trip point for power-down.

**Table 8-1. LatticeSC Power-Up and Power-Down Trip Points**

Supply	Power-Up Trip Point		Operating Range	Units
	Min.	Max.		
$V_{CC}$	0.50	0.65	1.2 (1.0) $\pm 5\%$	V
$V_{CC12}$	0.50	0.65	1.2 $\pm 5\%$	V
$V_{CCAUX}$	0.95	2.0	2.5 $\pm 5\%$	V
$V_{CCIO[1]}$	0.50	1.0	1.2/1.5/1.8/2.5/3.3 $\pm 5\%$	V
$V_{CCIO[7:2]}$	0.50	1.0	1.2/1.5/1.8/2.5/3.3 $\pm 5\%$	V
$V_{CCJ}$	0.50	1.0	1.8/2.5/3.3 $\pm 5\%$	V

**Power-Down Sequencing**

During power-down, power should be removed from one of the supplies  $V_{CC}$ ,  $V_{CC12}$  or  $V_{CCAUX}$  first to ensure that no high currents are seen on the input pins as the other  $V_{CCIO}$  supplies are removed. This only applies when input signals are still being driven, as in hot-socketing applications.

For non-hot-socketing applications, the input signals are likely to be powered from the same supply as  $V_{CCIO}$ , so the input signals will usually be less than or equal to  $V_{CCIO}$  during power-down.

**Additional Requirements for VCC and VCC12 Sequencing**

The  $V_{CC12}$  power supply must always be higher than  $V_{CC}$  or if lower should always be within 150 mV of  $V_{CC}$ . For 1.2V operation on  $V_{CC}$ , both the  $V_{CC}$  and  $V_{CC12}$  supplies are typically sourced by the same board level 1.2V power supply. Therefore, sequencing will not be an issue.

**Power Sequencing Suggestions**

To prevent high power supply and input pin currents during power-up, all supplies should have a ramp up time of 75 msec or less to reach their minimum operating voltage.

To prevent high power supply and input pin currents during power-down, power should be removed from one or more of  $V_{CC}$ ,  $V_{CC12}$  or  $V_{CCAUX}$  before power is removed from any  $V_{CCIO}$  or  $V_{CCJ}$ .

**Power Calculation Hardware Assumptions**

The power consumption for the device can be coarsely broken down into the DC portion and the AC portion.

The DC Power (or the Static power consumption) is the total power consumption of the used and unused resources. These components are fixed for each resource used and depend upon the number of resource units utilized. The DC component also includes the static power dissipation for the unused resources of the device.

The AC portion of power consumption, associated with the used resources, is the dynamic part of the power consumption. The AC power dissipation is directly proportional to the frequency at which the resource is running and the number of resource units used.

## Power Calculation Equations

The power equations used in the Power Calculator are listed below:

Total DC Power (Resource)

$$\begin{aligned}
 &= \text{Total DC Power of Used Portion} + \text{Total DC Power of Unused Portion} \\
 &= [\text{DC Leakage per resource when Used} * N_{\text{RESOURCE}}] \\
 &\quad + [\text{DC Leakage per resource when Unused} * (N_{\text{TOTAL RESOURCE}} - N_{\text{RESOURCE}})]
 \end{aligned}$$

Where:

$N_{\text{TOTAL RESOURCE}}$  is the total number of resources in a device  
 $N_{\text{RESOURCE}}$  is the number of resources used in the design

The total DC power consumption for all the resources in the design data is called Quiescent Power in the Power Calculator.

AC Power is governed by the following equation:

Total AC Power (Resource)

$$= K_{\text{RESOURCE}} * f_{\text{MAX}} * AF_{\text{RESOURCE}} * N_{\text{RESOURCE}}$$

Where:

$N_{\text{RESOURCE}}$  is the number of resources used in the design  
 $K_{\text{RESOURCE}}$  is the power constant for the resource (in mW/MHz)  
 $f_{\text{MAX}}$  is the maximum frequency at which the resource is running (in MHz)  
 $AF_{\text{RESOURCE}}$  is the activity factor for the resource group (as a percentage of switching frequency)

For example, the power consumption of the LUT is calculated in the following equation:

Total AC Power (LUT)

$$= K_{\text{LUT}} * f_{\text{MAX}} * AF_{\text{LUT}} * N_{\text{LUT}}$$

Where:

$N_{\text{LUT}}$  is the number of LUTs used in the design  
 $K_{\text{LUT}}$  is the power constant for the LUTs (in mW/MHz). This power constant is different depending upon the mode in which the SLICE is configured: Logic, Ripple or RAM.  
 $f_{\text{MAX}}$  is the maximum frequency of the LUT clock (in MHz)  
 $AF_{\text{LUT}}$  is the activity factor for the LUT (as a percentage of switching frequency)

Another example is the power consumption of the EBR block which is calculated below.

Total AC Power (EBR)

$$= K_{\text{EBR}} * f_{\text{MAX}} * AF_{\text{EBR}} * N_{\text{EBR}}$$

Where:

$N_{\text{EBR}}$  is the number of EBR blocks used in the design  
 $K_{\text{EBR}}$  is the power constant for the EBR blocks (in mW/MHz)  
 $f_{\text{MAX}}$  is the maximum frequency of the EBR clock (in MHz)  
 $AF_{\text{EBR}}$  is the activity factor for the read and write ports of the EBR (as a percentage of switching frequency)

Also note that the Slice can be configured in the Logic, Ripple or Distributed RAM modes. Each of these modes has different power constants/power coefficients. In general, though, the equations stay the same.

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The AC power of some of the dedicated blocks such as PCS, SERDES or MACO™ can be calculated using the following equation.

$$\begin{aligned} \text{Total AC Power (Dedicated Resource)} \\ = K_{\text{RESOURCE}} * f_{\text{MAX}} * N_{\text{RESOURCE}} \end{aligned}$$

Where:

$N_{\text{RESOURCE}}$	is the number of resources used in the design
$K_{\text{RESOURCE}}$	is the power constant for the resource (in mW/MHz)
$f_{\text{MAX}}$	is the maximum frequency at which the resource is running (in MHz)

## Activity Factor Calculation

Activity Factor % (or AF %) is defined as the percentage of frequency (or time) that a signal is active or toggling of the output.

Most of the resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users must provide this value as a percentage under the AF% column in the Power Calculator tool.

The AF% is applicable to the PFU, Routing, Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which I/Os toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the Output is defined as the following equation.

$$\text{Toggle Rate (MHz)} = 1/2 * f_{\text{MAX}} * \text{AF\%}$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% in case of other resources.

Although it is possible to calculate the AF for each routing resource, output or PFU, this involves in-depth calculations. For example, in a 16-bit counter, the LSB node of the 16-bit counter is switching every clock rising edge for an Activity Factor of 1. The second node is switching every other clock rising edge that corresponds to an Activity Factor of 1/2. The third node is switching every fourth clock rising edge for an Activity Factor of 1/4. The series for the sequence of 16 nodes is  $1 + 1/2 + 1/4 + 1/8 + 1/16 + \dots + 1/2^{15}$  converges to 2. Assuming a sum of 2 for the counter, divide by the total number of nodes (16) to measure the average AF per counter of  $2/16 = 0.125$ .

The general recommendation for a design occupying roughly 30% to 70% of the device is that the AF% used should be between 15% to 25%. This is an average value that can be seen most of the design. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

## Ambient and Junction Temperature and Airflow

A common method for characterizing a packaged device's thermal performance is with "Thermal Resistance", or  $\theta$ . For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are  $\theta_{JA}$ , Thermal Resistance Junction-to-Ambient (in °C/W) and  $\theta_{JC}$ , Thermal Resistance Junction-to-Case (also in °C/W). Another factor is  $\theta_{JB}$ , Thermal Resistance Junction-to-Board (in °C/W).

Knowing the reference (i.e. ambient, case or board) temperature, the power and the relevant  $\theta$  value, the junction temperature can be calculated as follows.

$$T_J = T_A + \theta_{JA} * P \quad (1)$$

$$T_J = T_C + \theta_{JC} * P \quad (2)$$

$$T_J = T_B + \theta_{JB} * P \quad (3)$$

Where  $T_J$ ,  $T_A$ ,  $T_C$  and  $T_B$  are the Junction, Ambient, Case (or Package) and Board temperatures (in °C) respectively.  $P$  is the total power dissipation of the device.

$\theta_{JA}$  is commonly used with natural and forced convection air-cooled systems.  $\theta_{JC}$  is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And  $\theta_{JB}$  applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the Ambient Temperature (°C) to calculate the Junction Temperature (°C) based on the  $\theta_{JA}$  for the targeted device, per equation 1 above. Users can also provide the Airflow values (in LFM) to get a more accurate value of the Junction temperature.

## Power Calculator

Power Calculator is a powerful tool which allows users to estimate power consumption at three different levels:

### 1. Estimate of the Utilized Resources

This is the first level of estimation. In this stage, the user provides estimates of device usage in the Power Calculator Wizard and the tool provides a rough estimate of the power consumption.

### 2. Post Place and Route Design

This is the second level of estimation. In this stage, the user's design has been placed and routed in the ispLEVER design tool. This provides a more accurate approach, as the exact device utilization information is imported from the placed and routed netlist (NCD) file. During this stage, the user is required to provide frequencies ( $f_{MAX}$ ), activity factors (AF%) and the toggle rate (TR in MHz).

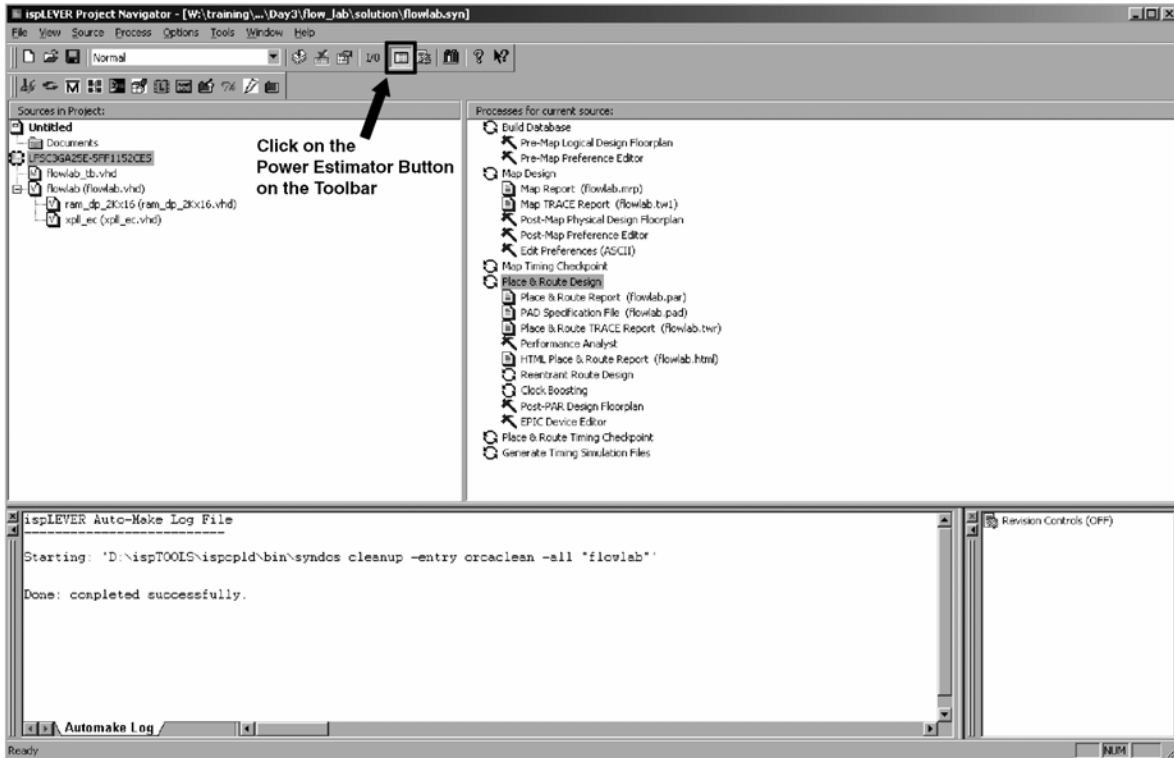
### 3. Post Place and Route and Post Simulation

The third level of power calculation takes the power calculations from the second stage and also allows users to import the post-simulation file (VCD file, output of ModelSim®), the trace report file (TWR file) or the preference file (PRF file), as generated by ispLEVER. These files provide the data for the frequency ( $f_{MAX}$ ), activity factors (AF%), and toggle rate (TR in MHz) cells in Power Calculator.

## Starting the Power Calculator

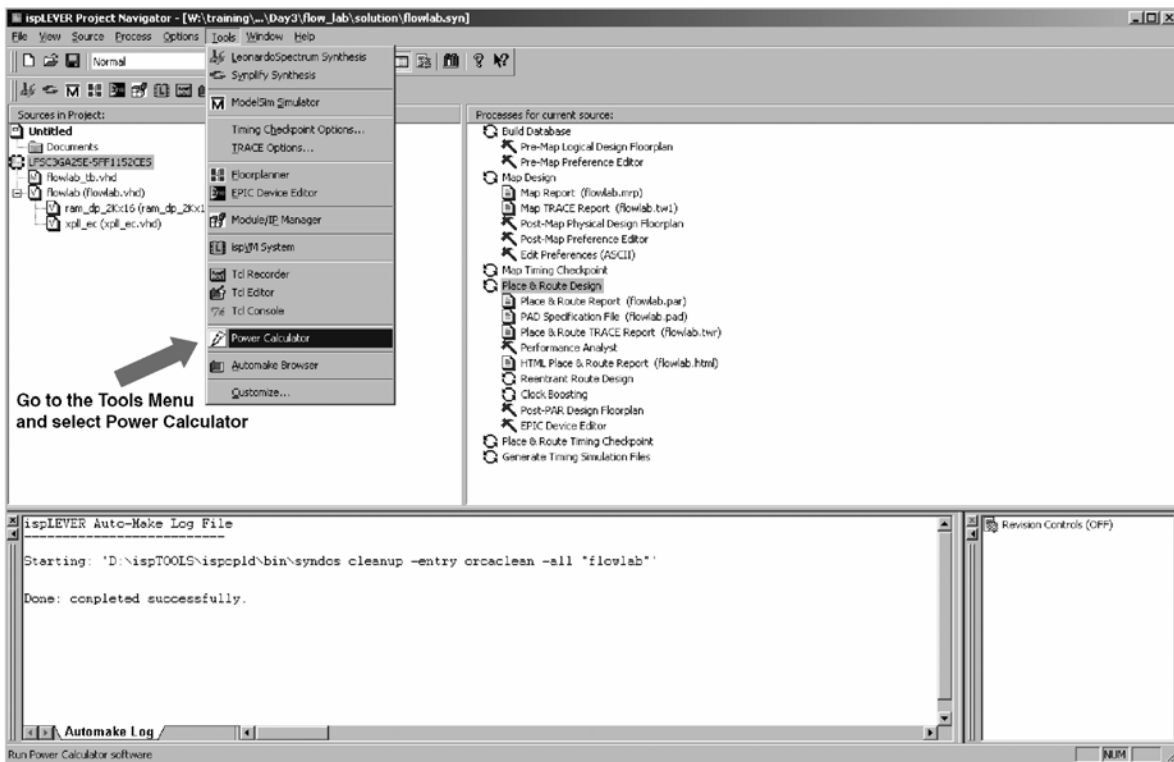
Users can launch the Power Calculator by one of two methods. The first method is to click the Power Calculator button in the toolbar as shown in Figure 8-2.

Figure 8-2. Starting Power Calculator from the Toolbar



Alternatively, users can launch Power Calculator by going to the **Tools** menu and selecting **Power Calculator** as shown in Figure 8-3.

Figure 8-3. Starting Power Calculator from Tools Menu

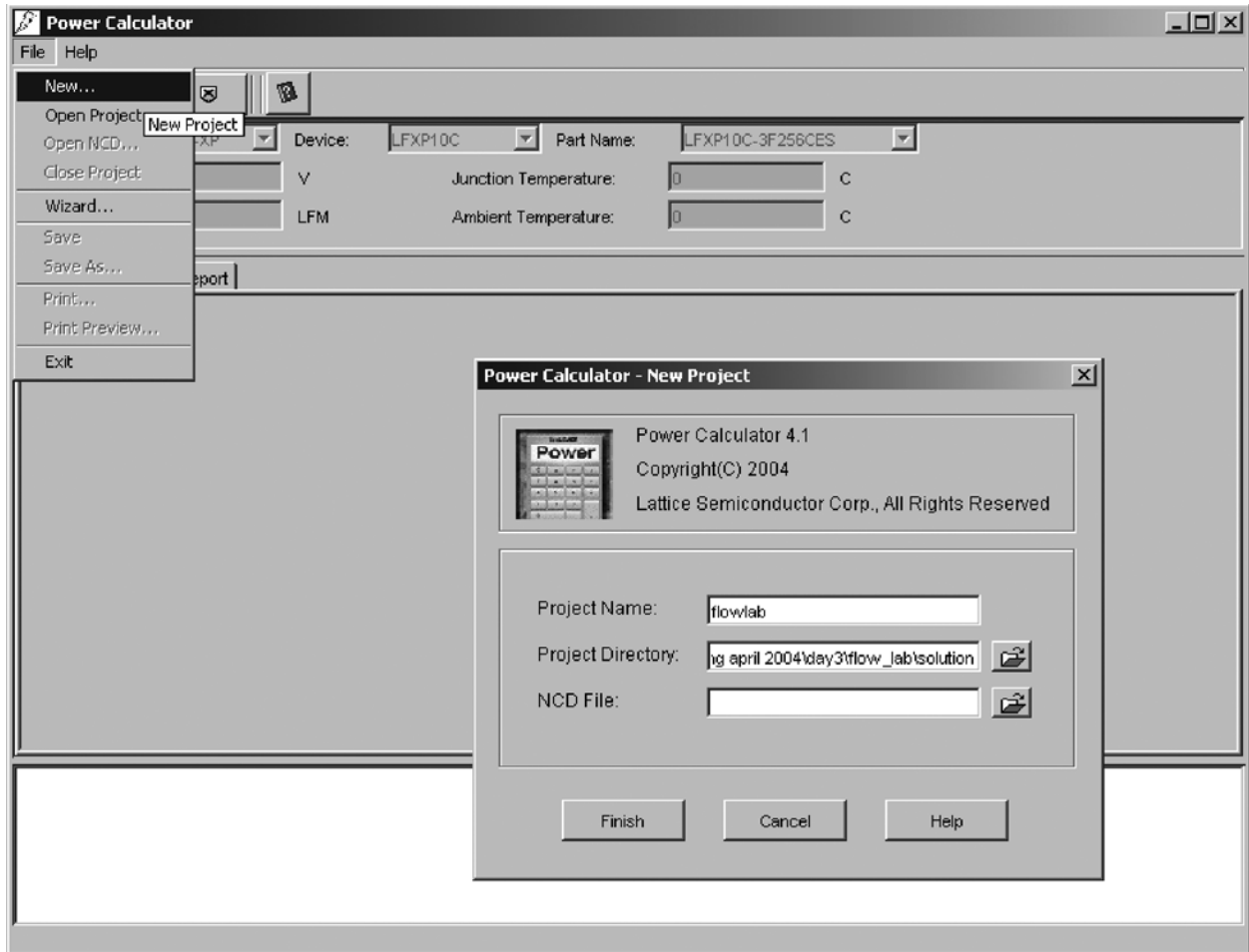


Note: Power Calculator does not support some of Lattice's older devices. The toolbar button and menu item are only present when supported devices are selected.

### Creating a Power Calculator Project

Once the Power Calculator has been started, users will see the Power Calculator window. Click **File -> New** to get to the Start Project window as shown in Figure 8-4.

Figure 8-4. Power Calculator Start Project Window (Create New Project)



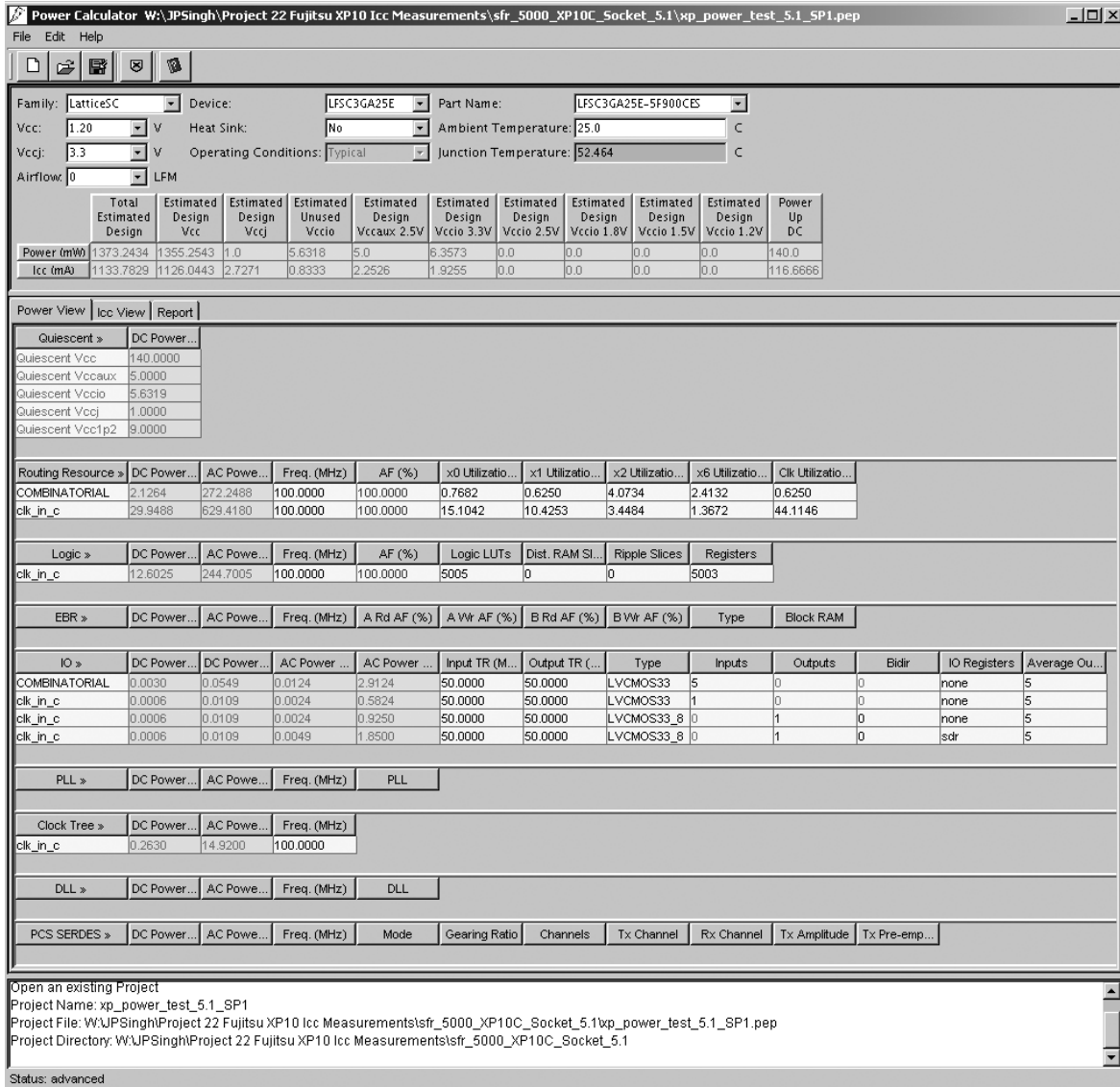
The Start Project Window is used to create a new Power Calculator Project (\*.pep project). Three pieces of data must be input in the Start Project Window.

1. The **Power Calculator Project Name** by default is same as the Project Navigator project name. Users can change it if they desire.
2. **Project Directory** is where the Power Calculator project (\*.pep) file will be stored. By default, it is stored in the main project folder.
3. Input an **NCD File** (if available) or users can browse to the NCD file in a different location.

Power Calculator Main Window

The main Power Calculator window is shown in Figure 8-5.

Figure 8-5. Power Calculator Main Window (Type View)



The top of the window shows information regarding device family, device and part number as it appears in the Project Navigator.

Power calculation depends upon a number of other voltage supplies in addition to the core voltage supply,  $V_{CC}$ .  $V_{CCIO}$  voltage supplies for the I/Os also contribute to the final power consumption of the device, and other voltage supplies such as  $V_{CCAUX}$  and  $V_{CCJ}$  also affect the final power consumption.

The present version of the Power Calculator tool uses the default values of these voltage supplies. For other Power Calculator assumptions, refer to the Power Calculator Assumptions section at the end of this document.

The top pane of the Power Calculator main window also includes information such as the Junction Temperature ( $^{\circ}C$ ), which is calculated as a function of the Ambient Temperature ( $^{\circ}C$ ), also included here. Air flow is also included.



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Upon opening up the Power Calculator, the second and third columns, shaded blue, provide the DC (static) and AC (dynamic) power consumption, respectively.

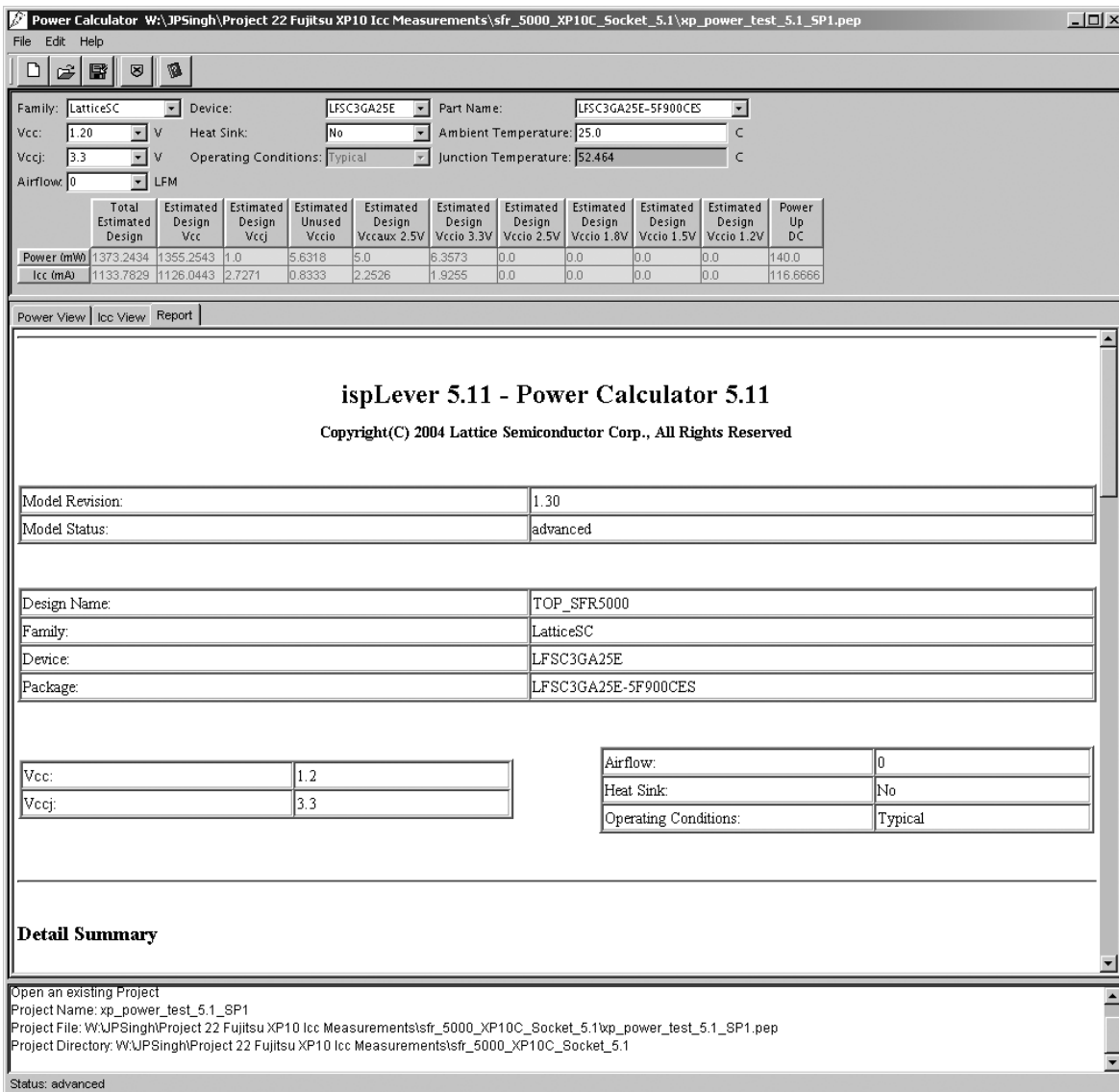
The first row shows the Quiescent power, which is the DC power of a device with no resource utilization.

The columns to the right of these, shaded yellow, show factors like  $f_{MAX}$ , resource utilization, Activity Factors (AF%) etc. that affect the static and dynamic power consumptions.

Power estimation is reported in two ways using the tabs:

1. **Type View**, the tabular format shown in Figure 8-5
2. **Power Report**, a text-based power estimation report shown in Figure 8-6

Figure 8-6. Power Calculator Main Window (Power Report View)

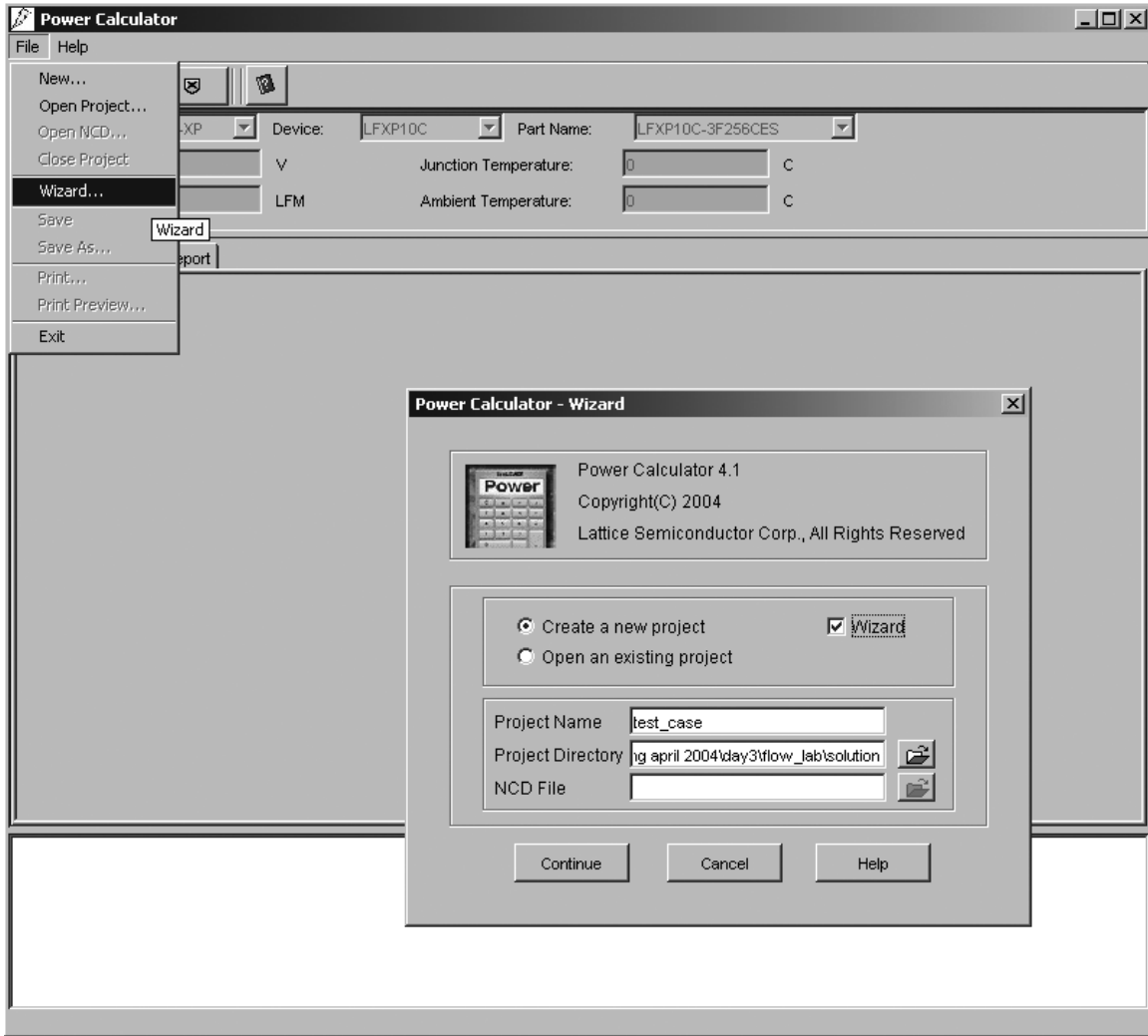


Power Calculator Wizard

The Power Calculator Wizard allows users to estimate the power consumption of the design. Because this estimation is done before a design is created, users must understand the logic requirements of the design. The Wizard allows users to provide these parameters and then estimates the power consumption of the device.

To start the Power Calculator in the Wizard mode, go to **File -> Wizard**. Alternatively, you can click on the Wizard button to get the Power Calculator - Wizard window, as shown in Figure 8-6. Select the option **Create a new Project** and check the **Wizard** check box in the Power Calculator Start Project window. Users must provide the project name and the project folder and click **Continue**. Since this is power estimation before the actual design, no NCD file is required.

Figure 8-7. Power Calculator Start Project Window (Using the New Project Window Wizard)



In the next screen, as shown in Figure 8-7, users select the device family, device and appropriate part number. After making the proper selections, click **Continue** (see Figure 8-8).

**Figure 8-8. Power Calculator Wizard Mode Window - Device Selection**

In the following screens (Figures 9, 10, 11, 12 and 13) the users can select additional resources such as I/O types, provide a clock name and the frequency at which the clock is running, and other parameters, by selecting the appropriate resource in the pull-down Type menu:

1. Routing Resources
2. Logic
3. EBR
4. I/O
5. PLL
6. Clock Tree
7. DLL

The number in these windows refers to the number of clocks and the index corresponds to each of the clocks. By default, the clock names are clk\_1, clk\_2, and so on. Clock names can be changed by typing in the Clock Name text box. For each clock domain and resource, parameters such as frequency, activity factor, etc. can be specified. User must click the **Create** button for each clock-driven resource to include the parameters they have specified for it in the final window.

These parameters are then used in the **Power Type View** window (Figure 8-14) which is visible after clicking on **Finish**.

Figure 8-9. Power Calculator Wizard Mode Window, Resource Specification: Logic

The screenshot shows the 'Power Calculator - Wizard' window with the following settings:

- Type of Resource: Logic
- Number of Clock Domains: 2
- Clock Domain: 2
- Clock Name: clk\_2
- Frequency (MHz): 50
- Activity Factor (%): 20
- Number of LUTs in Logic Mode: 3000
- Number of Slices in Dist. RAM Mode: 200
- Number of Slices in Ripple Mode: 0
- Number of Registers in all Mode: 0

Buttons at the bottom: Finish, Back, Cancel, Help.

Figure 8-10. Power Calculator Wizard Mode Window, Resource Specification: EBR

The screenshot shows the 'Power Calculator - Wizard' window with the following settings:

- Type of Resource: EBR
- Number of Clock Domains: 1
- Clock Domain: 1
- Clock Name: clk\_1
- Frequency (MHz): 70.0
- Port A Rd Activity Factor (%): 100.0
- Port A Wr Activity Factor (%): 100.0
- Port B Rd Activity Factor (%): 100.0
- Port B Wr Activity Factor (%): 100.0
- Type: RAM\_DQ
- Block RAM: 3

Buttons at the bottom: Finish, Back, Cancel, Help.

Figure 8-11. Power Calculator Wizard Mode Window, Resource Specification: PLL

The screenshot shows the 'Power Calculator - Wizard' dialog box. The 'Type of Resource' dropdown is set to 'PLL'. The 'Number of Clock Domains' is set to '1' with a 'Create' button next to it. The 'Clock Domain' dropdown is set to '1'. The 'Clock Name' text box contains 'clk\_1'. The 'Frequency (MHz)' text box contains '70.0'. The 'Number of PLL' text box contains '1'. At the bottom, there are four buttons: 'Finish', 'Back', 'Cancel', and 'Help'.

Note: The frequency specified must be the VCO frequency.

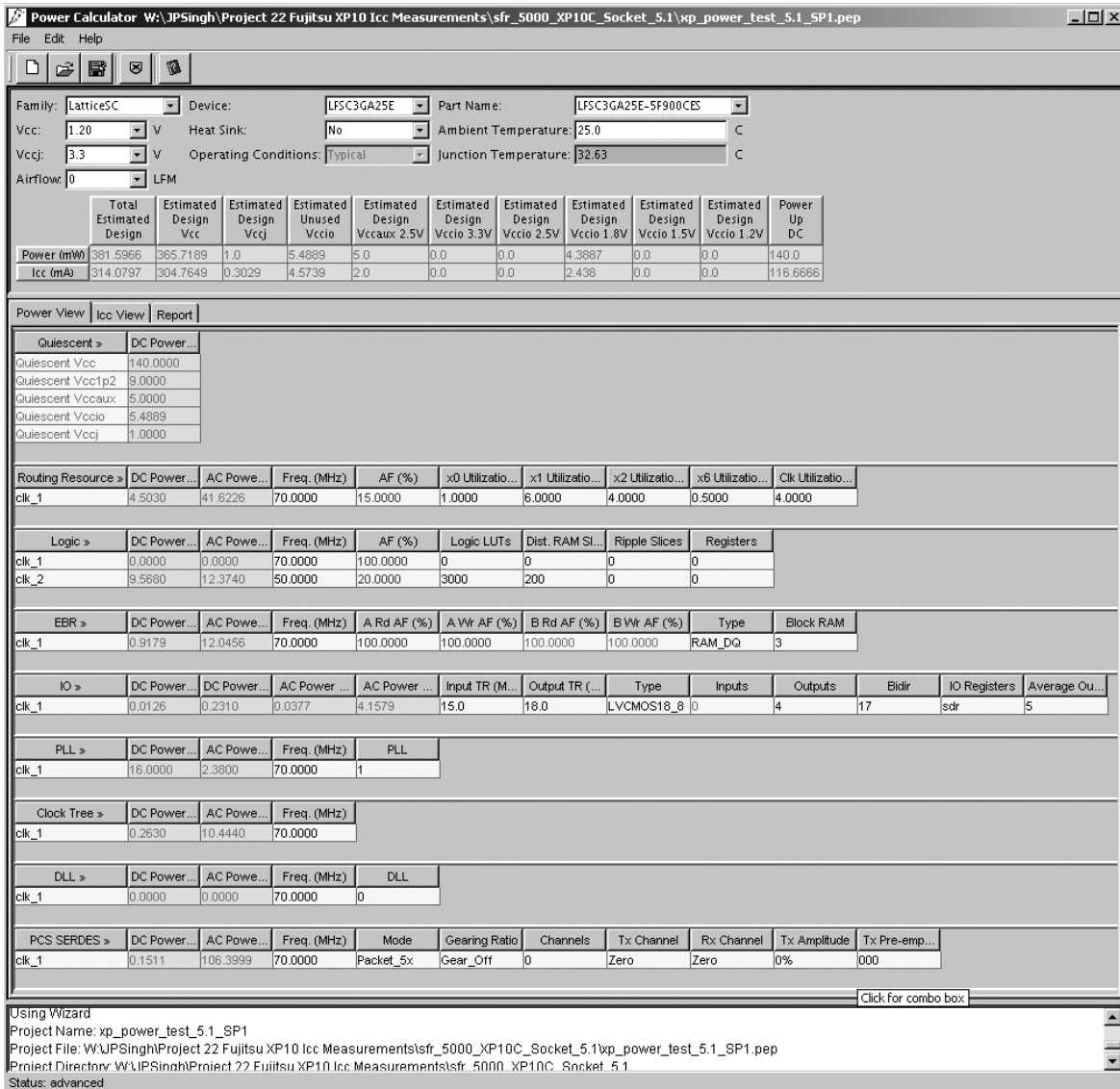
Figure 8-12. Power Calculator Wizard Mode Window, Resource Specification: Routing Resources

The screenshot shows the 'Power Calculator - Wizard' dialog box. The 'Type of Resource' dropdown is set to 'Routing Resource'. The 'Number of Clock Domains' is set to '1' with a 'Create' button next to it. The 'Clock Domain' dropdown is set to '1'. The 'Clock Name' text box contains 'clk\_1'. The 'Frequency (MHz)' text box contains '70'. The 'Activity Factor (%)' text box contains '15'. The 'Utilization for x0 (%)' text box contains '1'. The 'Utilization for x1 (%)' text box contains '6'. The 'Utilization for x2 (%)' text box contains '4'. The 'Utilization for x6 (%)' text box contains '0.5'. The 'Utilization for Clkmux (%)' text box contains '4'. At the bottom, there are four buttons: 'Finish', 'Back', 'Cancel', and 'Help'.

Figure 8-13. Power Calculator Wizard Mode Window, Resource Specification: I/O

The screenshot shows a dialog box titled "Power Calculator - Wizard" with a close button (X) in the top right corner. The dialog is divided into two main sections. The top section contains "Type of Resource:" with a dropdown menu set to "IO", "Number of Clock Domains:" with a text input field containing "1", and a "Create" button. The bottom section contains "Clock Domain:" with a dropdown menu set to "1", "Clock Name:" with a text input field containing "clk\_1", "Input Toggle Rate (MHz):" with a text input field containing "15", "Output Toggle Rate (MHz):" with a text input field containing "18", "Type:" with a dropdown menu set to "LVCMOS18\_8", "Number of Inputs:" with a text input field containing "0", "Number of Outputs:" with a text input field containing "4", "Number of Bidir IOs:" with a text input field containing "17", "IO Registers:" with a dropdown menu set to "sdr", and "Average Output Load (pF):" with a text input field containing "5". At the bottom of the dialog are four buttons: "Finish", "Back", "Cancel", and "Help".

Figure 8-14. Power Calculator Wizard Mode, Main Window



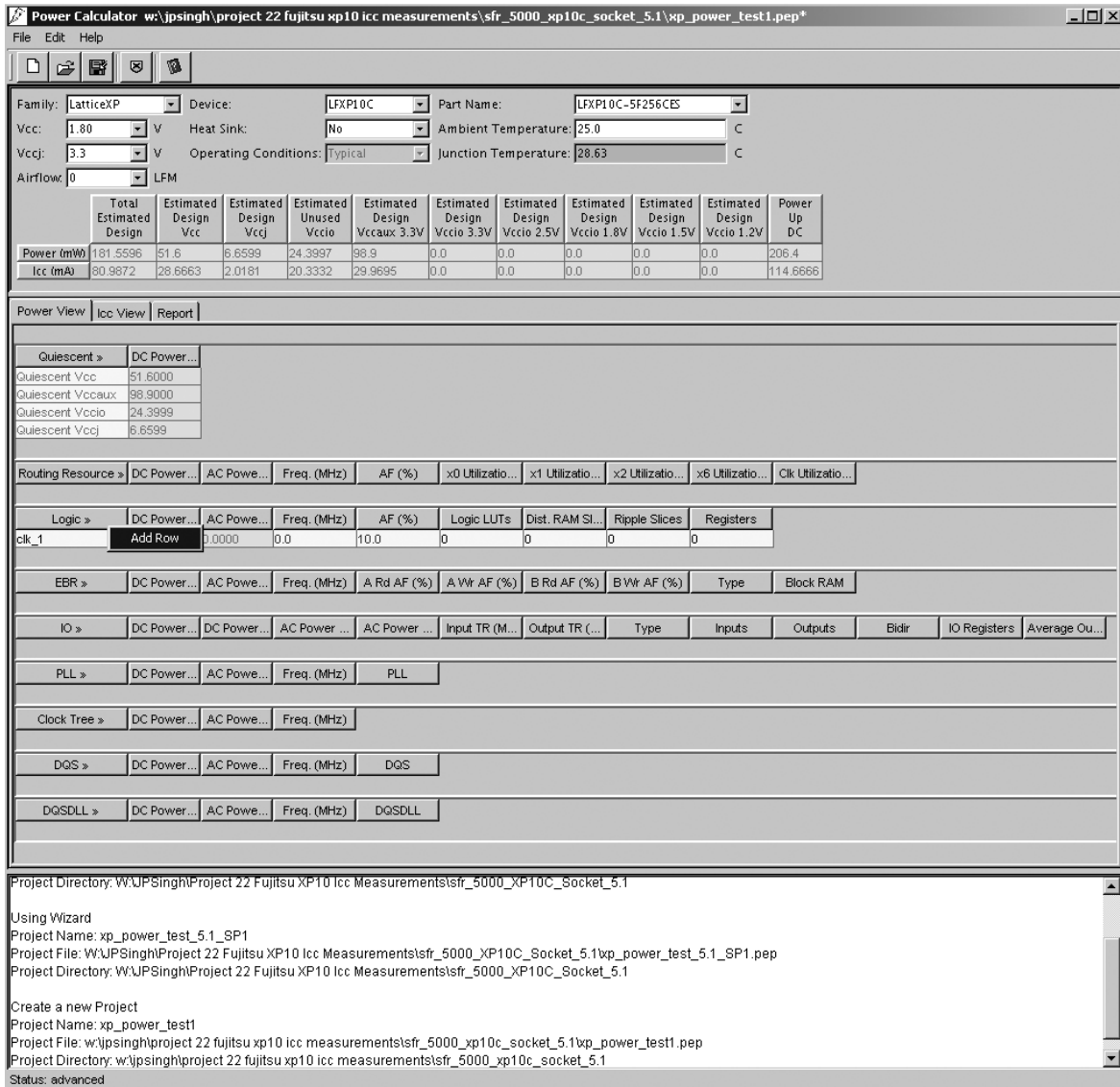
### Power Calculator – Creating a New Project Without the NCD File

Users can start a new project without the NCD file, either by using the Wizard (as discussed above) or by selecting the **Create a New Project** option in **Power Calculator - Start Project**. The project name and project directory must be provided. After clicking **Continue**, the Power Calculator main window will be displayed.

However, in this case there are no resources added. The power estimation row for routing resources is always available in the Power Calculator. Additional information such as Slice, EBR, I/O, PLL and clock tree utilization must be added to calculate the power consumption.

For example, to add logic resources, right-click on **Logic >>** and select **Add** in the menu, as shown in Figure 8-15.

Figure 8-15. Power Calculator Main Window – Adding Resources



This adds a new row for the logic resource utilization with clock domain as clk\_1.

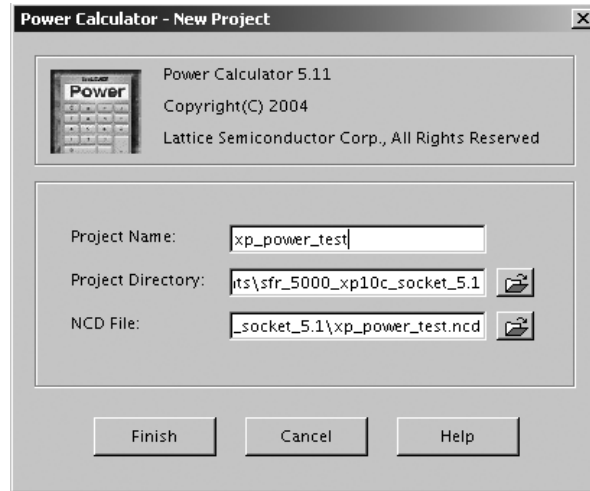
Similarly, other resources such as EBR, I/Os, PLLs and routing, can also be added. Each of these resources is for AC power estimation and categorized by clock domains.

### Power Calculator – Creating a New Project With the NCD File

If the post place and routed NCD file is available, Power Calculator can use this file to import accurate information about the design data and resource utilization to be used to calculate power. When the Power Calculator is started, the NCD file is automatically placed in the **NCD File** option, if available in the project directory. Otherwise, the user can browse to the NCD file in the Power Calculator.

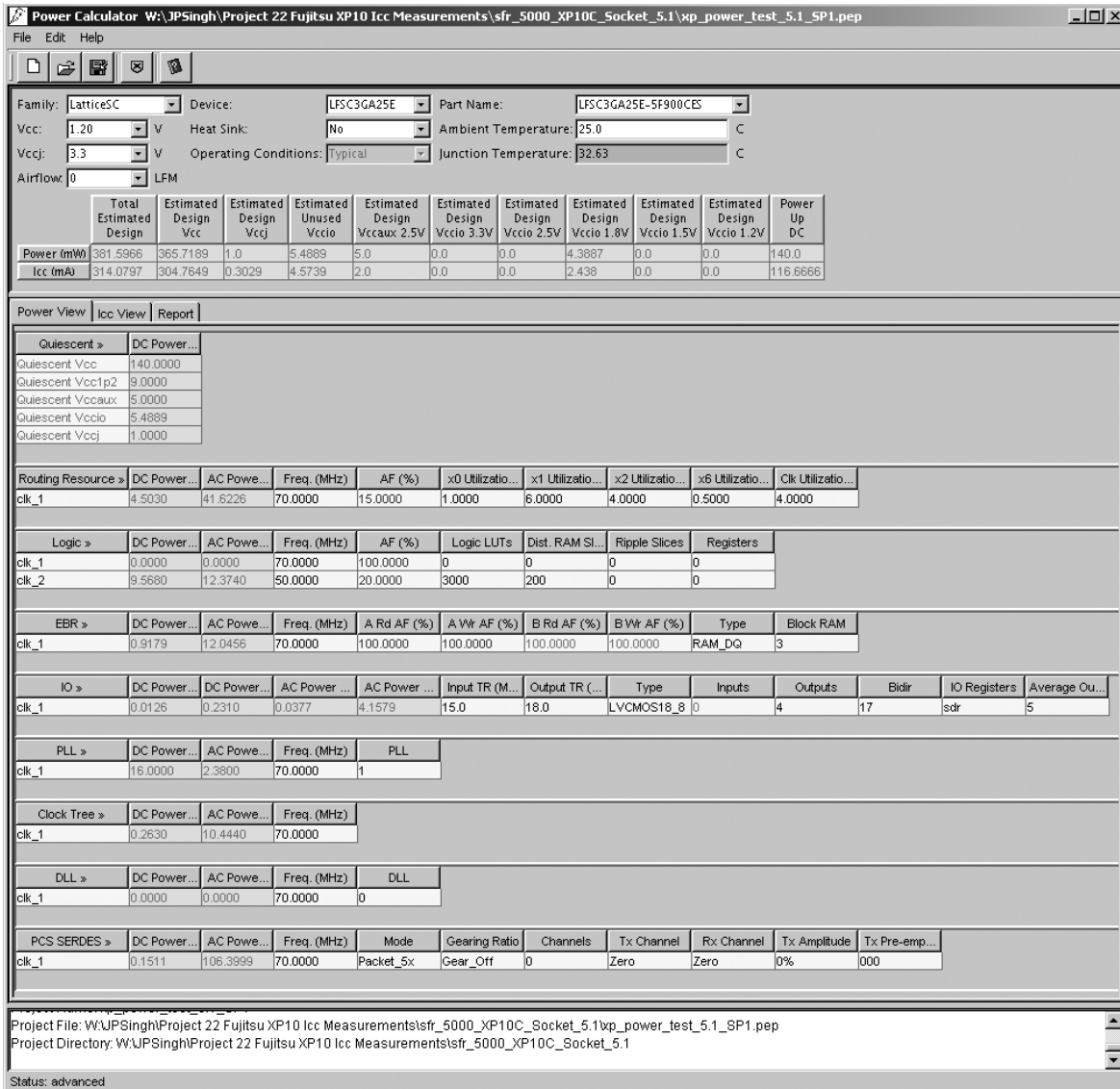


**Figure 8-16. Power Calculator Start Project Window with Post-P&R NCD File**



The information from the NCD file is automatically inserted into the correct rows and Power Calculator uses the Clock names from the user's design as shown in Figure 8-17.

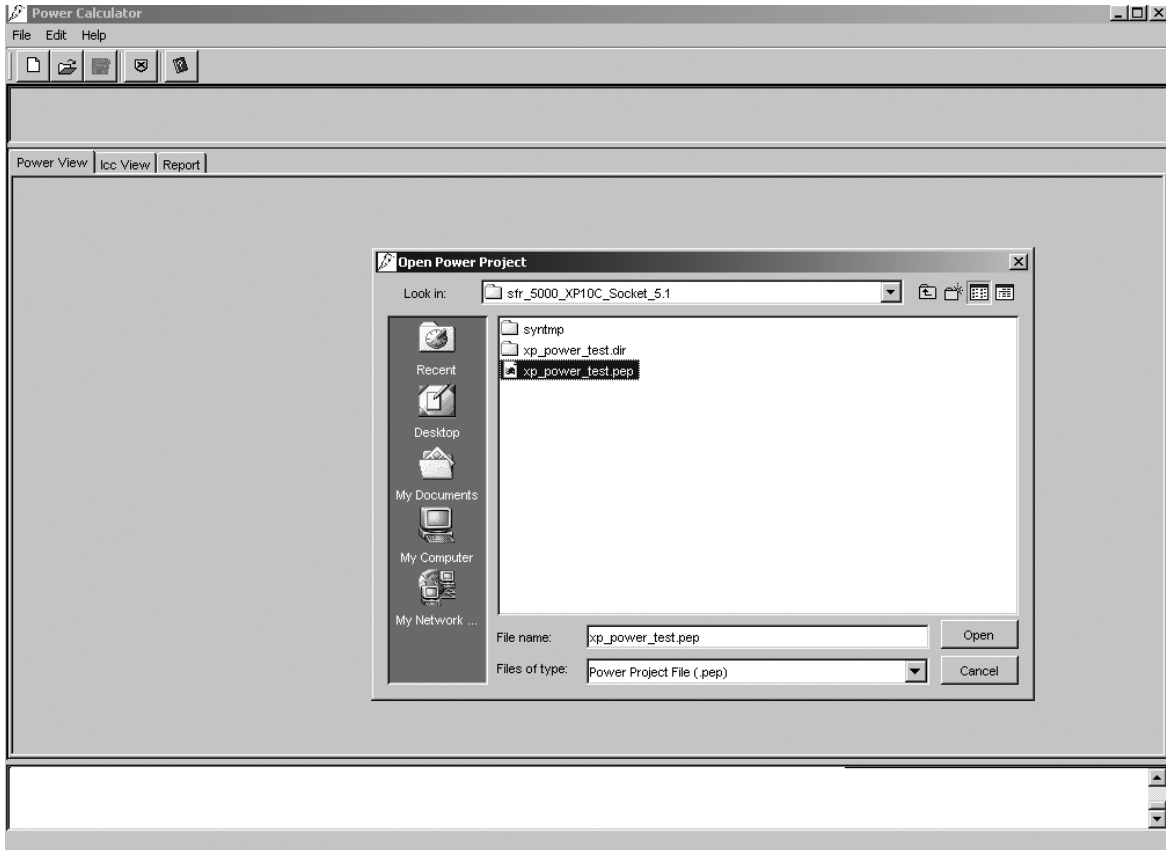
Figure 8-17. Power Calculator Main Window with Resource Utilization Picked Up From the NCD File



### Power Calculator – Open Existing Project

The **Power Calculator - Start Project** window also allows users to open an existing project. Select the option **Open Existing Project** and browse to the \*.pep project file and click **Continue**. This opens the existing project in similar windows, as discussed above (see Figure 8-18).

Figure 8-18. Opening Existing Project in Power Calculator

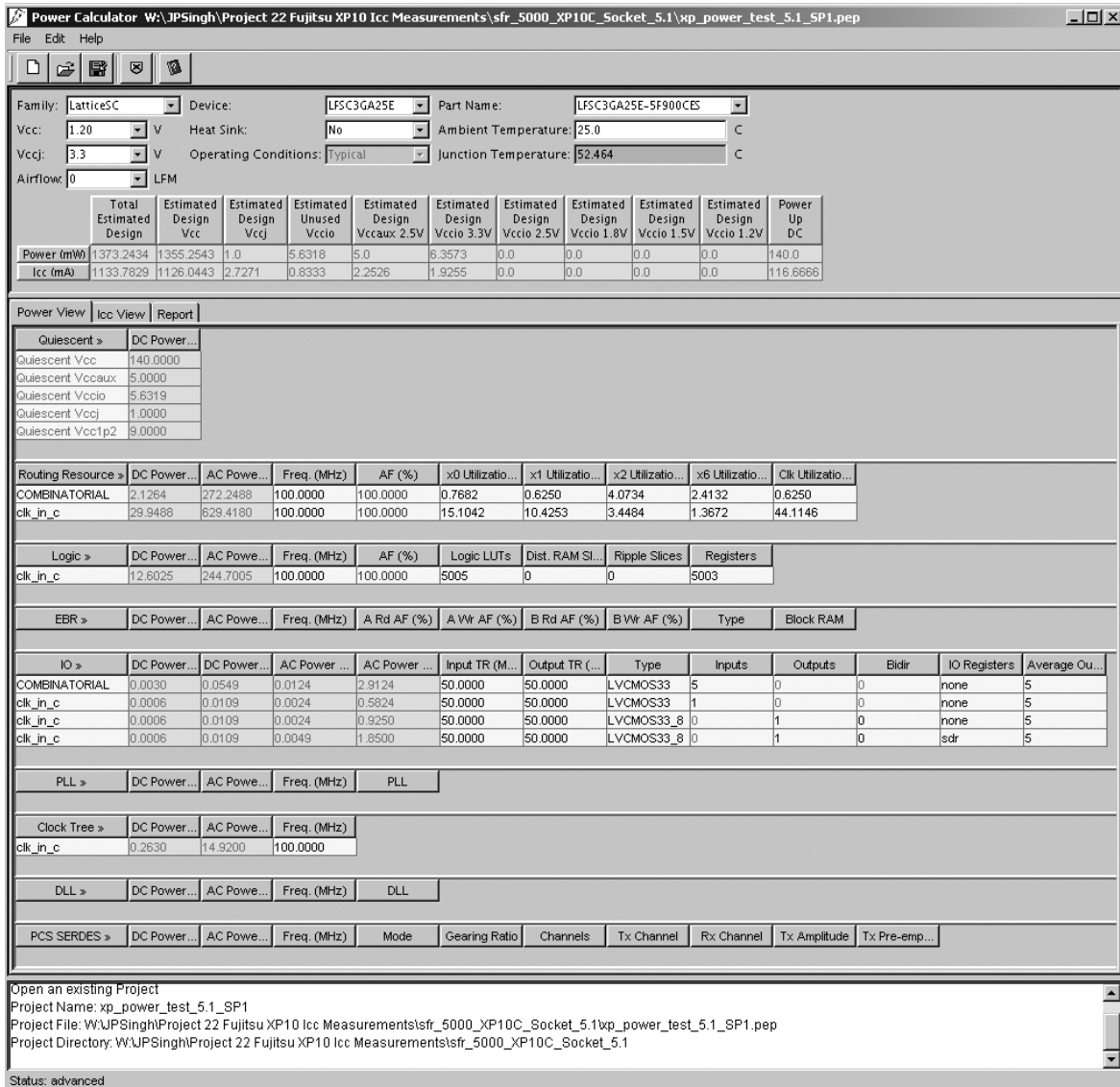


### Power Calculator – Total Power

A Power Calculator project created or opened using any of the methods discussed above allows a user to calculate the power consumption for a device running within their design.

The estimated power is indicated in the **Total** section at the bottom of the table, as shown in Figure 8-19.

Figure 8-19. Calculated Power in the Power Calculator Main Window



The second and third columns from the left indicate the DC (static) and AC (dynamic) power consumption. The total power consumption for the design can be seen in the same table by scrolling down to the row labeled **Total**.

### Power Calculator Assumptions

The following are assumptions made in the Power Calculator:

1. The Power Calculator tool is based on equations with constants based on room temperature of 25°C.
2. Users can define the Ambient Temperature ( $T_A$ ) for the device Junction Temperature ( $T_J$ ) calculation based on the power estimation.  $T_J$  is calculated from user-entered  $T_A$  and the power calculation of typical room temperature.
3. I/O power consumption is based on output loading of 5pF. Users have the ability to change this capacitive loading.
4. Power Calculator allows users to get an estimate of the power dissipation and current  $V_{CC}$ ,  $V_{CCIO}$ ,  $V_{CCJ}$  and  $V_{CCAUX}$ . Note that the power shown for  $V_{CC}$  is a combination of the power that is supplied on both

$V_{CC}$  and  $V_{CC12}$ . For  $V_{CCAUX}$ , only static  $I_{CC}$  values are provided at this time. For differential output buffers, differential input buffers and reference input buffers, the following DC bias currents are not included in the Power Calculator (needs to be added per pair for differential buffers, per pin for reference input buffers):

Typical - Differential Output Buffer: 9.5 mA (6 mA buffer mode - HyperTransport), 7.0 mA (3.5 mA mode - LVDS) or 5.5 mA (2 mA mode - RSDS).

Typical - Differential/Reference Input Mode Buffer: 3.0 mA (low power mode - single-ended reference inputs or differential inputs with common mode >600 mV at an differential input voltage of 100 mV at rates up to 2 Gbps), 5.0 mA (high power mode - full differential specification ranges for common mode up to rates of 2 Gbps).

Worst Case - Differential Output Buffer: 10.6 mA (6 mA buffer mode), 8.2 mA (3.5 mA mode) or 6.5 mA (2 mA mode). Worst Case: Differential/Reference Input Mode Buffer: 3.5 mA (low power mode), 6.0 mA (high power mode). For the Differential Output Buffer, there is also an AC component missing from the Power Calculator (both typical and worst case are equivalent):

Clock Output at 1 GHz (100% activity): 10.4 mA (6 mA buffer mode), 9.8 mA (3.5 mA mode) or 9.5 mA (2 mA mode)

PRBS 2<sup>7</sup> Data Output at 1 GHz: 5.4 mA (6 mA buffer mode), 4.8 mA (3.5 mA mode) or 5.3 mA (2 mA mode)

5. The nominal  $V_{CC}$  is used by default to calculate power consumption. Users can choose a lower or higher  $V_{CC}$  from a list of available values.
6. Power Calculator allows users to enter airflow in Linear Feet per Minute (LFM) along with the Heat Sink option to calculate the Junction Temperature.
7. The default value of the I/O types for LatticeSC devices is LVCMOS25, 8 mA. If the Power Calculator encounters a buffer type it does not understand it will issue a warning and use this buffer type.
8. The Activity Factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop changes at every clock cycle, 100% AF of a flip-flop running at 100MHz is 50MHz.
9. All of the input and output I/O pads have a dedicated programmable parallel termination to  $V_{CCIO}$ , GND or Thevenin termination to  $V_{CCIO/2}$  or to  $V_{TT}$ . All the differential input pads can also be differentially terminated on all sides of the device. In addition to differential termination, common mode differential termination is available for differential signals using the  $V_{CMT}$  node in the bank.

In general, I/O power can be calculated by splitting between input and output power dissipations.

The power dissipated by the chip I/O can be calculated by splitting the input and the output power dissipation:

$$P_{IO} = P_{IN} + P_{OUT}$$

$$= (N_{IN} * Z_{IN} * V_2 * f) + (N_{OUT} * Z_{OUT} * V_2 * f) \text{ mW}$$

- $P_{IN}$  is the total power dissipation due to input pins
- $N_{IN}$  is the number of input pins used
- $Z_{IN}$  is the average impedance of each input pin used
- $P_{OUT}$  is the total power dissipation due to output pins
- $N_{OUT}$  is the number of output pins used
- $Z_{OUT}$  is the average impedance of each output pin used

In considering the power dissipation of the I/Os, it should be noted that each termination chosen by the user has a power consumption associated with it. This would also be affected when there is an output load on the I/Os.

None of the I/O terminations found on the LatticeSC device are included in the results from the Power Calculator. These need to be added to the  $V_{CCIO}$  power that is already included per buffer using the following equations:

$$V_{TT} \text{ Termination: Power/buffer} = (V_{CCIO}/2 - 0.4V)^2 / \text{Termination Resistance}$$

Dynamically switched  $V_{TT}$  termination:

$$\text{Power/buffer} = ((V_{CCIO}/2 - 0.4V)^2 / \text{Termination Resistance}) * \% \text{ time as an input buffer}$$

$$\text{Thevenin Equivalent: Power/buffer} = ((V_{CCIO}^2) / 4x \text{ Termination Resistance}) + ((V_{CCIO} - 0.4V)^2 / 2x \text{ Termination Resistance})$$

10. The system bus is a low speed serial bus and it is always “on”. The wide data bus configuration of 32 bits with 4-bit parity supports high-bandwidth and uses the memory map. A master interface can access each of the slave peripherals on the system bus. The system bus is on during power-up and the power consumption stays constant during operation.
11. A heat sink can be included for each package. The heat sink, provided as a guide only for these devices, is an extrusion type with a maximum height of 1". This heat sink may overhang the dimensions of the package by as much as 10 mm per side to provide more surface area. Also included is a thermal bonding material that adds the following to the Theta-CA value of the heat sink: 0.2 for flip-chip packages (256 fpBGA and 900 fpBGA) and 0.6 for wirebond packages (all other packages). Users must determine the heat sink requirements for their application and provide their own Theta-CA values for the combination of the heat sink plus thermal bonding material as per the air-flow of their particular board.
12. The Power Calculator assumes that all four channels in a SERDES quad channel group are operation and that the Amplitude Boost mode is disabled.

## Managing Power Consumption

One of the most critical factors in design today is the reduction of system power consumption. A low order reduction in power consumption goes a long way, especially in hand-held devices and other modern electronics. There are several design techniques that can be used to significantly reduce overall system power consumption. Some of these include:

1. Employ power supplies efficiently. Reducing the operating voltage by operating at a lower and typical voltage rather than at the upper level reduces the power consumption of the device. For example, using the capability for the core to run at  $VCC = 1.0V$  typical saves approximately 50% core power from the higher level of  $VCC = 1.2V$ . By reducing the voltage swing of the I/Os where possible, a double-ended LVDS will have much less voltage swing as compared to the singles ended CMOS.
2. Operate within the specified package temperature limitations.
3. Use optimum clock frequency to reduce power consumption, since the dynamic power is directly proportional to the frequency of operation. Designers should determine if some portions of their design can be clocked at a lower rate to reduce power.
4. Reduce the span of the design across the device. A more closely placed design utilizes fewer routing resources and therefore less power consumption.
5. Use optimum encoding where possible. For example, a 16-bit binary counter has, on average, only 12% Activity Factor and a 7-bit binary counter has an average of 28% Activity Factor. On the other hand, a 7-bit LFSR counter toggles at an Activity factor of 50%, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, uses the least amount of power, as the Activity Factor is less than 10%.
6. Large current surges during power-up sequencing cause higher power consumption. When possible, try reducing or eliminating these spikes.
7. For hand-held and portable electronics, designers should use an efficient battery management system.

8. Minimizing operating temperatures by the following methods:
  - a. Use packages that can better dissipate heat.
  - b. Place heat sinks and thermal planes around the device on the PCB.
9. Employ airflow techniques that use mechanical airflow guides and fans (both system fans and device mounted fans).
10. Use of VTT termination in the device can save over 60% of the power required for on-chip termination versus Thevenin equivalents. If the dynamically enabled VTT termination is used and a 50% duty cycle of inputs to outputs is assumed, this power can be reduced by another 50%.
11. Use of embedded MACO blocks also reduces power. The power reduction of MACO versus the same function implemented in FPGA logic is typically greater than 50%.

## Revision History

Date	Version	Change Summary
February 2006	01.0	Initial release.
November 2006	01.1	Power Calculator Assumptions section - Updated for heatsink and V <sub>CCAUX</sub> options.
March 2007	01.2	Removed VCCPLL supply references.
		Added note after Power Calculator Wizard Mode Window, Resource Specification: PLL figure.
		Updated LatticeSC Power-Up and Power-Down Trip Points table.
		Updated Power Calculator Assumptions section.
		Updated Managing Power Consumption section.
July 2007	01.3	Document title changed to "Power Estimation and Management for LatticeSC Devices".

## Technical Support Assistance

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