LEADING FPGA ARCHITECTURES ARE MEETING THE CONNECTIVITY CHALLENGE

A Lattice Semiconductor White Paper

February 2006

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Introduction

Since their introduction nearly 20 years ago, FPGAs have grown into a multi-billion dollar segment of the semiconductor industry. Market forces and advanced technologies are converging in such a way that the future for these programmable SRAM devices remains bright. These market forces include the continuing convergence of datacom and telecom, tremendous growth in the metro space, new services and delivery options at the edge of the network and the relentless demand for overall bandwidth. As equipment vendors adjust their product portfolios to address the changing market landscape, they are confronted with a complex mix of protocols and standards that presents a true system connectivity challenge. FPGAs have always thrived at the confluence of disparate standards and technologies, and these market forces have been a boon to the FPGA industry.

In addition, TEMs (Telecom Equipment Vendors) are increasingly using off-the-shelf hardware and software solutions that have fueled the use of ASSPs at the expense of internally developed ASICs. As the role of ASSPs grew, so too did the need to bridge them to one another. FPGAs were called upon to fill the role of bridging different vendor's ASSPs to one another. Major market trends, strategic decisions at the major systems houses and dramatic improvements in FGPA technology have made FPGAs the device of choice for system connectivity.

Overview of System Connectivity

Figure 1 below summarizes the basic roles of FPGAs on a typical line card. At a high level, these basic functions are common across the major industries served by FPGAs, which include telecom, datacom and storage. Figure 1 also highlights the many interfaces and standards that FPGAs are called upon to support.

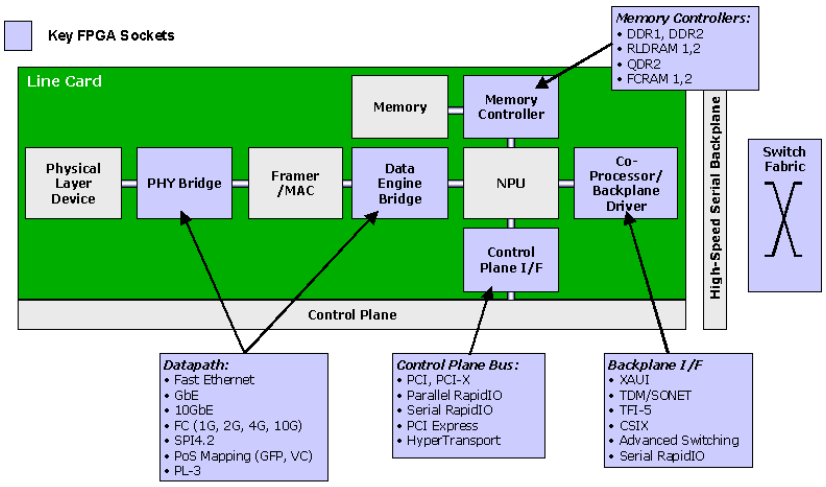


Figure 1

The System Connectivity Challenge

Today's FPGAs are asked to do much more than simple I/O bridging. As Figure 2 below illustrates, connectivity requires more than just electrical I/O support for signal integrity and clocking. Additional digital logic and portions of the link layer for certain protocols are also provided to simplify the implementation of several different high-speed parallel and serial standards. The inclusion of these standardized features into FPGA devices frees up design time that is better spent on developing "customer specific" design features.

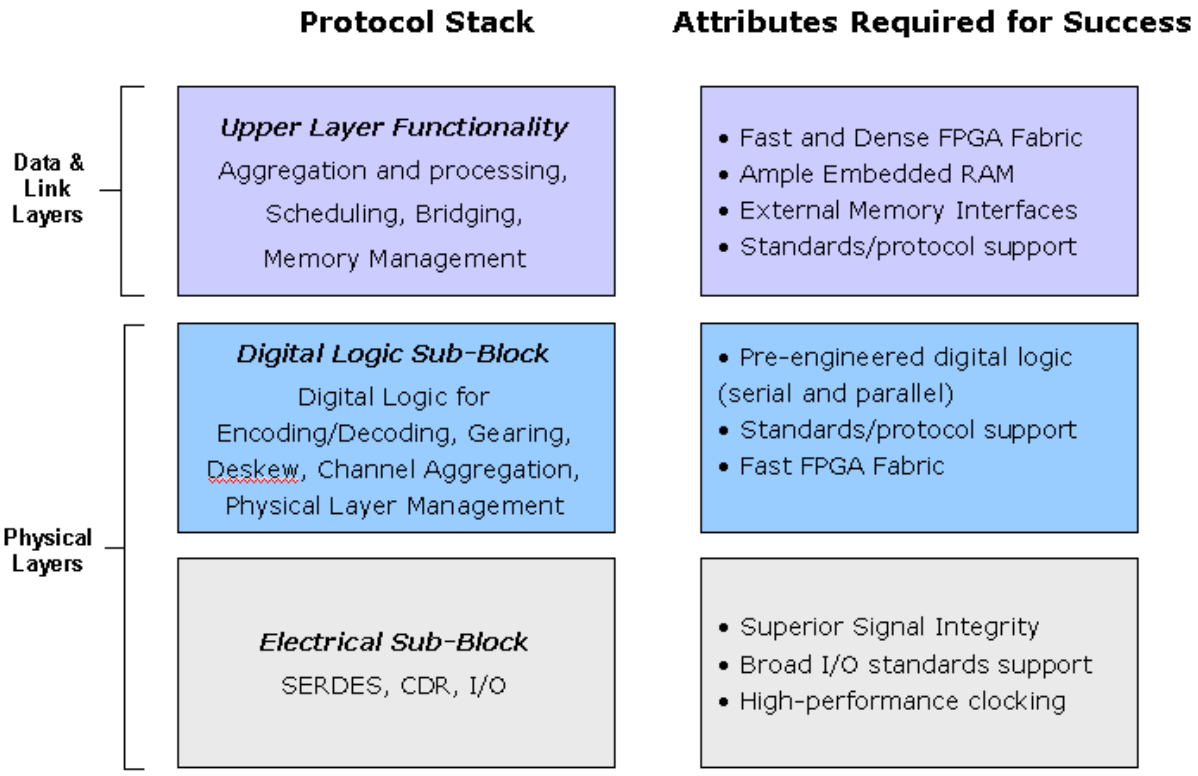


Figure 2

LatticeSC - A Platform for Connectivity

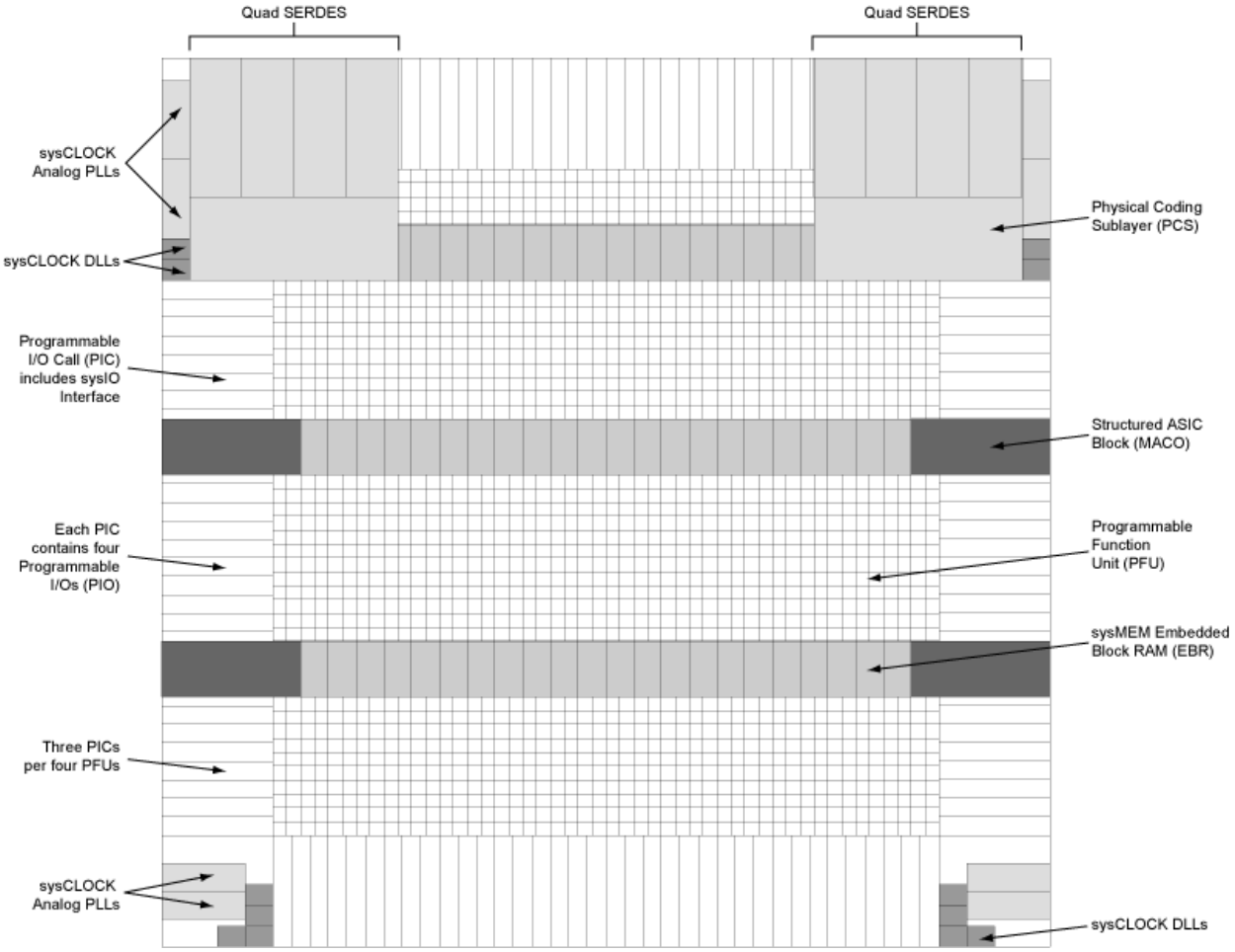
In order to reap the benefits from the market trends that are bringing FPGAs to the forefront of the connectivity challenge, these devices have undergone tremendous performance improvements and technological enhancements. In some cases, today's 90 nanometer FPGAs represent the eighth or ninth generation of innovation that has transformed these devices from a simple sea of LUTS into complex systems chips that are used in critical data path and control functions in virtually every major industry.

ARCHITECTURE OVERVIEW

The layout of a LatticeSC device is shown below. This chip combines a high-performance FPGA fabric with densities ranging from 15K to 115K LUTs, high-speed SERDES, high-performance I/Os and large embedded RAM in a single industry leading architecture. This FPGA family is fabricated in a state of the art 90nm technology to

provide the highest performing FPGAs in the industry. This family of devices includes features to meet the needs of today's communication network systems. These features include SERDES with embedded advance PCS (Physical Coding Sublayer), up to 7.8 Mbits of embedded block RAM and dedicated logic to support system level standards such as RapidIO, HyperTransport, SPI4.2, SFI-4, UTOPIA, XGMII and CSIX. The devices in this family feature clock multiply, divide and phase shift PLLs, numerous DLLs and dynamic glitch free clock MUXs that are required in high-end system designs.

The LatticeSC architecture contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of Embedded Block RAM (EBR). The upper left and upper right corners of the devices contain SERDES blocks and their associated PCS blocks. Each block of SERDES contains four channels (quad). Each channel contains a single serializer and de-serializer, synchronization and word alignment logic. The SERDES quad connects with the Physical Coding Sublayer (PCS) block that contains logic to simultaneously perform alignment, coding, de-coding and other functions.



The PICs contain logic to facilitate the conditioning of signals to and from the I/O before they leave or enter the FPGA fabric. The block provides DDR and shift register capabilities that act as a gearbox between high speed I/O and the FPGA fabric. The blocks also contain programmable Adaptive Input Logic that adjusts the delay applied to signals as they enter the device to optimize setup and hold times and ensure robust performance even as environmental conditions change. The EBRs are large dedicated fast memory blocks that may be configured as RAM, ROM or FIFO. These blocks have dedicated logic to simplify the implementation of FIFOs. The PFU, PIC and EBR blocks are arranged in a two-dimensional grid with rows and columns as shown below. These blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

The corners contain the sysCLOCK Analog Phase Locked Loop (PLL) and Digital Locked Loop (DLL) Blocks. The PLLs have multiply, divide and phase shifting capability; these are used to manage the phase relationship of the clocks. The LatticeSC architecture provides eight analog PLLs per device and 12 DLLs. The DLLs provide a simple delay capability and can also be used to calibrate other delays within the device. Every device in the family has a JTAG Port with internal Logic Analyzer (ispTRACY) capability. The sysCONFIG port supports serial or parallel device configuration. The system bus simplifies the connections of the external microprocessor to the device for tasks such as SERDES and PCS configuration or interface to the general FPGA logic. The LatticeSC devices use 1.2V as their core voltage operation with 1.0V operation also possible.

SUMMARY OF MAJOR DIFFERNTIATED DESIGN FEATURES

SERDES

The ever-present demand for increased bandwidth has led to the development of several new I/O standards and interfaces. Although faster parallel interfaces are still in the mix, the latest interfaces are based on high-speed serial (SERDES) technology that is used in commercial deployments at ranges up to 3.125 Gbps per individual link.

It is clear that serial technology is here to stay. Recent industry standardization efforts such as ATCA do not specify any one particular backplane transmission protocol, as ATCA takes great pains to remain “protocol agnostic.” This said, designers are not free to choose any standard; they must select one of five SERDES based transmission standards (Gigabit Ethernet, Fibre Channel, PCI Express, Serial RapidIO, or Infiniband). Other recent standardization efforts such as CPRI and OBSAI are also based on serial protocols.

These high data rates present unique challenges to the design community. FPGA vendors often collaborate with designers to review layout suggestions and review board level schematics in order to optimize SERDES signal integrity. Connectors have to be carefully designed as well, and a host of interop forums have emerged in the past few

years to address interoperability issues that have grown in complexity with the advent of this high speed SERDES technology.

The LatticeSC family contains from 8 to 32 SERDES channels arranged as quad banks. To support backplane applications in which the drive lengths approach 60 inches, a designer can enable Transmit Pre-emphasis as well as Receive Equalization, which are built into the LatticeSC SERDES. These two features overcome inherent transmission line loss and skin effects to improve the quality of the SERDES data eye, which deteriorates rapidly with distance over commonly used FR-4 based backplanes. The LatticeSC device has a typical power consumption of 100mW/channel @ 3.125 Gbps. Jitter specifications are 0.29 UI (typical at 3.125 Gbps) for Total Transmit Jitter and 0.8 UI (typical at 3.125 Gbps) for Total Receive Jitter Tolerance.

Other programmable features such as AC/DC coupling, various termination resistance values, amplitude settings and half rate modes are also provided to give customer great flexibility in implementing their solution.

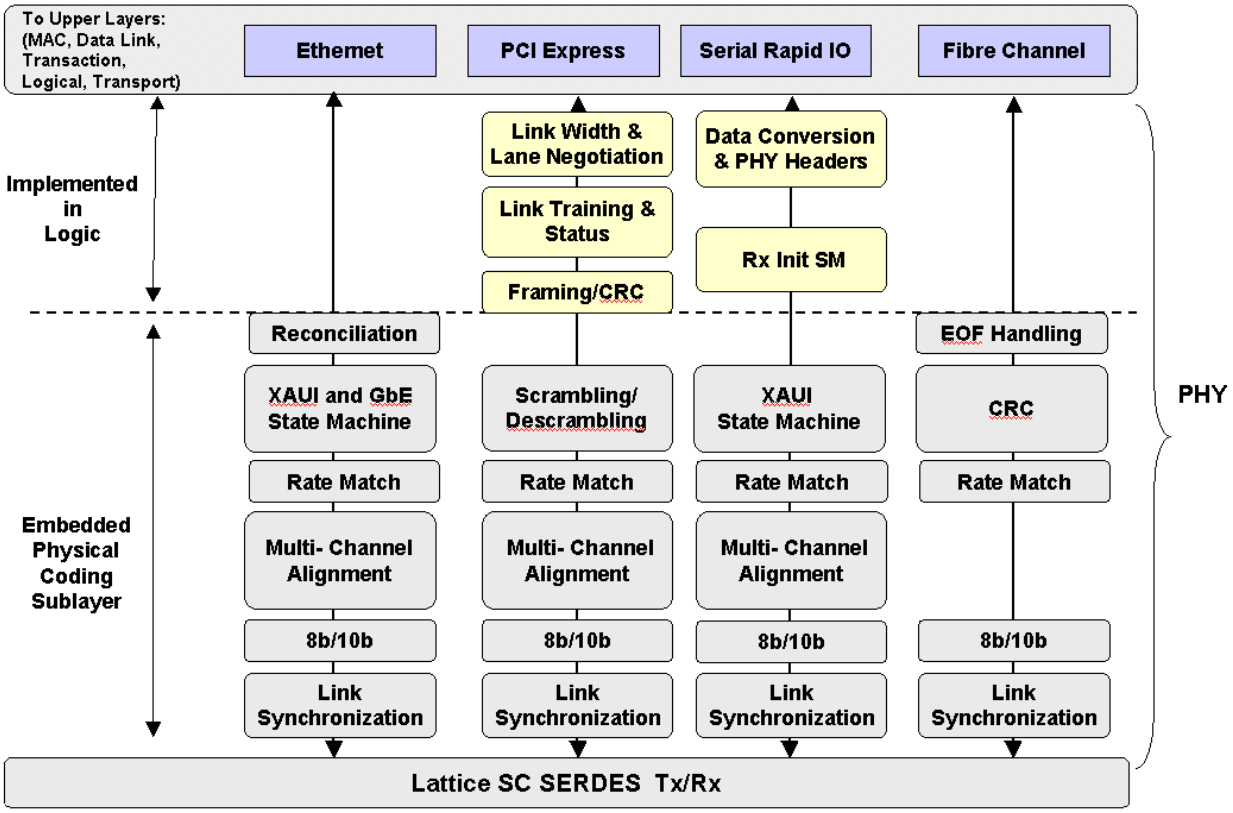
flexiPCS: Physical Coding Sublayer – Providing Complete PHY Layer Solutions

Today's connectivity challenge requires much more than simple I/O bridging. The LatticeSC device contains a unique, embedded Physical Coding Sublayer (PCS) that incorporates Physical Layer (PHY) functionality. The incorporation of these pre-engineered blocks designed using ASIC technology greatly reduces design time, FPGA gate utilization, cost and power consumption.

LatticeSC's SERDES/PCS logic can be configured to support numerous industry standard high-speed data transfer protocols. Each channel of SERDES/PCS logic contains dedicated transmit and receive SERDES for high-speed full-duplex serial data transfers at data rates up to 3.4 Gbps. The PCS logic in each channel can be configured to support an array of popular data protocols including:

- SONET/SDH (STS-12/STS-12c, STS-48/STS-48c, and TFI-5 support of 10 Gbps or above),
- Gigabit Ethernet (compliant to the IEEE 1000BASE-X specification)
- 10 Gigabit Ethernet XAUI
- PCI Express
- 1.02 or 2.04 Gbps Fibre Channel,
- Serial RapidIO

In addition, the protocol-based logic can be fully or partially bypassed in a number of configurations to allow users flexibility in designing their own high-speed data interface. A block diagram illustrating the PCS support for Ethernet, Fibre Channel, PCI Express and RapidIO is shown below.



Designers using any other packet-based protocols that use the same PHY Layer blocks (like CPRI and OBSAI) enjoy the same benefit.

Protocols requiring data rates above 3.4 Gbps can be accommodated by dedicating either one pair or all 4 channels in one PCS quad block to one data link. One quad can support full-duplex serial data transfers at data rates up to 13.6 Gbps. A single PCS quad can be configured to support 10Gb Ethernet (with a fully compliant XAUI interface), 10Gb Fibre Channel, and x4 PCI-Express and 4x RapidIO. The PCS also provides bypass modes that allow a direct 10-bit interface from the SERDES to the FPGA logic. Each SERDES pin can also be independently DC coupled and can allow for both high-speed and low-speed operation on the same SERDES pin, which is required by some Serial Digital Video applications. The LatticeSC device, as shown below, currently supports eleven modes within a SERDES quad.

Single Channel Modes:

- 8-bit SERDES Only
- 10-bit SERDES Only
- Generic 8b10b
- Gigabit Ethernet
- Fibre Channel (Single SERDES)
- 1x RapidIO
- x1 PCI-Express
- SONET (STS-12/STS-48)

Quad (4 channel) modes:

- XAUI (10GbE or 10Gb FC)
- x4 PCI-Express
- 4x RapidIO

Other Channel Modes:

- 8b/10b
- Sonet
- TFI-5
- All with multi-channel alignment per device as well as alignment between two devices.

Protocols requiring greater than 10Gbps bandwidth (e.g. PCI Express x8, x16, x32) can utilize multiple quads and use dedicated alignment circuitry, also provided in the PCS.

SONET/SDH Is Still Strong

Just a few years ago, SONET/SDH was viewed as a legacy technology that would give way to all-optical or native Ethernet transport technologies. In fact, SONET/SDH has remained firmly entrenched as a transport technology due to its proven track record, robust reliability and pervasiveness. Enhancements to SONET/SDH such as GFP,

VCAT and LCAS have extended the life of SONET/SDH by improving its ability to support multiple protocols, enhancing its granularity and reducing its deployment costs. The LatticeSC device has embedded support for SONET/SDH applications, summarized below. In addition, a few special functions were specifically added for TFI-5 support, including the option to replace some A1/A2 bytes with customer data and the ability to align all channels to within 1 UI.

Standard	Framer	Scrambler	Auto-TOH	B1 Checking	AIS Insertion and Checking	RDI-L Insertion Checking	Pointer Interpreter	Channel Alignment
OC-48	✓	✓	✓	✓	✓	✓	✓	✓
OC-12	✓	✓	✓	✓	✓	✓	✓	✓
TFI-5	✓	✓	N/A	✓	N/A	N/A	N/A	✓

PURESPEED I/O Block

In addition to SERDES, the LatticeSC device also supports several differential and single-ended I/O standards. These include LVTTL, LVCMOS, SSTL, HSTL, GTL+, AGP, LVDS, LVPECL and Hypertransport.

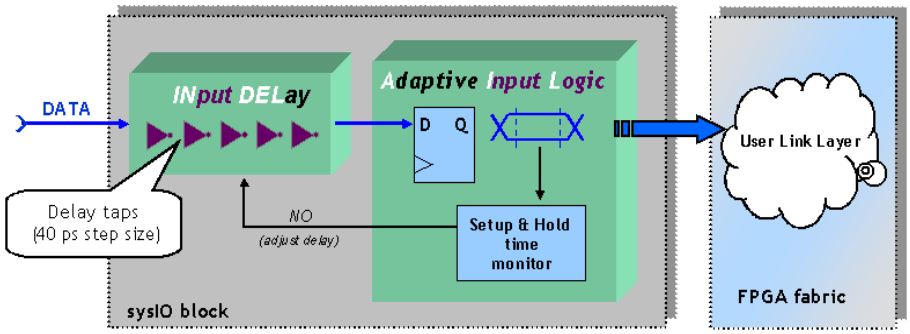
However, just being electrically compliant with these standards is not enough, as today's high speed interfaces require bit-based compensation due to the increasing difficulty of meeting and maintaining adequate setup and hold time margins for shrinking clock cycle times. This issue is exacerbated for high-speed parallel protocols, such as SPI4.2, where dynamic bit-based alignment and word alignment are key elements of the total system solution. The LatticeSC PURESPEED technology provides a dedicated I/O logic block to help simplify this process by providing a complete, highly flexible and proven I/O system. As a system, the PURESPEED block contains all of the embedded circuitry necessary to solve system level connectivity challenges without requiring the use of any generic FPGA logic resources.

Delay based alignment

While PLLs and DLLs can be used to align data and clock, the simplest way to address applications in which the clock to data relationship is well known is by utilizing an input delay block. For this purpose, the LatticeSC sysIO logic block provides the user with a 144 tap (40 ps step sizes) delay block on every pin that can be used in several modes.

Adaptive Input Logic

For many applications, bus based alignment using dedicated PLL-or DLL-based circuitry is often deemed satisfactory. However, for higher speed interfaces, bus-based alignment does not provide the precision necessary, since the delay compensation is applied globally. Essentially what is needed is a closed-loop, control and monitoring circuit that dynamically maintains proper setup and hold time margins on a bit by bit basis. For this reason, there is a third mode within the LatticeSC sysIO block where the input delay block is used in conjunction with embedded Adaptive Input Logic in order to tackle high-speed applications in which the clock to data relationship is unknown. In this configuration, shown below, the user has the ability to establish and dynamically maintain the clock to data relationship on a bit by bit basis, providing the proper resolution necessary to support speeds of up to 2Gbps on a single pin.



The key to this mode is the fact it is a self-contained, closed loop system that can be enabled/disabled under FPGA control. The closed loop design also allows for tracking and compensating for delay variations due to process, voltage and temperature conditions.

Gearbox Logic (High speed Mux/Demux)

Due to the high-speed nature of these interfaces, gearbox logic must be utilized to slow these signals down to manageable speeds for the FPGA fabric. The LatticeSC sysIO block provides this gearbox logic for both SDR and DDR interfaces. In addition, on-chip clock dividers are also provided to support the clocking requirements of the gearbox logic, alleviating the need to use generic PLL/DLL resources for this purpose. Another feature of the gearing logic is the fact that the proper domain transfer of the high-speed edge clock to the lower speed FPGA system clock is guaranteed across process, voltage and temperature. This would be impossible at these rates for FPGA devices without dedicated logic for this purpose.

MEMORY

To support line speeds of 10Gbps and more, FPGAs have incorporated larger embedded memory blocks as well as dedicated circuitry to support standardized off-chip memory devices.

There are essentially 3 hierarchies of memory utilization associated with the LatticeSC device:

- On Chip Distributed Memory: All the Programmable Functional Units can be configured as RAMs or ROMs. This versatility of the base functional building block allows the user to use the logic block build things like small FIFOs for local clock domain transfers. Up to 1.8Mb of distributed memory can be found on the LatticeSC devices.
- Embedded Block RAM (EBR): To support packet buffering, large elastic buffers and to build context and address look-up memories, an array of dedicated RAM

blocks are included on-chip. Aggregate memories reaching 7.8Mb can be built from these blocks, giving the LatticeSC one of the most competitive Memory/LUT ratios in the industry.

- External Memory Interfaces: For applications needing even larger memories, for example to support jumbo packet transfers, or buffering for traffic management and long distance transmission, the sysIO blocks have been engineered specifically to interface to existing and emerging memory components and modules. FPGA designers can now select from a variety of standard interfaces such as DDR1 / 2, RLDRAM 1 / 2, or QDR1 / 2. The LatticeSC combines DDR circuitry in the I/O Logic block, with Input Delay and dedicated DQS detection circuitry to provide memory interface solutions that exceed 800Mbps per pin bandwidth.

CLOCKING AND CLOCK MANGEMENT

High speed connectivity implies that the FPGA needs to have a powerful and efficient clocking network to be able to manage and output high frequency signals, while also allowing the FPGA fabric to process the data at very high rates. The LatticeSC clocking network has been built from the ground up to specifically tackle this issue.

Clocking Network

The LatticeSC features a hierarchical clock network starting with the 1GHz I/O connected edge clocks that are designed to interact directly with the PURESPEED I/Os toggling at 1GHz clock rates. High speed signals are transferred seamlessly to the 700MHz primary and secondary global clocks domains traversing the FPGA fabric via dedicated gearbox logic as outlined in the PURSEPEED I/O section of this white paper.

"No-Compromise" Clocking Management

DLLs provide the most area and power efficient method of managing and tracking incoming clocks. However, they do not provide very good clock and

frequency synthesis capabilities. This job is best left to low-jitter analog PLLs. Lattice delivers a "no-compromise" solution by providing 12 DLLs (max frequency of 700MHz) and 8 PLLs (max frequency of 1GHz) per device. For low EMI applications, the LatticeSC PLLs have a spread spectrum option as well.

Precision Clock Divider

These dedicated clock dividers are connected directly to the PURESPEED I/O logic blocks to provide phase matched, jitter free clock division (x2 and x4) of incoming clocks. Designers do not have to utilize or route to PLL resources on the FPGA fabric.

Masked Array for Cost Optimization (MACO) Structured ASIC Blocks

Structured ASICs have gained in popularity because of their density and performance relative to SRAM-based FPGA devices. Unlike full-custom or standard cell ASICs, structured ASICs cost far less to design, because they require only one to seven metal layer changes to accomplish their task. This results in significantly lower NRE than full custom or standard cell ASICs, as well as quicker turn-around time. Recognizing significant bandwidth, time-to-market, port density and protocol pressures in the communications market, Lattice Semiconductor has included structured ASIC blocks on the LatticeSC device. There are up to 12 structured ASIC blocks per device. Relative to FPGA gates, the use of these blocks results in highly area efficient implementations that consume minimum die real estate and offer significantly reduced power consumption.

The LatticeSCM devices use these MACO blocks to deliver popular pre-engineered IP that take 1/10th of the area and dissipate ½ the power of equivalent FPGA implementations. These include:

- flexiMAC: A unique micro-sequencer based multi-protocol engine supporting the MAC layers for Gigabit Ethernet, 10 Gigabit Ethernet and PCI Express
- SPI4.2: 256 channel, fully OIF compliant 256 Channel with dynamic alignment option

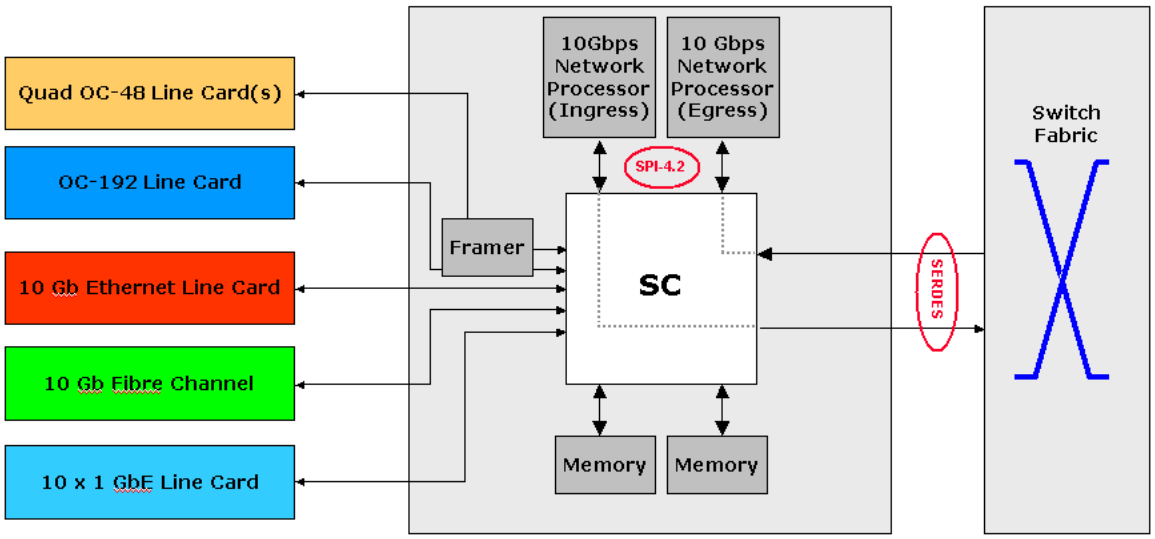
- Memory Controller: Support DDR1 / 2 and QDR1 / 2

Advanced Software Support

The ispLEVER® design tools from Lattice allow large complex designs to be efficiently implemented using the LatticeSC family of FPGA devices. Synthesis library support for LatticeSC is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeSC device. The ispLEVER tool extracts the timing from the routing and back annotates it into the design for timing verification. Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE modules for the LatticeSC family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity. An innovative high-performance FPGA architecture, high-speed SERDES with PCS support, embedded memory and high performance I/O are combined in the LatticeSC to provide excellent performance for today's leading edge systems designs.

Connectivity Application Example

The figure below illustrates the connectivity role played by FPGAs in today's multi-service environment. A single LatticeSC device is capable of supporting multiple data flavors that are in use today, as shown. In addition, the LatticeSC device will interface directly to a 10G network processor using a SPI4.2 interface. In some cases, separate processors are used for ingress and egress and a single LatticeSC device can readily support two such interfaces. High-speed memory interfaces are required to support data buffering at these faster line rates, and the LatticeSC device supports all of the latest memory standards. Finally, the LatticeSC device with up to 32 SERDES channels supports a number of serial backplane standards, such as SRIO, PCI Express, Ethernet and Fibre Channel and SONET/SDH.



LatticeSC: Meeting the Connectivity Challenge

Now it can be seen how the LatticeSC device meets the connectivity challenge. At the electrical level, the LatticeSC includes a broad range of interface standards to support the latest memory devices, network processors, DSPs, and switch fabrics. To meet the challenges created by high-speed serial designs, the LatticeSC device includes pre-emphasis at the transmitter as well as equalization at the receiver to improve signal integrity. High performance, dedicated, PLLs enable quick and accurate clock extraction from the serial stream.

Moving up to the Digital Logic Sub Block, the LatticeSC device includes a Physical Coding Sublayer that provides built-in support for leading protocols such as PCI Express, Gigabit Ethernet, SRIO, Fibre Channel and SONET/SDH. These logic blocks include such functions as 8b/10b encode/decode, Tx/Rx State Machines, Link Synchronization and deskew logic. Including these logic blocks in the LatticeSC frees design resources to focus on implementing upper layer functions, where equipment vendors can differentiate their products.

These upper layer functions include, among others, traffic aggregation, processing, policing, shaping and scheduling. Although ASSPs are often relied upon to manage

these functions, it is often the case that an FPGA will also be utilized to support an ASSP in this role or to implement customized features. The LatticeSC device includes a high speed FPGA fabric with up to 115K LUTs, embedded RAM, external memory interfaces and abundant clocking resources to support the implementation of these additional features.

Conclusion

This white paper has examined the role played by FPGAs in meeting today's connectivity challenge. Increasingly, equipment vendors are turning to FPGAs to meet the challenges imposed by rapidly changing and evolving standards and protocols as the network continues to evolve. Demand for bandwidth, the introduction of new services and the integration of these services onto existing equipment platforms are all drivers that create the need for system connectivity. The LatticeSC FPGA has been designed as a platform technology to facilitate the implementation of the many connectivity challenges that designers face today.

###