Generating a Schematic Symbol for OrCAD Capture

September 2006 **Application Note AN8075**

Introduction

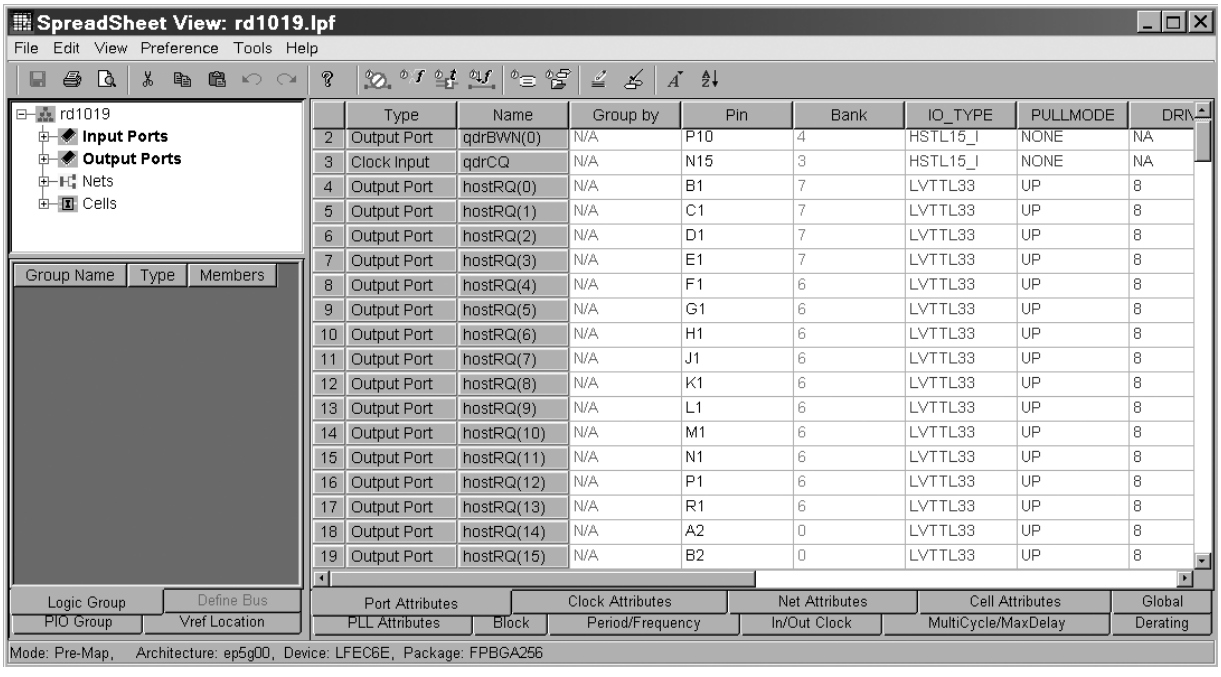
OrCAD® Capture® is a popular schematic design entry tool for system-level PCB design. The primary output of Capture is a netlist report used to import component connectivity into a PCB layout product.

Since high-density FPGA packages can provide potentially hundreds of pins, the manual methods to create schematic symbols can be tedious and error-prone. This note describes the recommended procedure to create symbols using the data import/export abilities of ispLEVER® and Capture.

Note: The procedures of this section are compatible with OrCAD Capture 10.5 and ispLEVER 6.0 or later.

Exporting Pin Information from the ispLEVER Design Planner

1. Start the ispLEVER system, if it is not already running.
2. In the Project Navigator, select the target device in the Sources in Project windows.
3. Double-click the **Pre-Map Design Planner** or **Post-PAR Design Planner** tool.
4. From the Design Planner Control window, choose **View > Spreadsheet View**.
5. Choose **File > Export > Pin Layout CSV File...**
6. Specify the output File Name and click **OK**.



The Design Planner produces a comma-separated-value (CSV) report file of all physical device pins and logic details.

An example portion of the Pin Layout CSV File is shown in the listing below. Line numbers 1-25 have been added for clarity.

Figure 1. Pin Layout CSV Example

```
 1 #Pin Layout Report csv format generated by Preference Editor
 2 #Generated at Wed Sep 07 11:50:45 2005
 3 #Design : rd1019.ngd
 4 #Package : FPBGA256
 5 Pin Name,Bank,Signal Name,Direction,IO_TYPE,PULLMODE,DRIVE,SLEWRATE,PCICLAMP,OPENDRAIN
 6 A1,Bank0,GND,,,,,,,
 7 A2,Bank0,hostRQ(14),Output Port,LVTTL33,,,,,
 8 A3,Bank0,hostRQ(29),Output Port,LVTTL33,,,,,
 9 A4,Bank0,hostRA(8),Input Port,LVTTL33,,,,,
10 A5,Bank0,hostWA(0),Input Port,LVTTL33,,,,,
11 A6,Bank0,hostWA(13),Input Port,LVTTL33,,,,,
12 A7,Bank0,hostWD(1),Input Port,LVTTL33,,,,,
13 A8,Bank0,hostWD(11),Input Port,LVTTL33,,,,,
14 A9,Bank0,hostWD(20),Input Port,LVTTL33,,,,,
15 A10,Bank0,hostWD(29),Input Port,LVTTL33,,,,,
16 A16,Bank0,GND,,,,,,,
17 B2,Bank0,hostRQ(15),Output Port,LVTTL33,,,,,
18 B3,Bank0,hostRQ(30),Output Port,LVTTL33,,,,,
19 B4,Bank0,hostRA(9),Input Port,LVTTL33,,,,,
20 B5,Bank0,hostWA(1),Input Port,LVTTL33,,,,,
21 B6,Bank0,hostWA(14),Input Port,LVTTL33,,,,,
22 B7,Bank0,hostWD(2),Input Port,LVTTL33,,,,,
23 B8,Bank0,hostWD(12),Input Port,LVTTL33,,,,,
24 B9,Bank0,hostWD(21),Input Port,LVTTL33,,,,,
25 B10,Bank0,hostWD(30),Input Port,LVTTL33,,,,,
```

The Pin Layout CSV File is an export of all physical device pins organized by bank number and pin name.

Lines 1-4 of the report are preceded with pound signs (#) and provide a report header with details about the file timestamp, ispLEVER database (NGD or NCD) and device package.

Line 5 of the report is the data header for each pin record.

Lines 6 and later are the pin records.

Depending on what stage you are in in the FPGA design flow you may or may not have assigned logical signal names from your design to specific pin locations. If so, any logical names and related preferences will appear in the report. In the example above, hostRQ(14) and hostRQ(29) (lines 7 and 8) have been assigned to pins A2 and A3 respectively of the 256 fpBGA package.

The programmed mode (Output Port) and signal standard (LVTTL33) also appear. You may choose to incorporate these details into your Capture schematic depending on your documentation standards. Reserved special purpose pins like power and no-connects appear in the report and will use the default name in the Signal Name field. In the example above, A1, Bank0 (line 6) is a ground pin (GND).

Preparing the Pin Layout CSV File for Import into Capture

1. **Start Microsoft Excel**.
   The following procedure is best performed in a spreadsheet tool like Microsoft Excel. The steps below use Excel but the technique should be similar in any other spreadsheet that supports CSV import.
2. Choose **File > Open**.
3. From the Files of type list choose **Text Files (*.prn; *.txt; *.csv)**, select the .csv file you created earlier, and click **Open**. Excel creates a new spreadsheet and places each pin record field into a column.
4. Choose **File > Save As...**

5. From the Save as type list choose **Microsoft Excel Workbook (*.xls)**, specify a new .xls filename and click **Save**.
6. Delete the report header in rows 1-4.
7. Modify the column headings to use the following OrCAD Capture naming conventions:
   a. Replace “Pin Name” with “Number”
   b. Replace “Bank” with “Section”
   c. Replace “Signal Name” with “Name”
   d. Replace “Direction” with “Type”
8. Add the following columns: **Shape**, **PinGroup**, **Position**.
9. Organize the columns (A-G) into the following order: **Number**, **Name**, **Type**, **Shape**, **PinGroup**, **Position**, **Section**.
10. Specify a default pin name for any blank cells of the Name column. A good convention is “Unused”.
11. Use Edit > Replace to replace the contents of the Type column using the following conventions:
    a. Replace “Input Port” with “Input”
    b. Replace “Input Clock” with “Input”
    c. Replace “Output Port” with “Output”
    d. Replace “Bidir Port” with “Bidirectional”

    At this point you may wish to apply other pin types that can be applied to a Capture symbol pin:
    - 3STATE
    - OPEN COLLECTOR
    - OPEN EMITTER
    - PASSIVE
    - POWER

    For example it’s common for GND and VCC pins to be designated as POWER type and Unused pins to be designated as PASSIVE type. This will influence the netlist output and design rule checks performed with Capture later.

    For more information on Capture pin types, see the Capture Knowledge System provided with OrCAD software.
12. Specify one of the following Capture symbol pin shapes for each pin record in the **Shape** column:
    - CLOCK
    - DOT
    - DOT CLOCK
    - LINE
    - SHORT
    - ZERO LENGTH

    A good default for most FPGA symbol pins is the “LINE” shape.
13. Specify one of the following Capture symbol pin positions for each pin record in the Position column:
    - Bottom
    - Left
    - Right
    - Top

    Choose **File > Save**.

Defining Part Sections

In most cases, given a device with many pins, you will likely want to establish Capture part sections which allow you to place collections of pins related to the device independent of the others. This partitioning of pins improves the readability of schematics and allows the system engineer to better represent interconnect and logical dataflow.

You can create any number of sections you wish for the FPGA symbol that will best meet your documentation standards. A common convention is to allocate a section to each I/O bank of the FPGA. Lattice FPGAs generally provide eight banks (0-7) of programmable I/Os (PIOs).

The most direct method to specify a Capture symbol section based on banks is to modify the Section column of the worksheet.

1. Replace the contents of the Section column with a number that reflects the bank organization. For example you might use the following convention for a typical Lattice FPGA:
   - Replace “Bank0” with “1”
   - Replace “Bank1” with “2”
   - Replace “Bank2” with “3”

     :
   - Replace “Bank7” with “8”

   Some pins including No-Connects (NC), VCC, VCCAUX, and GND are not associated with any particular FPGA PIO Bank. In this case you may wish to allocate an additional section to hold them. For the design example, Section 9 was assigned to all non-bank pins. For details on pin and bank organization, see the Pinout Information section of the appropriate Lattice device family data sheet.

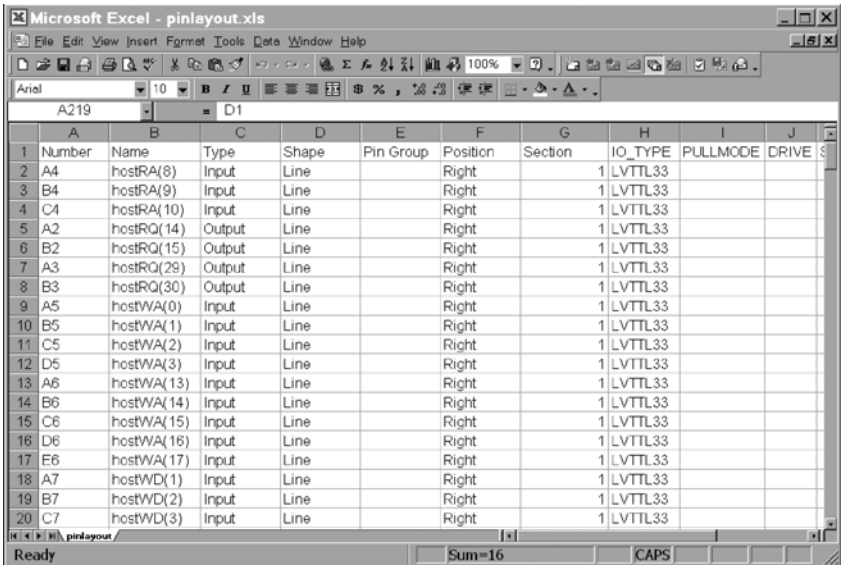
2. Choose **File > Save**.

Adjusting the Pin Order

In most cases you will likely want to establish pin order based on some company standard. The data sorting feature of the spreadsheet eases this task by allowing you to apply one or more filters. For example, you may wish to sort first by Section, then Signal Name, then Pin Name.

Note: The alphanumeric sort applied by many spreadsheets may result in unusual bus orders such as: data(0), data(1), data(10), data(11). You may need to reorder rows of the spreadsheet to account for this.

The screen shot below illustrates the changes made based on the sample pin report.

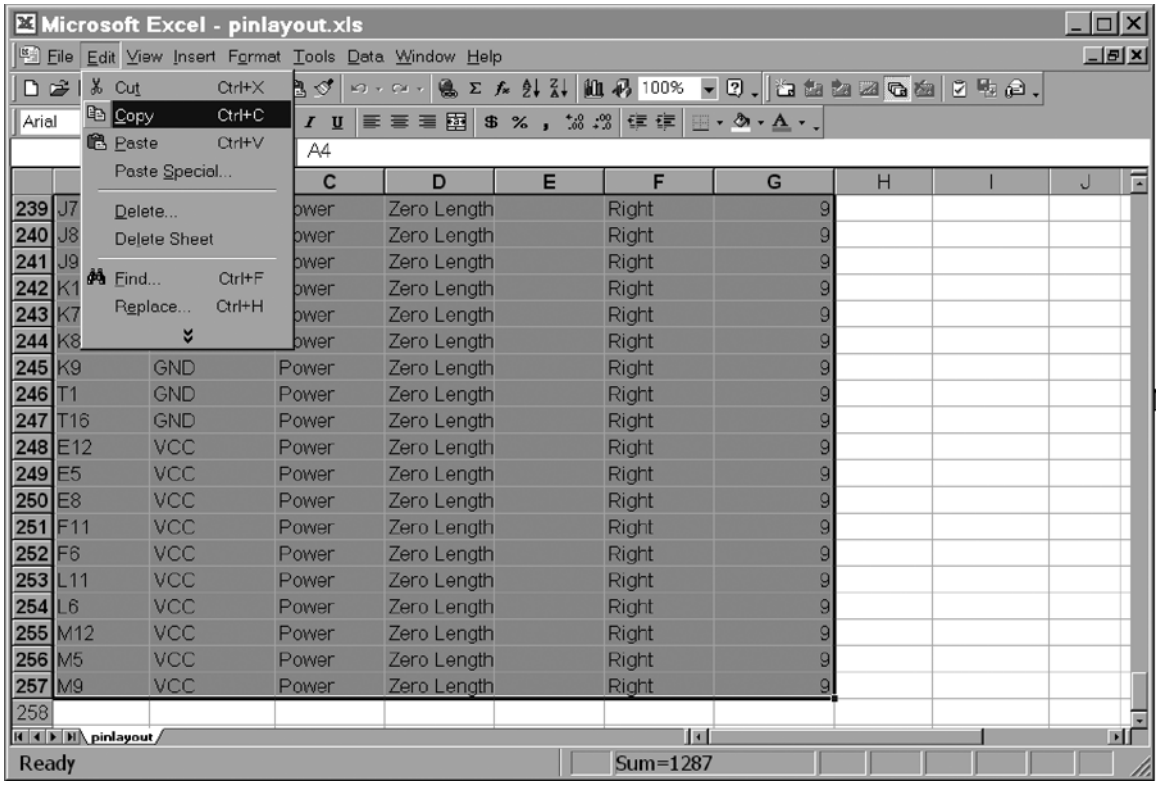


	A	B	C	D	E	F	G	H	I	J
1	Number	Name	Type	Shape	Pin Group	Position	Section	IO_TYPE	PULLMODE	DRIVE
2	A4	hostRA(8)	Input	Line		Right	1	LVTTL33		
3	B4	hostRA(9)	Input	Line		Right	1	LVTTL33		
4	C4	hostRA(10)	Input	Line		Right	1	LVTTL33		
5	A2	hostRQ(14)	Output	Line		Right	1	LVTTL33		
6	B2	hostRQ(15)	Output	Line		Right	1	LVTTL33		
7	A3	hostRQ(29)	Output	Line		Right	1	LVTTL33		
8	B3	hostRQ(30)	Output	Line		Right	1	LVTTL33		
9	A5	hostWA(0)	Input	Line		Right	1	LVTTL33		
10	B5	hostWA(1)	Input	Line		Right	1	LVTTL33		
11	C5	hostWA(2)	Input	Line		Right	1	LVTTL33		
12	D5	hostWA(3)	Input	Line		Right	1	LVTTL33		
13	A6	hostWA(13)	Input	Line		Right	1	LVTTL33		
14	B6	hostWA(14)	Input	Line		Right	1	LVTTL33		
15	C6	hostWA(15)	Input	Line		Right	1	LVTTL33		
16	D6	hostWA(16)	Input	Line		Right	1	LVTTL33		
17	E6	hostWA(17)	Input	Line		Right	1	LVTTL33		
18	A7	hostWD(1)	Input	Line		Right	1	LVTTL33		
19	B7	hostWD(2)	Input	Line		Right	1	LVTTL33		
20	C7	hostWD(3)	Input	Line		Right	1	LVTTL33		

Generating a Capture Schematic Symbol

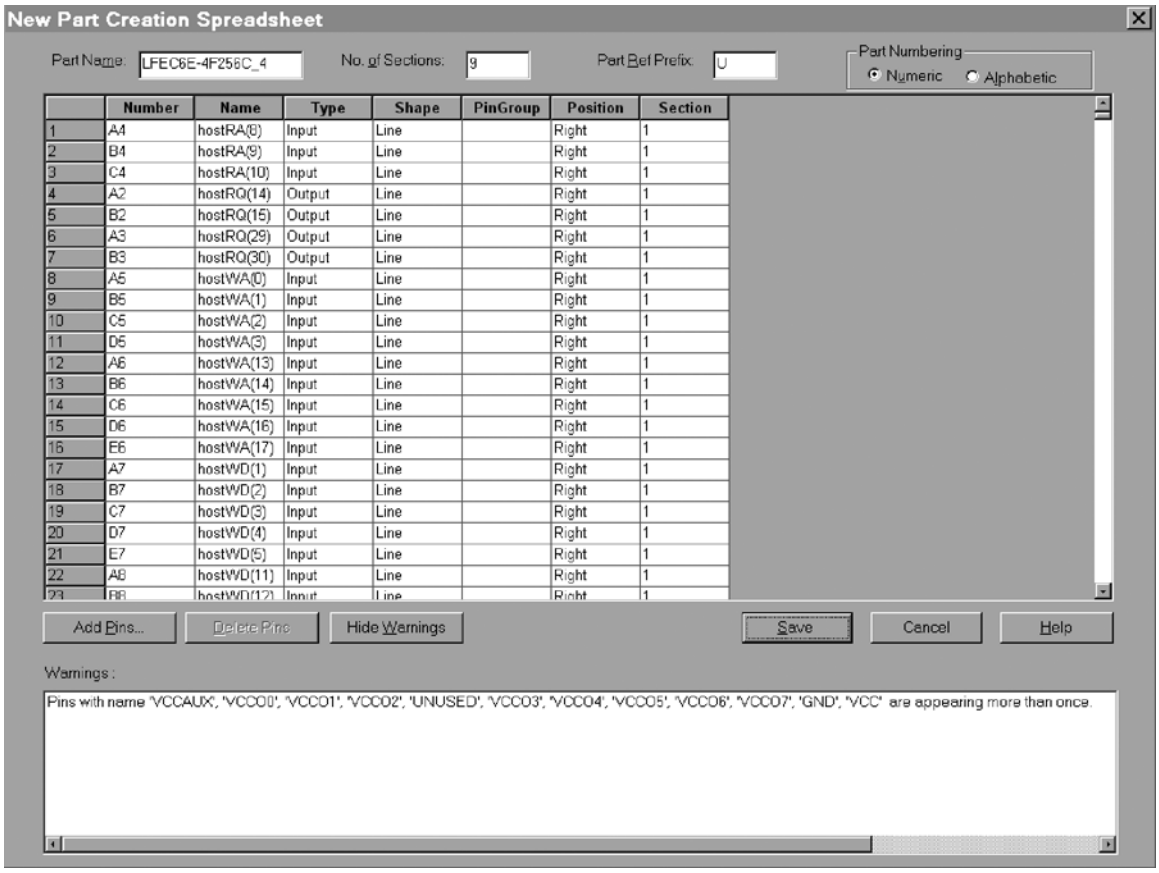
1. Start OrCAD Capture.
2. Choose **File > New > Library** then select the **filename.olb** file in the Library folder.
3. Choose **Design > New Part from Spreadsheet...**

   The New Part Creation Spreadsheet dialog appears.
4. Specify the Part Name, No. of sections, and Part Ref Prefix. If you used sections based on the FPGA bank organization in the earlier procedure, specify the number and set Part Numbering to Numeric.
5. 5. From Excel, select all the pin record cells of columns A-G, excluding the column headers, and choose **Edit > Copy**.



6. From Capture, select the **New Part Creation Spreadsheet**.
7. Select the upper left cell in row 1 and type **Ctrl+V** to paste the pin records.
8. Click **Save**.

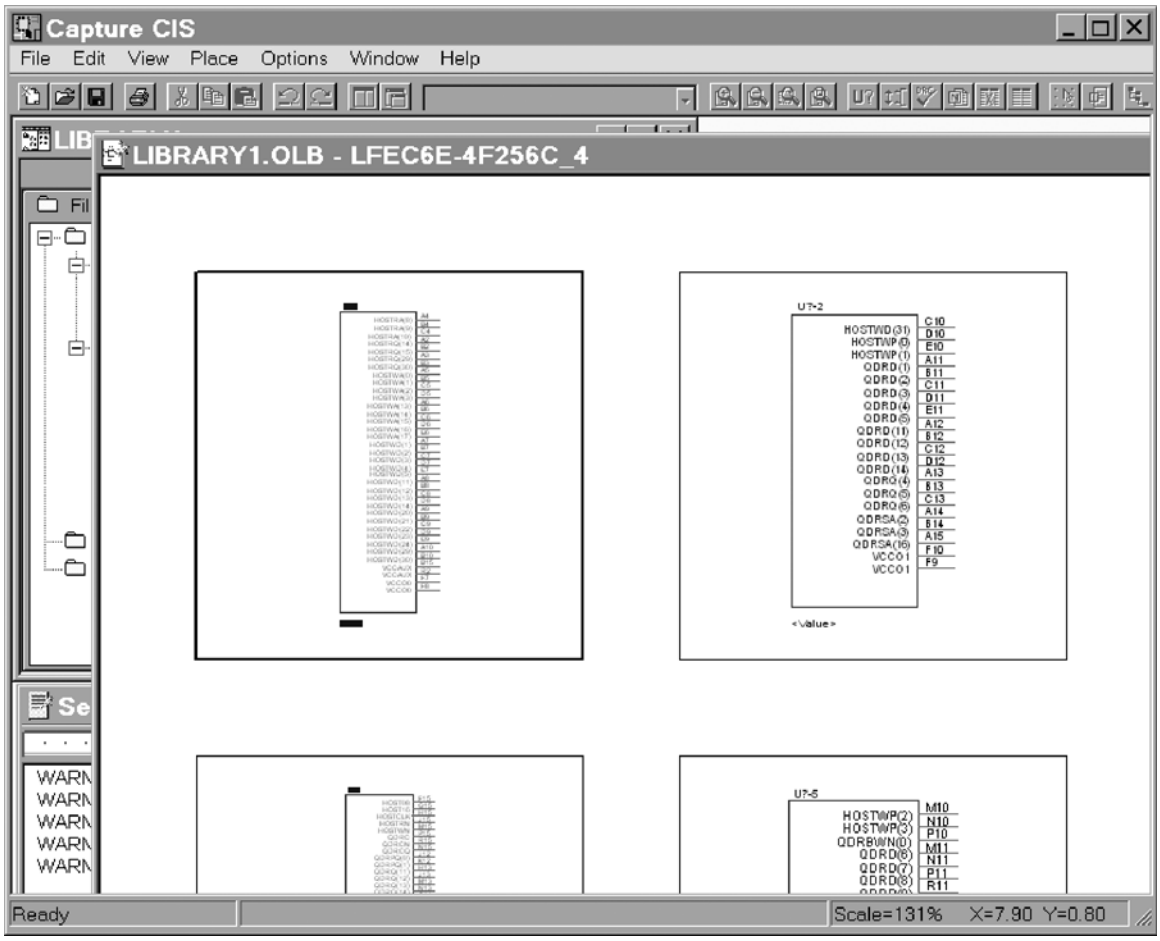
   A New Part Creation design rule check runs on the definition and you have to option to view Warnings. You can inspect and modify the spreadsheet to correct any potential problems.



After you inspect the Warnings, click **Save** again and then choose **Continue** to generate the part. A new part appears in the **filename.olb** list.

9. Double-click the new part.
   The first section appears. Use **Ctrl+N** (Next) or **Ctrl+P** (Previous) to scroll through the part sections.

The screen shot below illustrates the Package View of the Library Editor.



Technical Support Assistance

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Revision History

Date	Version	Change Summary
January 2006	01.0	Initial release.
September 2006	01.1	Replaced references to Preference Editor with Design Planner. Replaced figure 1 with a new screen shot.