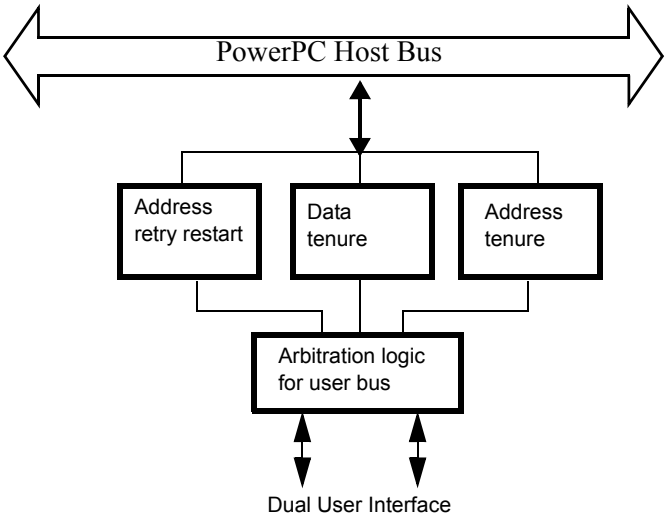
EP201 PowerPC Bus Master

FEATURES

- Fully supports PowerPC™ 60x bus protocol, include PowerPC 603, 604, 740, 750 and 8260.
- Automatic bus arbitration for address bus and data bus based on internal bus request.
- Separate address bus and data bus tenure with individual grant signals.
- Supports address bus retry and data transfer error.
- Qualified address bus grant and data bus grant through the use of bus busy signals.
- User specified burst data transfer and single beat data transfer.
- Supports two back-end user request ports with built-in arbitration.
- Efficient back-end bus for internal data transfer.
- Supports bus parking.
- Designed for ASIC or programmable logic device implementations in various system environments.
- Fully static design with edge triggered flip-flops.
- Optimized for ispXPGA product family.



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DESCRIPTIONS

The PowerPC bus master is a bus interface unit designed for the PowerPC host bus. It allows the user to initiate data transfer directly on the PowerPC CPU bus through a very simple user interface.

The PowerPC bus master arbitrates for the PowerPC address bus before starting any transfers. It handles separate address and data bus tenure so that data bus is arbitrated independently from the address bus. The bus master handles address retry by the CPU or other sources on the CPU bus. Upon address retry, it automatically re-starts the data transfer unless an error has occurred.

Single beat, burst data and extended MPC8260 data transfer are supported. Different data size and transfer types are allowed and can be specified through an internal back-end bus. There are two user interface ports provided by the bus master. It allows two different devices to access the PowerPC bus through a single bus master. The bus master contains arbitration logic to arbitrate between the two request ports.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
Extended data transfer	MPC8260 extended data transfer
Dual or single user interface	Supports one, two or multiple user request ports.
Address only transfer	Execute address only transfer on the CPU bus for data snooping.

Device Utilization

Family	Device	Utilization	Percentage	Performance
ispXPGA	LFX1200B	133 PFUs	4%	94Mhz
EC	LFFC20	527 LUTs	4%	115Mhz
XP	LFXP10	431 LUTs	8%	115Mhz
XP2	LFXP2-17E	298 slices	4%	143Mhz

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