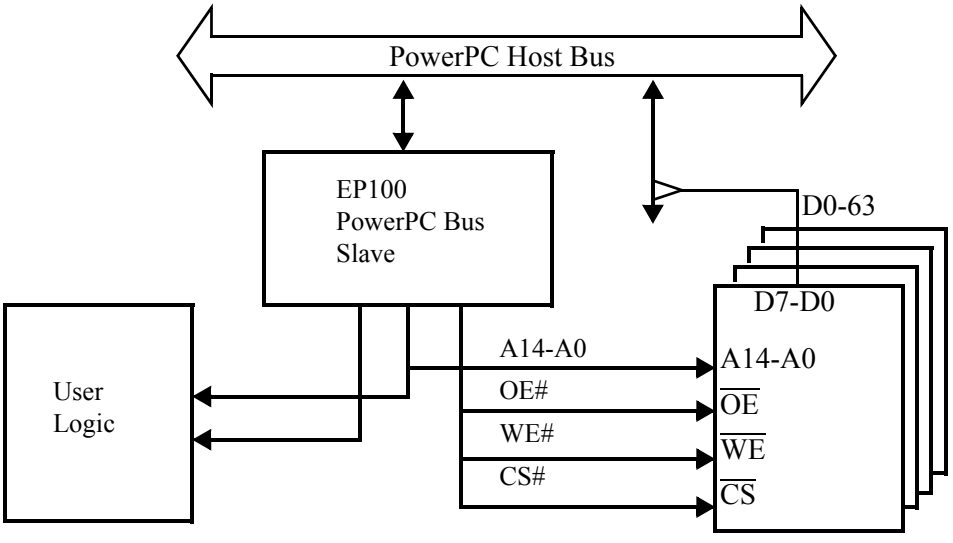
EP100 PowerPC Bus Slave

FEATURES

- Fully supports PowerPC™ 60x bus protocol including PowerPC 603, 604, 740, 750 and MPC8260.
- Provide PowerPC bus device access to memory and devices on user interface.
- Direct support for standard asynchronous SRAM and synchronous BURST SRAM.
- Burst access support using conventional asynchronous SRAM.
- Additional back-end interface bus for on-chip and off-chip logic and register access.
- Back-end interface supports user device with various wait states.
- Burst access support including MPC8260 extended transfer size.
- Write buffer supports write posting for the back-end bus interface.
- Handles separate address bus and data bus tenure.
- Supports PowerPC address pipeline for improve performance.
- Supports address bus retry generated by other external device.
- Qualified address data bus grant through the use of bus busy signals.
- Designed for ASIC and programmable logic device implementations in various system environments.
- Fully static design with edge triggered flip-flops.
- Optimized for ispXPGA product family.



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DESCRIPTIONS

The EP100 PowerPC bus slave device is a bus interface unit designed for the PowerPC host bus. It is designed to work on any 60x compliant bus architecture.

It has two user interfaces, one for interfacing with on-chip and off-chip user logic and register and the second interface is a direct interface to external asynchronous SRAM and synchronous BURST SRAM.

The PowerPC slave works together with other devices or system controllers on the PowerPC bus. The slave can be assigned to a specific address space where it is mapped into. Access to the slave device is further directed to either the SRAM interface or the user interface bus based on address mapping. The address mapping controller can be hardwired to the core or can be supplied by the user during run-time. The slave supports both the regular data transfer size and also the extended data transfer size specific to MPC8260.

The slave handles address pipeline on the PowerPC bus with up to 2 outstanding requests. While the slave is processing data transfer of one request, the CPU can start the address tenure of a second request. Address retry and separate address and data bus tenure are also supported by the slave. The slave detects data bus grant and data bus busy before starting its data tenure.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
SRAM speed	Different SRAM access speed can be programmed as wait states.
Pipeline or flow-through burst SRAM	Support both types of burst SRAM.
Bus sharing	Sharing the CPU bus with MPC106/107
Data parity	Supports PowerPC data parity
Multiple address mapping	Address space mapping to support multiple user logic devices.

Device Utilization

Family	Device	Utilization		Performance
		Slices	Percentage	
ispXPGA	LFX1200B	220	6%	72Mhz
EC	LFEC20	696	7%	92Mhz
XP	LFXP10	696	14%	97Mhz
XP2	LFXP2-17E	500	6%	116Mhz

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