Programmable Comparator Options for the ispPAC-POWR1220AT8

November 2005 Application Note AN6069

Introduction

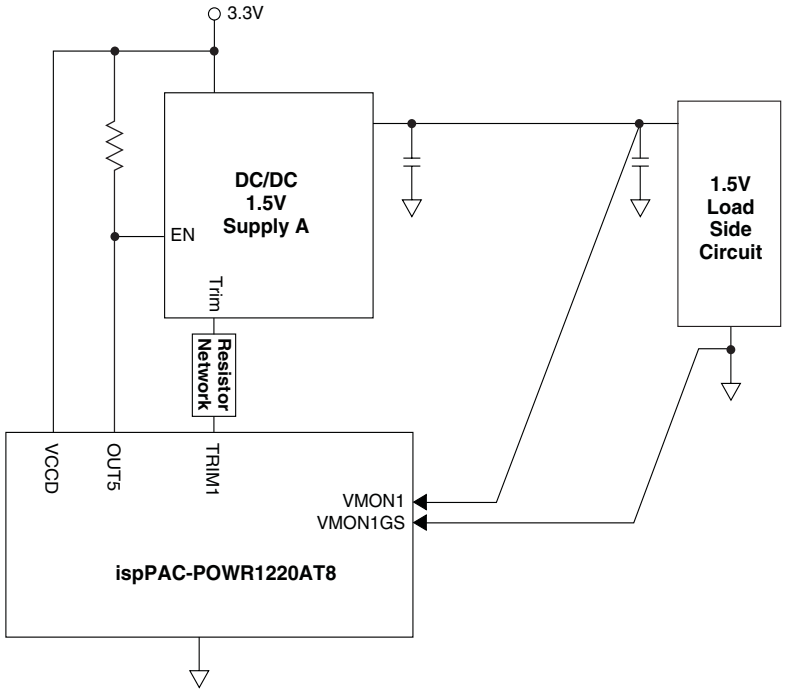
Lattice's ispPAC®-POWR1220AT8 offers a wide range of features for managing multiple power supplies in a complex system. This application note outlines the key features associated with the voltage monitoring functions. In order to better understand the flexible architecture of the front end, the circuitry will be broken down into sections to be discussed individually. The relationships of these blocks is also discussed, along with how they interact with the PLD and other functional blocks within the ispPAC-POWR1220AT8.

The ispPAC-POWR1220AT8 provides 24 independently programmable trip point comparators connected to 12 voltage monitoring pins. Each of the comparators has 368 programmable trip points, ranging from .664V to 5.734V. In addition to these, there is a low level trip point for powered down supplies that trips at 75mV. The 75mV setting is used to determine if a given supply has decayed all the way down and is safely off, before recycling it back on or starting another sequence or event.

Differential Input Comparator

The ispPAC-POWR1220AT8 has 24 comparators, each independently programmable. Each set of VMON pins or voltage monitors is tied to a pair of comparators (see Figure 1). The VMON pins themselves are a pair of differential inputs to minimize measurement error in a noisy environment. The differential pair for each VMON, allows the designer to monitor the voltage at a remote point on the board with a pair of pins, one the positive VMON and the other the sense line or ground sense (VMONGS). Figure 1 below shows a simplified diagram of the ispPAC-POWR1220AT8 controlling and monitoring a 1.5V supply. Note the remote sense line and location of the VMON1 voltage monitor line. The physical location on the net where the voltage is to be measured is critical if there is high current for the supply rail or noise on the board. Each VMON has a ground sense line, these must be connected in all cases. If the sense line is not hooked directly to the ground near the load, connect it to the local ground plane. The ground sense lines can have a maximum voltage of -200mV to +300mV with respect to the ground of the ispPAC-POWR1220AT8.

Figure 1. Simplified Interface Showing VMON Groundsense



Trip Points

The 368 programmable trip points allow the user to select voltages around popular power supply ranges. The trip points range from .664V (Table 1) to 5.734V (Table 2). In addition there is a low-level trip point at 75mV to determine if a power supply has discharged all the way down. Each VMON pin has the 368 programmable trip points plus the 75mV trip point setting. To monitor supplies outside the range of these voltages such as 12V or 24V, a simple voltage divider can be placed in front of the VMON pins. See Lattice application note AN6041, *Extending the VMON Input Range of ispPAC Power Manager Devices* for further information. The VMON input impedance, which is typically 65k Ohms, must be considered when designing this voltage divider.

ispPAC-POWR12220AT8 Trip Point Tables

Table 1. Trip Points for Under-Voltage Detection

Fine Range Setting	Coarse Range Setting											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	0.786	0.936	1.114	1.326	1.571	1.874	2.232	2.650	3.139	3.738	4.792	5.703
2	0.782	0.930	1.108	1.319	1.563	1.864	2.220	2.636	3.123	3.718	4.766	5.674
3	0.778	0.926	1.102	1.312	1.554	1.854	2.209	2.622	3.106	3.698	4.741	5.643
4	0.773	0.921	1.096	1.305	1.546	1.844	2.197	2.607	3.089	3.678	4.715	5.612
5	0.769	0.916	1.090	1.298	1.537	1.834	2.185	2.593	3.072	3.657	4.689	5.581
6	0.765	0.911	1.084	1.290	1.529	1.825	2.173	2.579	3.056	3.637	4.663	5.550
7	0.761	0.906	1.078	1.283	1.520	1.815	2.161	2.565	3.039	3.618	4.638	5.520
8	0.756	0.901	1.072	1.276	1.512	1.805	2.149	2.550	3.022	3.598	4.612	5.489
9	0.752	0.896	1.066	1.269	1.503	1.795	2.137	2.536	3.005	3.578	4.586	5.459
10	0.748	0.891	1.060	1.262	1.495	1.785	2.125	2.522	2.988	3.558	4.561	5.428
11	0.744	0.886	1.054	1.255	1.486	1.774	2.113	2.507	2.971	3.537	4.535	5.397
12	0.739	0.881	1.048	1.248	1.478	1.764	2.101	2.493	2.954	3.517	4.509	5.366
13	0.735	0.876	1.042	1.240	1.470	1.754	2.089	2.479	2.937	3.497	4.483	5.336
14	0.731	0.871	1.036	1.233	1.461	1.744	2.077	2.465	2.920	3.477	4.457	5.305
15	0.727	0.866	1.030	1.226	1.453	1.734	2.064	2.450	2.903	3.457	4.431	5.274
16	0.723	0.861	1.024	1.219	1.444	1.724	2.052	2.436	2.886	3.437	4.406	5.244
17	0.718	0.856	1.018	1.212	1.436	1.714	2.040	2.422	2.869	3.416	4.380	5.213
18	0.714	0.851	1.012	1.205	1.427	1.704	2.028	2.407	2.852	3.396	4.355	5.183
19	0.710	0.846	1.006	1.198	1.419	1.694	2.016	2.393	2.836	3.376	4.329	5.152
20	0.706	0.841	1.000	1.190	1.410	1.684	2.004	2.379	2.819	3.356	4.303	5.121
21	0.701	0.836	0.994	1.183	1.402	1.673	1.992	2.365	2.802	3.336	4.277	5.090
22	0.697	0.831	0.988	1.176	1.393	1.663	1.980	2.350	2.785	3.316	4.251	5.059
23	0.693	0.826	0.982	1.169	1.385	1.653	1.968	2.337	2.768	3.296	4.225	5.030
24	0.689	0.821	0.976	1.162	1.376	1.643	1.956	2.323	2.752	3.276	4.199	4.999
25	0.684	0.816	0.970	1.155	1.369	1.633	1.944	2.309	2.735	3.256	4.174	4.968
26	0.680	0.810	0.964	1.148	1.361	1.623	1.932	2.294	2.718	3.236	4.149	4.937
27	0.676	0.805	0.958	1.140	1.352	1.613	1.920	2.280	2.701	3.216	4.123	4.906
28	0.672	0.800	0.952	1.133	1.344	1.603	1.908	2.266	2.684	3.196	4.097	4.876
29	0.668	0.795	0.946	1.126	1.335	1.593	1.896	2.251	2.667	3.176	4.071	4.845
30	0.664	0.790	0.940	1.119	—	1.583	1.884	2.236	—	3.156	4.045	4.815
Low-V Sense	75mV											

Table 2. Trip Points for Over-Voltage Detection

Fine Range Setting	Coarse Range Setting											
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	0.790	0.941	1.120	1.333	1.580	1.885	2.244	2.665	3.156	3.758	4.818	5.734
2	0.786	0.936	1.114	1.326	1.571	1.874	2.232	2.650	3.139	3.738	4.792	5.703
3	0.782	0.930	1.108	1.319	1.563	1.864	2.220	2.636	3.123	3.718	4.766	5.674
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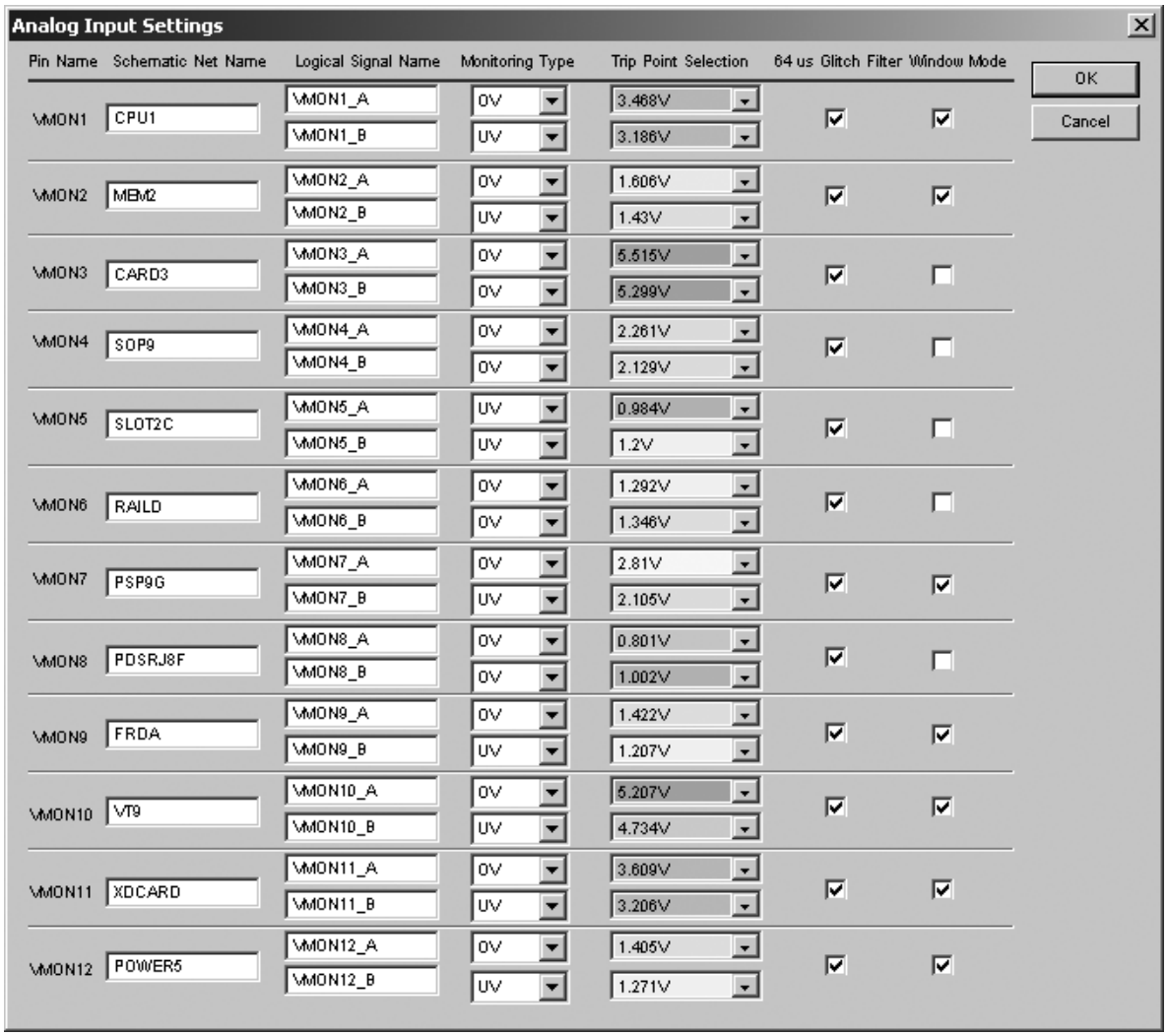
30	0.668	0.795	0.946	1.126	—	1.593	1.896	2.251	—	3.176	4.071	4.845
Low-V Sense	75mV											

Table 1 lists the available trip points when a VMON is being used to sense an under-voltage condition and Table 2 lists the trip points that are available when a VMON is being used to sense and over-voltage condition. Most of the values in Table 1 are also used in Table 2; thus, the total number of trip points is still 368.

Figure 2 shows the “Analog Input Settings” dialog box from PAC-Designer® (a full featured Windows®-based design utility) that is used to configure each of the 24 VMON trip points. Notice each trip point can be configured as either an “Over” or “Under” trip point. The list of available trip points automatically changes from the list in Table 1 to the list in Table 2 based on the “Over” or “Under” selection. By dynamically changing the list of trip points, the software automatically includes the comparator hysteresis in the setting.

Figure 2. Analog Input Settings Software Screen



Hysteresis

Each comparator has hysteresis of approximately 1% of the trip point value. The hysteresis scales with the input divider setting, looking at the columns in Table 2, the column on the far right with the highest values range up to 5.734V. This range has hysteresis of approximately 61mV. This is summarized in Table 3. Each column in the main trip point table is represented in the hysteresis table below. To summarize, the hysteresis scales with the trip point setting, is approximately 1% and ranges from 8mV to 61mV.

Table 3. Hysteresis vs. Trip Point

Low Limit	High Limit	Hysteresis (mV)
.664	.790	8
.790	.941	10
.940	1.12	12
1.119	1.333	14
1.326	1.580	17
1.583	1.885	20
1.884	2.244	24
2.236	2.665	28
2.650	3.156	34
3.156	3.758	40
4.045	4.818	51
4.815	5.734	61

Window Comparator

In Figures 3 and 4, the upper comparator (Comp A in Figure 3) must be configured as an "Over" Voltage comparator and the trip point Voltage should be the highest voltage of the window (3.468V in Figure 4). The lower comparator (Comp B in Figure 3) has to be configured as an "Under" Voltage comparator and the trip point Voltage has to be set to the lower of the two values (3.148V in Figure 4).

The MUX in Figure 3 (switch in Figure 4) selects the window output from the AND gate or the direct output from the upper comparator (Comp A in Figure 3). The selection is made by checking the "Window Mode" check box for the respective VMON in the "Analog Input Settings" dialog box shown in Figure 2.

Regardless of the "Window Mode" setting, the output of lower comparator (Comp B in Figure 3) is always provided unmodified to the PLD as the VMON1B signal. The VMON1B signal can be combined with the window signal (VMON1A) to determine if the voltage at the pin is below the window or above it.

The output of the upper comparator (Comp A in Figure 3) is inverted at the input to the AND gate to provide a true logic level for the window function when the Comp A trip point voltage is greater than the Comp B trip point voltage. The logic level of the VMON1A output signal in window mode is "HIGH" when the monitored voltage is "INSIDE" the window that is defined by the user selectable trip points.

Figure 3. VMON Comparator Logic Diagram

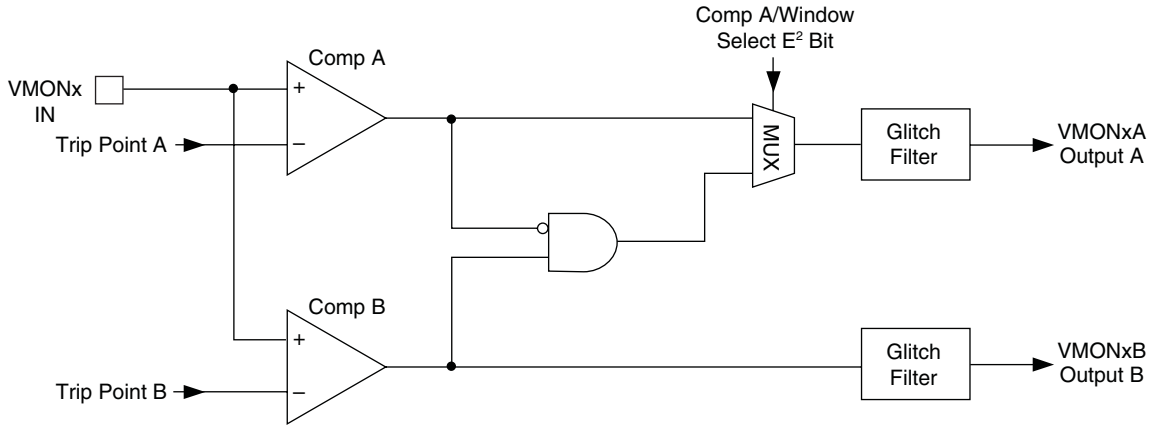


Figure 4. PAC-Designer Screen Showing Window Comparator Function

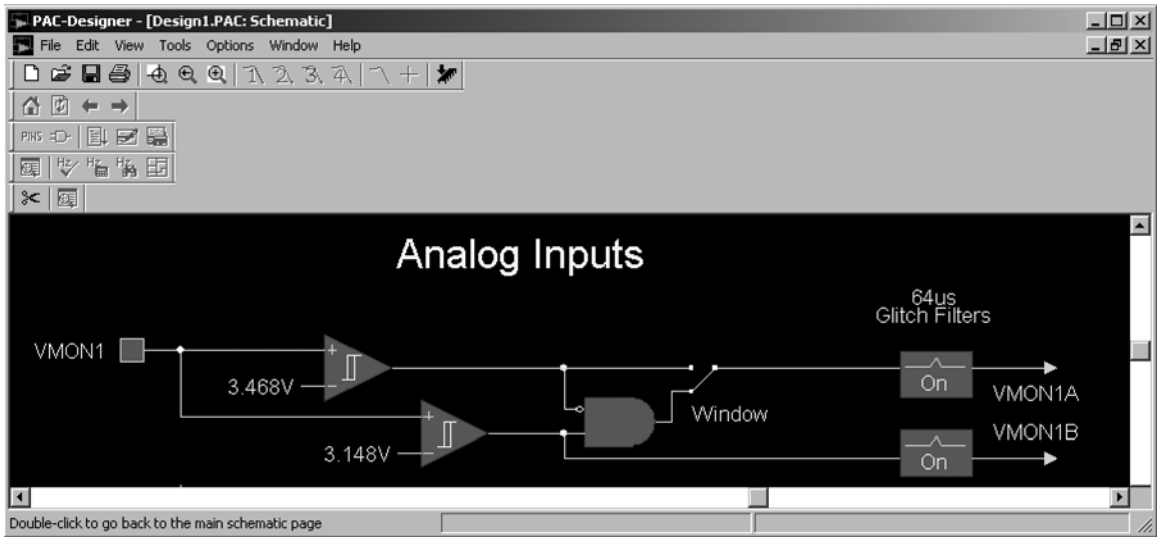
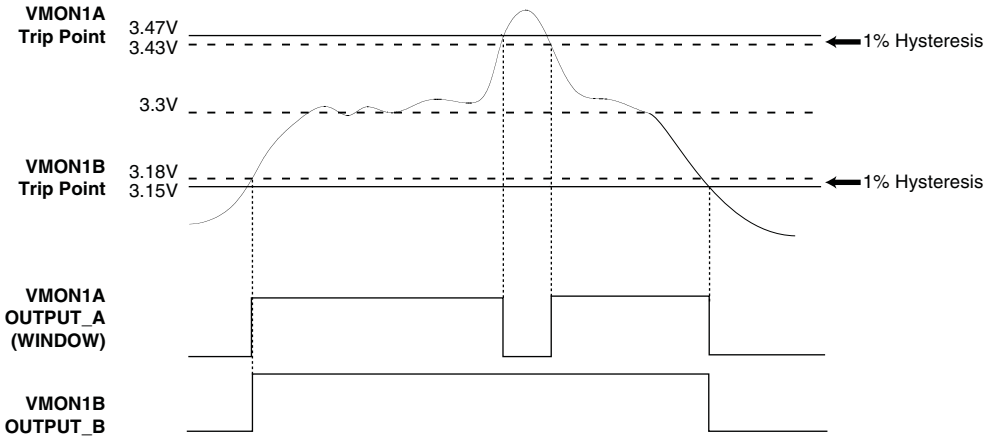


Figure 5 shows the output logic waveform relationship as would be seen on an oscilloscope for the two comparators when used in window mode. The area inside the window is defined as the voltage bound by VMON1A trip point and the VMON1B trip point in this example. Note the output VMON1A (Window Mode) is high when the voltage is inside the window defined by the trip point values programmed. Also note the output VMON1B is still active and switches based on the trip point set on VMON1B. As long as the width of the high going pulse is wide enough to get past the glitch filter, the output will toggle.

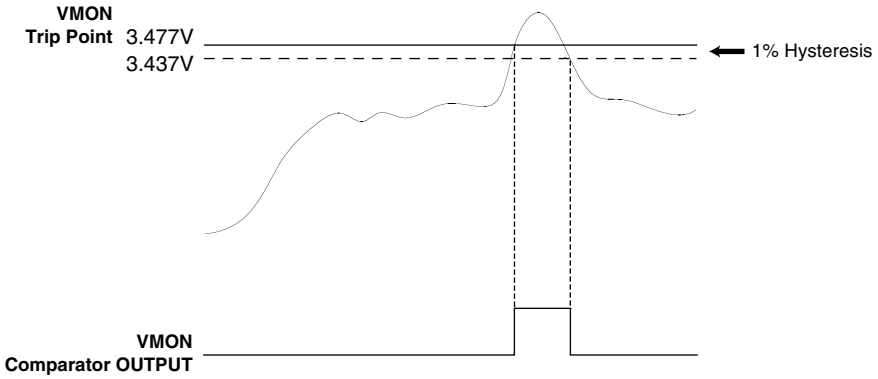
Figure 5. Over-Voltage Monitoring Waveform, Window Mode



Over-Voltage Monitoring

PAC-Designer selects the comparator trip points from the two tables (Table 1 and Table 2), based on the type of monitoring that is to be done. If the monitored signal should not exceed a certain value then over-voltage “OV” trip points should be used. When “OV” trip points are selected the hysteresis will be placed below the selected trip point so the actual trip value at the device will match the value selected in software. “OV” trip points are used in conjunction with input signals that are rising or are suspect to increase with time. Using over-voltage trip points assures one that the comparator output will be a logic HIGH exactly when the input signal goes above the selected trip point. Either VMON comparator (Comp A or Comp B) can be configured for “OV” monitoring. “OV” trip points can be used to verify a power supply is above a certain minimum to be operational and/or they can be used to sense if the input signal is exceeding a certain maximum voltage. Figure 6 illustrates the logic output of a comparator that is using an over-voltage trip point of 3.477V.

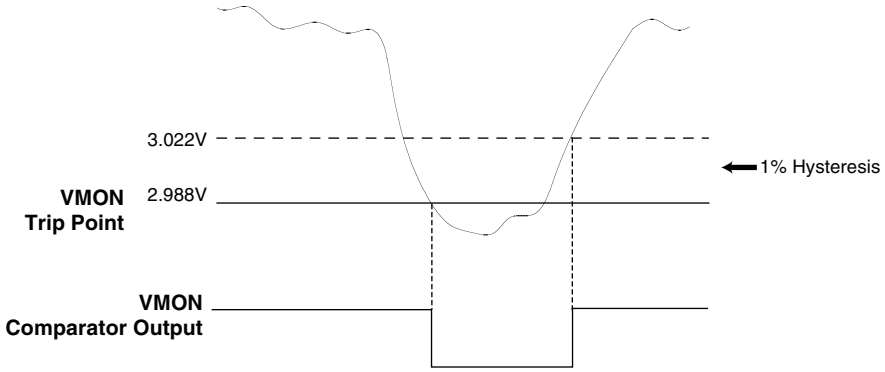
Figure 6. Over-Voltage Monitoring



Under-Voltage Monitoring:

The comparator trip points are adjusted by PAC-Designer based on the type of monitoring that is to be done. If the monitored signal should not fall below a certain value then under-voltage "UV" trip points should be used. When "UV" trip points are selected the hysteresis is placed above the selected trip point so the actual trip value at the device will match the value selected in software. "UV" trip points are used in conjunction with input signals that are falling or are suspect to decrease with time. Using under-voltage trip points assures one that the comparator output will be a logic LOW exactly when the input signal goes below the selected trip point. Either VMON comparator (Comp A or Comp B) can be configured for "UV" monitoring. "UV" trip points can be used to verify a power supply is above a certain minimum to be operational and/or they can be used to sense if the input signal has fallen below a certain minimum voltage. Figure 7 illustrates the logic output of a comparator that is using an under-voltage trip point of 2.988V.

Figure 7. Under-Voltage Monitoring



Power Supply Discharge Monitoring (75mV VMON)

In addition to the 368 trip points for each VMON comparator, there is a low trip point setting at 75mV. This is for monitoring to see if the power supply is all the way off or fully discharged. In order to recycle power back up again after a fault, some systems require that the supplies to certain chip sets such as ASICs or FPGAs be discharged below a given value. The 75mV VMON setting can be used to determine if the supply is nearly discharged all the way down before it is turned back on again and the sequence re-initiated. The 75mV setting is selected as any other VMON and simply pulled down from the menu list.

Glitch Filter

The ispPAC-POWR1220AT8 has a digital glitch filter between the VMON comparator outputs and the PLD inputs. Each VMON input has two filters (one for Comp A and one for Comp B). When the filter is enabled it prevents the PLD from reacting to glitches that are shorter than 64 microseconds. Even with hysteresis built into the compara-

tors noisy environments (such as power supplies) can cause the outputs to change state. When the filter is not enabled the PLD inputs are updated (or sample the comparator outputs) every 16 microseconds. Regardless of whether the glitch filters are enabled or not, they contain the architecture to synchronize the comparator outputs to the PLD inputs. Thus, the external asynchronous events, such as a power supply ramping up, are synchronized to the PLD clock.

AGOOD Logic Signal

All the VMON comparators auto-calibrate immediately after a power-on reset event. During this time, the digital glitch filters are also initialized. This process completion is signalled by an internally generated logic signal: AGOOD. All logic using the VMON comparator logic signals must wait for the AGOOD signal to become active.

Summary

In this application note we have taken a detailed tour through the ispPAC-POWR1220AT8 Power Managers VMON input circuits. Starting with the 12 differential inputs that allow voltage monitoring at various loads without introducing errors from small differences in the ground potentials. Each VMON has two comparators that can be set independently to support “window” monitoring without using PLD logic resources. The comparators can be set to any one of 368 precision trip points or the near zero voltage trip point of 75mV. A fixed hysteresis of about 1% of the trip point voltage is built into each comparator to provide a stable output signal. PAC-Designer automatically includes the hysteresis in each trip point selection based on the type of monitoring to be done. Over voltage “OV” trip points use the upper value while under voltage “UV” use the lower value. Thus, designers can specify the direction of the voltage condition and the precise trip point at which something has to happen from a simple and user-friendly graphical interface. Finally, two glitch filters are provided for each VMON to filter and synchronize the signals before presenting them to the PLD. In conclusion, the combination of features in the VMON hardware and the support of software with PAC-Designer places the ispPAC-POWR1220AT8 at the lead of the Power Manager pack.

Technical Support Assistance

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