COMPLEX POWER MANAGEMENT:

AN IMPERATIVE FOR

MODERN SYSTEM DESIGN

A Lattice Semiconductor White Paper

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Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

The Need for Complex Power Management

Modern embedded systems designs emphasize increased system performance while reducing operating power consumption. Increasing performance is usually achieved by increasing the operating frequency or by using more powerful, higher density VLSI ICs (or both). However, both approaches increase the circuit board's power consumption. Consequently, advanced power management techniques are imperative to increase performance and reliability within a power budget.

Such systems include ATCA, CompactPCI, and Wireless Base Station. In these systems, overall system-level power consumption is controlled by a processor in the control card called the shelf manager. These shelf managers determine if a line card plugged into the backplane should be turned on.

An Increasing Number of DC-DC Converters on a Circuit Board

The number of DC-DC converters used on a circuit board should be able to generate all supply voltages required by multi-voltage devices used. Often, however, more DC-DC converters may be required than the total number of power supply voltages used on the circuit board. This is due to:

Intermediate Bus Architecture (IBA)

Most telecom systems are powered by -48V. But most devices on the circuit board require voltages much lower than that (e.g.. 3.3V, 2.5V, 1V, etc.). Generating each of these voltages using an individual isolated DC-DC converter is both inefficient and expensive. Modern designs use one isolated DC-DC converter to generate an intermediate voltage of 12V. This locally generated 12 volts will power non-isolated DC-DC converters to generate all the required power supply voltages. This power supply distribution architecture is called an intermediate bus architecture.

The power manager is now required to monitor the intermediate bus voltage in addition to the supply voltages on the circuit board.

Point of Load Power Supply

Many high density ICs require that some of their power supplies (usually core supply voltages) be located close to their corresponding power pins in order to meet their dynamic power requirement. This demand is often met by the use of an independent Point-of-Load (POL) power supply. This results in the use of multiple POLs, even though the same voltage might have been generated by another DC-DC converter elsewhere on the circuit board. Additionally, all these POLs should be sequenced correctly (as determined by the device requirements), as well as monitored for power supply faults.

The Need for a Non-standard Supply Voltage

For most multi-voltage devices, the I/O voltage requirements are determined by the logic standard used. However, their core power supply voltages are determined by fabrication technology. For example, for devices fabricated using 90 nm technology, the core power supply voltage will be approximately 0.9V to 1.2V.

Most discrete off-the-shelf voltage supervisors can monitor standard power supply voltages (e.g., 3.3V, 2.5V, 1.8V) for faults. But to monitor non-standard supply voltages, designers resort to either a resistive network with a standard voltage monitoring IC, or to a programmable threshold voltage supervisor.

Tight Control over Power Supply Output Voltage Swing

The signal quality of high-speed communication ICs using SERDES technology depends not only on the output signal jitter (characterized by the width of the Eye Diagram), but also its voltage swing (characterized by the height of the Eye Diagram). The voltage swing can be maximized by limiting the I/O power supply voltage variation. Usually, most power supplies have a variation of 3%.

Consequently, a separate DC-DC converter with very low voltage variation may have to be used to source the I/O power supply.

Power Supply Voltage Margining

In order to verify circuit board operation across its specified range, one common practice is to check board operation at elevated and depressed power supply voltage levels. The tolerable power supply voltage increase or reduction, called power supply margining, varies for each circuit board and usually is part of a quality control test. For example, the power supplies on a circuit board may be reduced by 5% from their typical values and verified for operation at their specified performance levels.

Power Manager II Family of Products

The ispPAC Power Manager II family is a functional superset of Lattice's award winning ispPAC Power Manager devices, and provides power supply margining and trimming as well as power supply voltage measurement through its I^2C interface. The first member of this family is the ispPAC-POWR1220AT8 (Power1220AT8) packaged in a 100-pin TQFP package.

Block Diagram Description

The POWR1220AT8 device, built on advanced, non-volatile E^2CMOS ® technology, integrates a 48 macrocell ruggedized CPLD, 12 analog voltage monitor inputs each with dual voltage monitoring comparators, a 10-bit Analog to Digital Converter (ADC) for voltage measurements, and eight 8-bit Digital to Analog Converters (DAC) for trimming power supplies. The integrated I^2C interface enables a microcontroller, such as an Intelligent Platform Management Controller (IPMC), to read the status of all the comparators -- inputs as well as outputs.
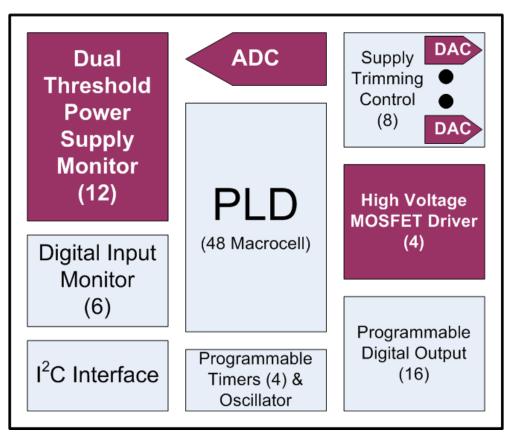
Figure 1 – Power1220AT8 Block Diagram

Power Supply Monitoring Inputs

The ispPAC-POWR1220AT8 has 12 analog voltage monitoring inputs. Figure 2 shows the architecture of an analog monitoring input. The power supply voltage is sensed using a differential input buffer to minimize the effects of circuit board ground noise on voltage monitoring / measurement accuracy. The output of the differential input buffer is connected to an ADC for voltage measurement, as well as to two independent comparators (CompA and CompB) that may be used for sensing the relationship of the monitored input voltage to two user-programmable reference thresholds. Each comparator reference has 368 programmable trip points over the range of 0.664V to 5.734V. Additionally, a 75mV 'zero-detect' threshold is selectable, which allows the voltage monitors to determine if a monitored signal has dropped to ground level. The hysteresis at the comparator

input scales with the set threshold. In general, the hysteresis is nearly 1% of the programmed threshold setting.
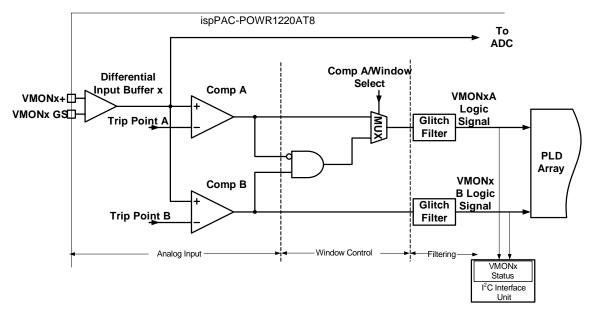

Figure 2 - Architecture of Voltage Monitoring Input

The outputs of the comparators are connected to the on-chip CPLD. The logic gate between the comparators enables window comparison, and this output can be routed to the CPLD instead of the comparator output.

VMON comparator outputs can be made immune to glitches of up to 64 microseconds by turning the glitch filter on.

The comparator output status also can be monitored through the I^2C interface.

Voltage Measurement Through 10-bit ADC

The Power1220AT8 provides a 10-bit Analog to Digital Converter (ADC) and a 14 input analog multiplexer to measure voltages on VMON Pins. The functions of the ADC are:

1. Measuring the voltage of any VMON input pin through the I^2C bus.

2. The digital closed loop trim hardware uses the ADC to measure the power supply voltage to compare with the set point voltage.

To facilitate voltage measurement up to 6 V, a 3:1 attenuator is provided at each VMON input

Margin / Trim Block

A key feature of the ispPAC-POWR1220AT8 is its ability to make adjustments to power supplies that it also may be monitoring and/or sequencing. This is accomplished through the Margin and Trim Block (MTB) of the device. The MTB can adjust the voltages of up to eight different power supplies through TrimCells, as shown in Figure 4. The DC-DC blocks in the figure represent virtually any type of DC power supply that has a trim or voltage adjustment input. This can be an off-the-shelf unit, or a custom circuit designed around a switching regulator IC.

To simplify the diagram, a single resistor, R1 – R8, represents the interface between the ispPAC-POWR1220AT8 and the DC power supply. Each of these resistors represents a resistor network.

Other control signals driving the Margin / Trim Block are:
- VPS [1:0] – Control signals from device pins common to all 8 TrimCells, which are used to select the active voltage profile for all the TrimCells.
- PLD_VPS [1:0] – Voltage profile selection signals generated by the PLD. These signals can be used instead of the VPS signals from the pins
- ADC input – used to determine the trimmed DC-DC converter voltage
- PLD_CLT_EN (only from the PLD) – is used to enable closed loop trimming of all TrimCells together

Next to each DC-DC converter, four voltages are shown. These voltages correspond to the operating voltage profile of the Margin / Trim Block.

When VPS [1:0] = 00, representing voltage profile 0 (voltage profile 0 is recommended for normal circuit operation), the output voltage of the DC-DC converter controlled by Trim 1 pin of the ispPAC-POWR1220AT8 will output 1V

and that TrimCell will operate in closed loop trim mode. At the same time, the DC-DC converters controlled by Trim 2, Trim 3 and Trim 8 will output 1.2V, 1.5V & 3.3V, respectively.

When VPS [1:0] = 01, representing Voltage profile 1 being active, the DC-DC output voltage controlled by Trim 1, 2,3, and 8 pins will be 1.05V, 1.26V, 1.57V, & 3.46V. These supply voltages are 5% above their respective normal operating voltage (Also called Margin High).

Similarly, when the VPS [1:0] = 11, all DC-DC converters are Margined Low by 5%.
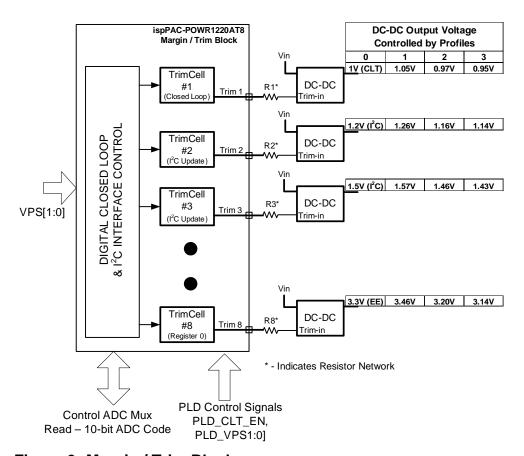

Figure 3- Margin / Trim Block

Voltage Profile Control

The Margin / Trim Block of the ispPAC-POWR1220AT8 consists of eight TrimCells. Because all eight TrimCells in the Margin / Trim Block are controlled by two common voltage profile control signals, they all operate at the same voltage profile. These common voltage profile control signals are derived from a Control Multiplexer. One set of voltage profile control inputs to the control multiplexer is from a pair of device pins: VPS0, VPS1. The second set of voltage profile control inputs is from PLD: PLD_VPS0, PLD_VPS1. Selection between the two sets of voltage profile control signals is programmable and the selection is stored in the E^2CMOS memory.
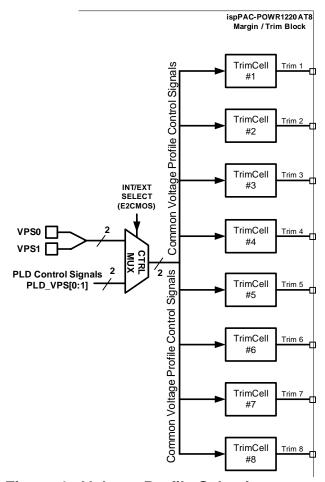

Figure 4 - Voltage Profile Selection

TrimCell Architecture

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Figure 5 shows the architecture of a TrimCell. Each TrimCell has an output 8-bit DAC and there are 6 registers to store DAC codes. Of these 6 DAC registers, four are non-volatile (DAC-Register [0: 3] and their contents are determined at program time and 2 are volatile (DAC-Register I^2C & Closed Loop Trim Register) and their contents either can be dynamically loaded through the I^2C interface or automatically controlled by Closed Loop circuitry. Common Voltage Profile control signals select the DAC Registers. The voltage profile 0 (when VPS [0:1] = '00') has three modes of operation: DAC-Register 0, DAC-Register I2C, and Closed Loop Trim Register.
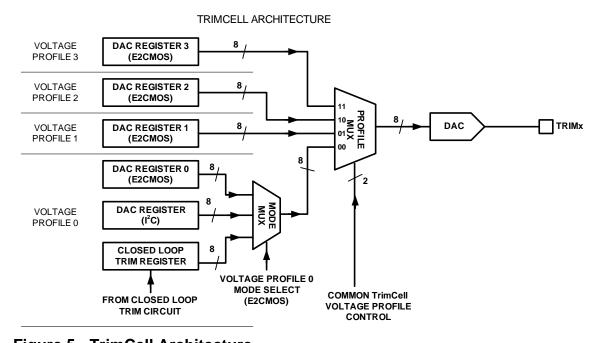
TRIMCELL ARCHITECTURE

Figure 5 - TrimCell Architecture

Digital Closed Loop Operation:
Accurate DC-DC Converter Voltage Control

This mode of operation is used to accurately maintain the output voltage of a DC-DC converter to a set point. In this mode, the voltage set register for a TrimCell is programmed to a desired voltage. The power supply voltage is monitored by the internal hardware using the ADC, and is compared with the voltage set by the

set point register. The Power1220AT8 will then increase or reduce the DAC code at regular intervals until the output voltage of the DC-DC converter is equal to the voltage set point.
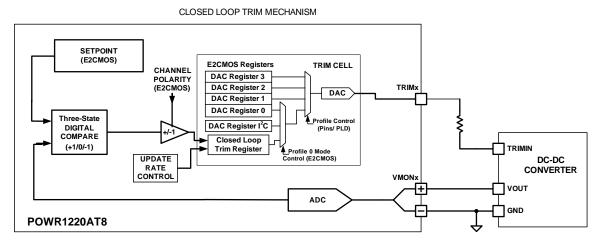
CLOSED LOOP TRIM MECHANISM

Figure 6 – TrimCell Operating in Digital Closed Loop Trim Mode

Dynamically Update the DAC Code from the I^{2}C Port

This mode is used for external closed loop control of the power supply voltage. A microcontroller monitors the output voltage of the DC-DC converter and adjusts the power supply output voltage by altering the DAC code.

Timers

There are 4 programmable long duration timers in a Power1220AT8 device. These timers can be programmed between 32 microseconds and 2 seconds in 128 steps. PLD outputs can directly control these timers, and the timer output can be monitored by the PLD. Timers can be used to control the power supply sequencing delay to time out various processes, including use by the software as a watchdog timer. The same timer can be used within a design multiple times.

CPLD

The Power1220AT8 device has a 48-macrocell ruggedized CPLD on chip. This CPLD is used to implement all the power management functions using the LogiBuilder software, which is included with PAC-Designer version 4.0

I^{2}C Interface

The Power1220AT8 device implements a slave I^{2}C mode of operation. The I^{2}C address can be programmed for any standard slave address using the JTAG port.

The I^{2}C interface of the Power1220AT8 can be used for:

- Reading the status of all comparators, digital inputs and outputs

- Measuring voltages

- Reading the DAC Code after the digital closed loop is stable

- Loading the DAC code for any TrimCell

- Controlling five of the 6 inputs (Inputs can be programmed to be controlled by either the pin or I^{2}C commands)

- Resetting the device

- Resetting SMBusAlert status

The I^{2}C interface also can be programmed to be compatible with SMBus functions.

Application Example: ATCA Payload Power Management

Circuit Diagram
Figure 7 shows typical Payload power management in an Advanced TCA (ATCA) Field Replaceable Unit (FRU).
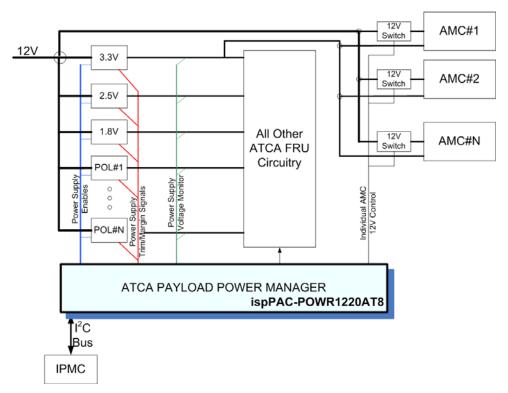
Figure 7 - Power Management Circuit of an ATCA FRU

The card uses an isolated power supply to generate 12 Volts from the -48V backplane supply. All power supply voltages required for the Payload section of the FRU are derived from the 12V bus. The Power1220AT8 (ATCA Payload Power Manager) and the microcontroller Intelligent Platform Management Controller (IPMC) are powered by a management supply separately generated within the circuit board.

A multiple sequence control design implemented in the ispPAC-POWR1220AT8 simultaneously supports communication with the IPMC as well as the Payload power management.

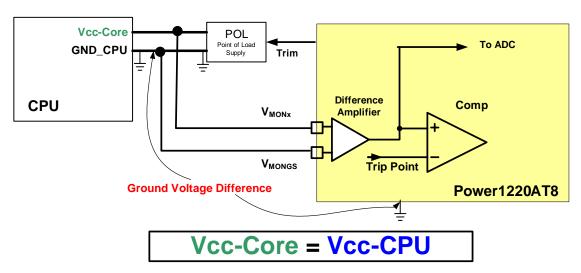The IPMC commands implemented are:

- Turn Payload supplies on

- Turn Payload supplies off

- Watchdog timer trigger

The Payload power management includes the Payload power sequencing, monitoring, generation of Reset, Watchdog trigger management for the Payload CPU, and power supply trimming

Differential Voltage Sensing Results in Accurate Control of Output Voltage

Figure 8 shows the Power1220AT8 device sensing a power supply voltage using its differential inputs (V_{MONx} input pin to sense the power supply positive voltage pin, and V_{MONGS} to sense the power supply ground pin). The differential amplifier at the input of the Power1220AT8 subtracts the voltage on its V_{MONGS} from the V_{MON}. This effectively eliminates the effect of ground voltage differences. Consequently, the monitoring accuracy as well as voltage measurement accuracy will be immune to ground voltage differences.

Additionally, the POWR1220AT8 is used for trimming the power supply voltage. Because the voltage measurement accuracy is independent of the ground voltage difference, the calculated trim voltage to set the DC-DC converter's supply voltage also will be accurate.

Ground Voltage Difference is the instantaneous Voltage difference between the GND_CPU and Power Manager Ground
Vcc-CPU is the required CPU voltage
Vcc-Core is the Actual, Trimmed Supply Voltage

Figure 8: Differential Sensing Results in Accurate Power Supply Trimming

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On the other hand, single ended monitoring / measurement is prone to error due to ground voltage differences. Competitive devices from SummitMicro, Analog Devices and Potentia resort to single ended voltage monitoring, and it is very difficult to design accurate power supply management circuits using these devices.

PAC-Designer Software

Lattice's PAC-Designer Version 4.0 software supports the ispPAC-POWR1220AT8 device. There are a number of new features in Version 4.0

LogiBuilder

The embedded LogiBuilder software module in PAC-Designer supports the implementation of multiple control sequence algorithms, such as the IPMC command response, Payload power management and AMC management required in ATCA applications. Designers are able to implement complex algorithms using 7 types of instructions. With an extremely intuitive design flow, users can learn its operation and complete designs in minutes.

Margin / Trim Utility

The Power1220AT8 can margin up to 8 power supplies. Figure 9 shows the circuit required to drive a DC-DC converter from the Trim pin of the POWR1220AT8 device. For a given DC-DC converter and the output voltage under different voltage profiles, the Margin / Trim utility calculates the values of all resistors.
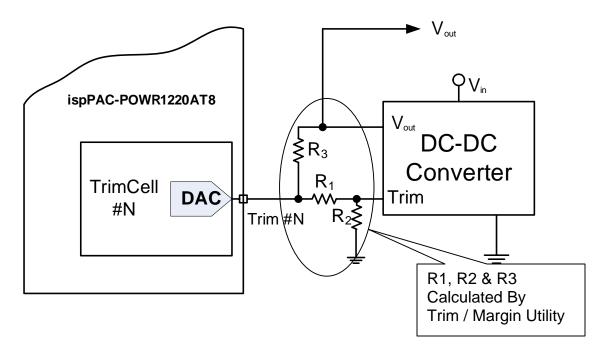
Figure 9 – TrimCell Driving a DC-DC Converter

DC-DC Library Utility

This utility enables the modeling of a DC-DC converter for use by the Margin / Trim utility for resistor calculation. The user can create the DC-DC library by using the configuration example in the DC-DC converter datasheet. The Margin / Trim Utility can use the latest power supply library entry and calculate the values of R1, R2, and R3 directly.

I^2C Utility

This utility can be used with an ispPAC-POWR1220AT8 evaluation board. Through a simple and intuitive user interface, the utility enables reading the status of comparators, inputs, outputs, making VMON voltage measurement, control inputs, outputs, etc.

HVOUT Simulator

This simulator can be used to calculate the power supply ramp rate for a given HVOUT current setting, type of MOSFET, and load current. Users can also add to the list of MOSFETs in the library by using the MOSFET specification table.

POWR1220AT8 Provides Reliable Power Management Solution

Differential voltage sensing provides accurate and repeatable power supply voltage monitoring and measurement. LogiBuilder-based design software implements the complete power management algorithms. The resulting design is implemented in a ruggedized CPLD that can operate in a noisy power supply environment. Power supply trimming, coupled with differential voltage sensing and digital closed loop mode of operation, tightly controls the DC-DC converter output voltage. Because all the blocks required for the implementation of a complete power management function are integrated on one chip, the ispPAC-POWR1220AT8 further increases board reliability through reduced component count and circuit board space.

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