MachXO Starter Evaluation Board

Ready-Made Platform for MachXO256 – Includes AC Adapter & Download Cable

The MachXO™ Starter Evaluation Board is a complete working solution for the MachXO crossover programmable logic technology. Efficiently packed with a rich set of features, the MachXO Starter Evaluation Board is a simple, yet versatile solution allowing for detailed analysis of the MachXO performance and technology. The board is also a convenient platform to help you get started with your own MachXO design.

Efficient and Flexible Design

The MachXO Starter Evaluation Board is packed with basic building blocks that can be used to demonstrate any number of programmable logic features or functions:

I/O Evaluation

Measure the drive strength, speed, and switching characteristics of the MachXO I/Os, configured to whatever specification you program.

Measure Power Consumption

Check the actual power consumption of a MachXO design, see how changes in your design, and various MachXO settings, affect power results.

In-System Evaluation

Use the prototype area to connect to any number of instruments or see how the MachXO interfaces with other technology.

Discover Lattice Technology

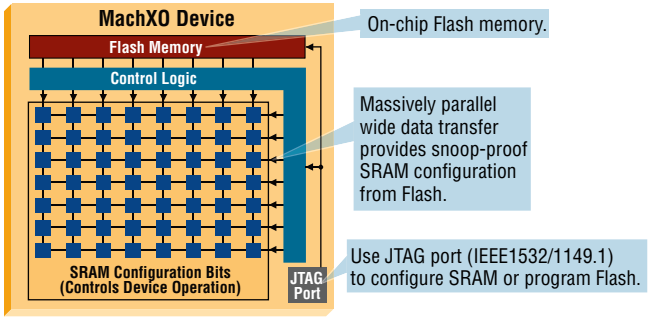
The MachXO Starter Evaluation Board, along with downloadable software tools, give you everything you need to evaluate the entire Lattice design flow without making a huge investment.

MachXO – Crossover PLD

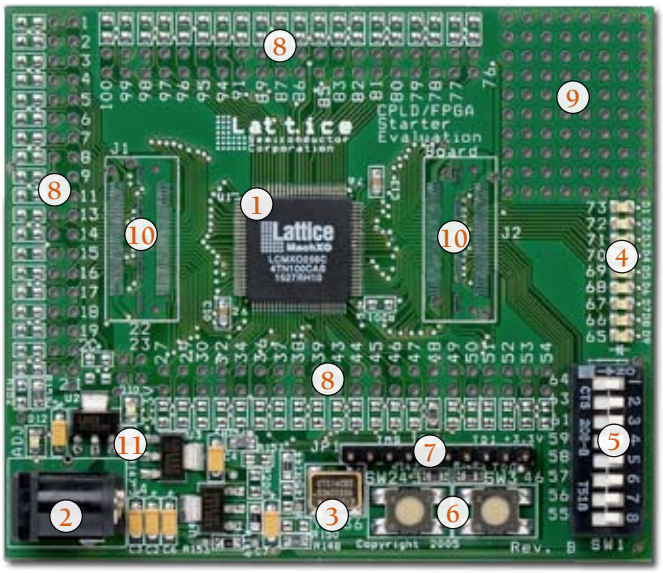
The MachXO family of non-volatile, infinitely reconfigurable Programmable Logic Devices (PLDs) is designed for applications traditionally implemented using CPLDs or low-capacity FPGAs.

The MachXO family combines an optimized Look-Up Table (LUT) fabric with Lattice's ispXP™ technology to provide the high pin-to-pin performance and instant-on associated with CPLDs, with the flexibility of FPGAs, all in a single low-cost device.

MachXO Configuration



MachXO Starter Evaluation Board (actual size)



Key Features

1. MachXO device (LCMXO256C-4T100C)
2. Power input jack
3. 33MHz oscillator
4. Status LEDs, and 9 I/O LEDs
5. 8-bit input switch
6. 2 push-button switches
7. JTAG programming interface
   - Download cable included (HW-DL-3C)
8. Access to all device I/O
9. Prototyping area
10. Landing pads for off-board expansion connectors
11. On-board power control
    - AC adapter included

Ordering Information

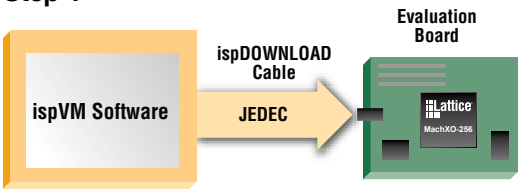
Product	Description	Ordering Part #
MachXO Starter Evaluation Board	MachXO evaluation board with LCMXO256C-4T100C device, ispDOWNLOAD® Cable, and AC adapter	LCMXO256C-S-EV

Only $99!
Order online or call your local Lattice representative

Demo Example: Re-programming without System Interruption

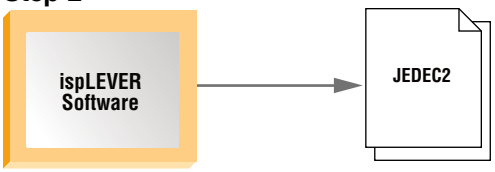
Lattice's Transparent Field Reconfiguration (TransFR™) feature enables the MachXO to be re-programmed without significant system interruption. This unique capability can be easily demonstrated with the MachXO Starter Board.

Step 1



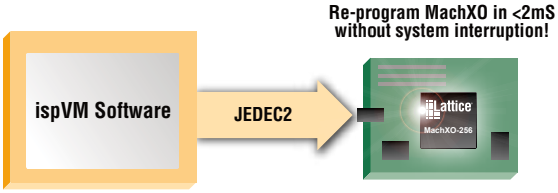
Program the MachXO device on the Evaluation Board with the sample program (JEDEC file) using the ispVM System software, and the ispDOWNLOAD Cable.

Step 2



Use the ispLEVER Design Tools to modify the sample program (e.g. reverse the counter), and generate a second, modified JEDEC programming file. (JEDEC2)

Step 3



With the ispDOWNLOAD Cable still attached, use the ispVM System software to perform a TransFR operation to the MachXO device, programming the Flash Block on the MachXO with the modified JEDEC file, while the FPGA operates. The new program can then be loaded to the SRAM when convenient, for seamless function changeover.

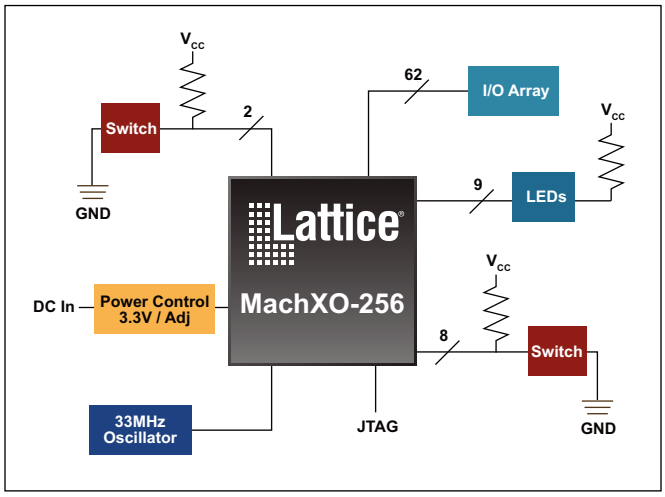
Demo Requirements

- MachXO Starter Evaluation Board Package
- ispVM™ System Software and ispLEVER® software (downloadable from www.latticesemi.com/software)
- MachXO Starter sample program (downloadable from www.latticesemi.com/boards)

More Information

For additional information on this example, see tech note TN1087, available on the Lattice website.

MachXO Starter Block Diagram



ispLEVER Design Tools

Lattice's ispLEVER development tools offer a comprehensive design environment for the MachXO architecture. ispLEVER tools include everything you need for design entry, synthesis, map, place & route, floorplanning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Mentor Graphics and Synplicity are included with ispLEVER.

MachXO devices are supported by Lattice's ispLEVER Starter software. Download a free copy of ispLEVER Starter software at www.latticesemi.com/starter.

ispLeverCORE™ Intellectual Property

Lattice offers an expanding portfolio of IP cores to support the easy integration of commonly used functions. For the MachXO this includes reference designs to address:

- PCI Target
- SDRAM Memory Controllers
- I^2C Controller

ispLever™ CORE

For more information on Lattice IP cores, go to www.latticesemi.com/ip.

Lattice Evaluation Boards

Lattice designs and manufactures a broad range of evaluation boards for Lattice programmable products. For further details, including a summary of available boards and kits, go to the Lattice website at: www.latticesemi.com/boards.

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