THE APPLICATION OF PROGRAMMABLE LOGIC TO A MIXED-SIGNAL POWER MANAGEMENT DEVICE

A Lattice Semiconductor White Paper

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Multiple Power Supply PCB Challenges

Advanced integrated circuits, such as communications processors, achieve increased performance, added functionality and reduced power consumption when fabricated using the latest sub-micron technologies. This results in reduced operating core voltages. Increasingly, inter-device communications standards also require the use of a variety of I/O supply voltages. These factors result in multi-voltage devices with multiple power supply requirements.

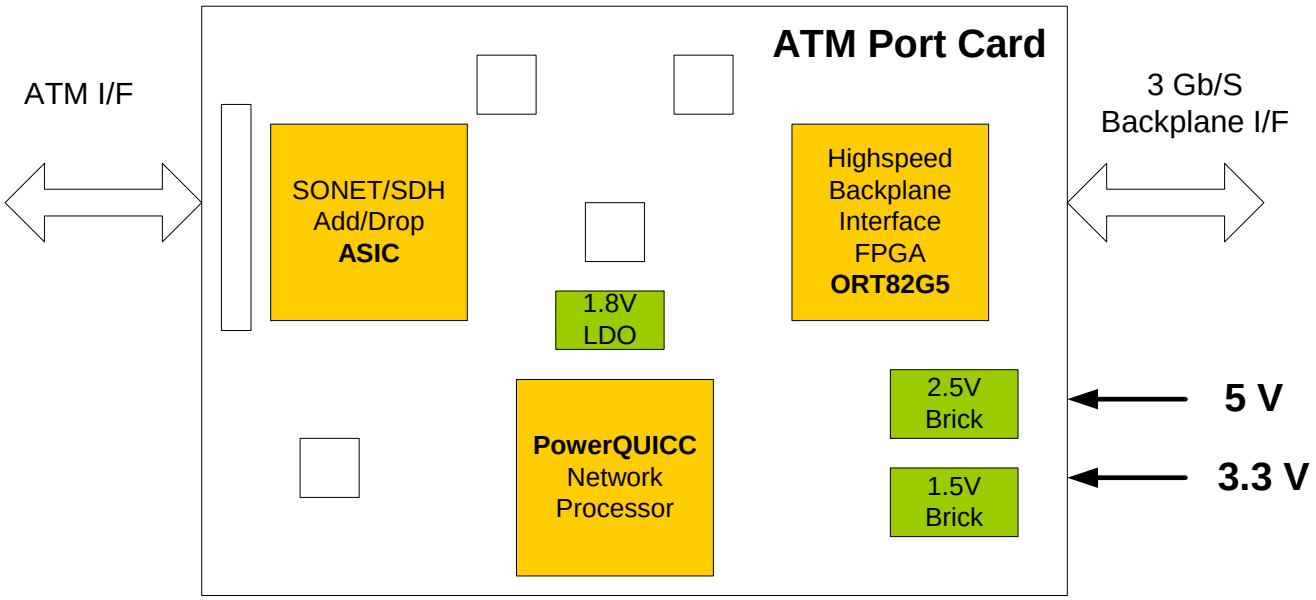

Figure 1 - ATM Port Card with Multi-Voltage Devices

Figure 1 shows the devices used on a typical ATM port card along with its backplane interface and power supplies. Table 1 summarizes the power supply requirement of these multi-voltage devices.

The power supply requirement of each device, taken separately, is easy to implement; however, satisfying the cumulative power supply requirements on this ATM port card can be quite a complex process.

Device	Supplies Required	Sequencing & Tracking	Additional Requirements
PowerQUICC CPU	1.8V-Core & 3.3V-I/O	Voltage difference between core and I/O should not exceed 400 mV during power-up or down 1.8V should track 3.3V	CPU_Reset should be active for at least 50 ms after the supplies stabilize
ORT82G5 FPSC	1.5V Core, 3.3V I/O	Core voltage should be present before I/O voltages ramp. Power supplies should ramp monotonically 1.5V 1st & 3.3V Next	
SONET ASIC	2.5V Core, 3V3 I/O	Highest voltage first & core voltage last 3.3V first, 2.5V next	

Table 1 – Power Supply Requirements for Individual Devices

Apart from the requirements of individual devices, the design also calls for monitoring power supply voltages during normal operation. If any supply voltage falls below threshold, the CPU should be reset and the power supply to all devices should be recycled.

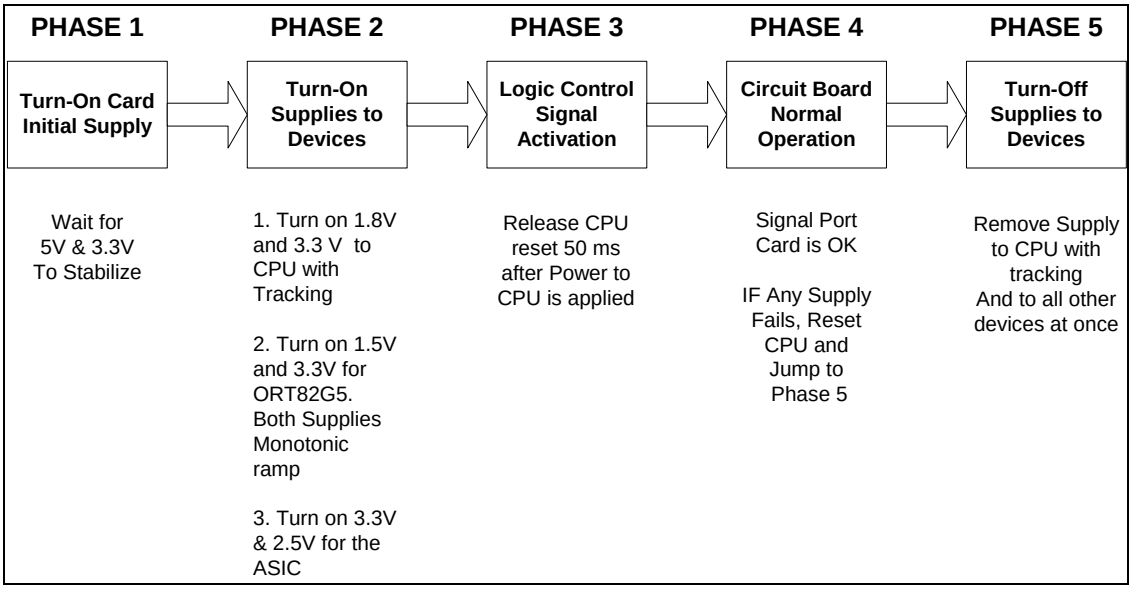

Figure 2 - Five Power Supply Phases of the ATM Port Card

Five Phases of System Power Supply Activity

Overall system power supply activity can be subdivided into the 5 phases shown in Figure 2.

Phase 1: The ispPAC Power Manager device waits for the 5V and 3.3V inputs to the card to stabilize, using the signals Good_Input_5V signal and Good_Input_3V3, respectively.

Phase 2:

A. 1.8V LDO and 1.5V FET are turned on together. This will power the core of the CPU through the schottky diode (connected between the CPU's I/O and its core). The I/O voltage also closely follows the core voltage, meeting the tracking requirement. At the same time, the power supply to the ORT82G5 core also monotonically ramps up.

B. Once the 1.8V and 1.5V sources stabilize, the 3.3V supply is turned on through both MOSFETs Q1 and Q3. Initially, the CPU's I/O pin stays at 1.8V through the schottky diode. When the 3.3V source raises above 1.8V, the schottky diode is automatically turned off and the I/O pins follow the 3.3V MOSFET Q1's output. The exact waveform is shown in figure 5. Simultaneously, 3.3V is applied to both the ASIC and the ORT82G5 devices through the MOSFET Q3.

C. After the 3.3V stabilizes at the ORT82G5 and the ASIC I/O supply, the 2.5V brick is turned on, meeting the supply sequence requirement of the SONET ASIC.

Phase 3: After ensuring the 3.3V and 1.8V at the CPU are stable, a 60 ms timer is started. After that timer has expired, the CPU_Reset signal is de-asserted. This results in stretching of the reset pulse for the CPU.

Phase 4: The card signals the main controller that the card is turned on correctly. This is done by asserting the Port_Card_OK signal. Subsequently, all power supply voltages are monitored continuously for faults. When faults occur (i.e., one of the supplies falls below a defined Vccmin threshold), the CPU_Reset signal is asserted and the device logic transitions to Phase 5.

Phase 5: Here the power supplies for the ASIC and ORT82G5 devices are turned off immediately. In order to meet the power supply turn off tracking requirement, the following steps are implemented:

A. Turn off the 3.3V to the CPU and simultaneously turn on the shorting FET (Q2), shorting the CPU's I/O pins to core voltage.

B. Wait a few milliseconds for the I/O decoupling capacitors to discharge.

C. Turn-off the core voltage (1.8V) to the CPU.

Power Supply Management of ATM Port Card

Complete power supply management of this ATM port card, implemented using the ispPAC-POWR1208 device, is shown in the circuit diagram below (Figure 3).

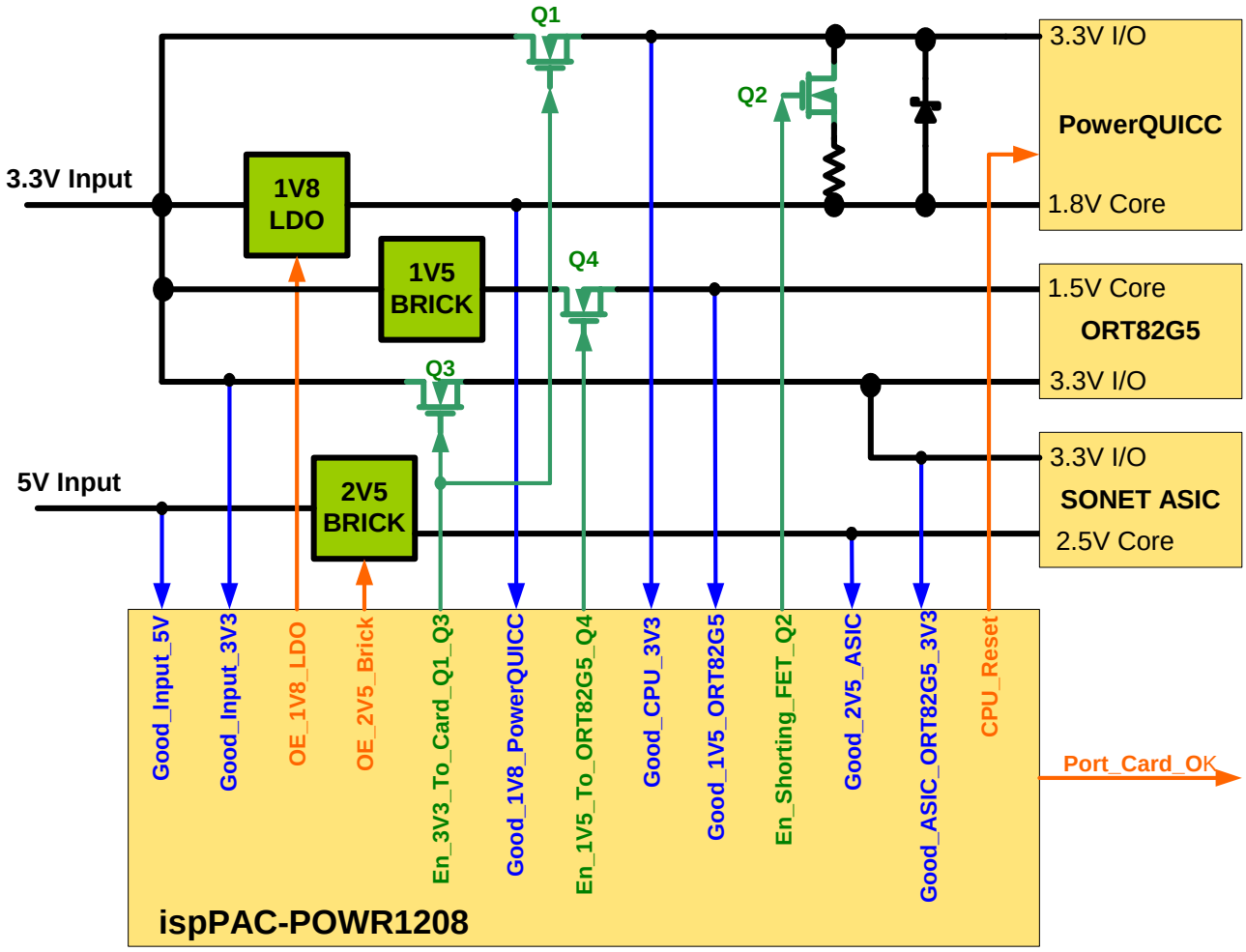

Figure 3 – Power Management of the ATM Port Card Using ispPAC-POWR1208

The tracking requirement of the PowerQUICC network processor can be implemented using the bootstrapping method. However, that method results in a non-monotonic ramp of 3.3V at the CPU's I/O pins. While that non-monotonic ramp is not a problem for the CPU, it does not conform to the ORT82G5's power supply requirement. Consequently, it is necessary to route the 3.3V through another power supply MOSFET. The power supply sequence of the SONET ASIC is opposite to that of the sequence of the CPU and ORT82G5. To address all requirements simultaneously, 5 power supply busses are needed:

1. 1.8V supply, generated using 1.8V LDO (Low Drop Out regulator) for CPU's core.
2. 3.3V for CPU's I/O is fed through the MOSFET Q1. To facilitate independent ramp rate control, MOSFET Q3 is also driven by the same signal.
3. 1.5V for the core of ORT82G5 is generated using the permanently enabled 1.5V brick (DC-TO-DC Converter). The MOSFET Q4 is used to provide monotonic ramp for the core supply.
4. 3.3V for the ORT82G5 and SONET ASIC is supplied through the MOSFET Q3. This supply is enabled along with the 3.3V of the CPU.
5. 2.5V for the SONET ASIC is generated using a 2.5V brick sourced from the 5V backplane source. The enable signal is controlled to meet the sequencing requirement of the ASIC.

As can be seen, the ispPAC Power Manager device controls the sequencing and monitoring of power supplies efficiently while generating required supervisory signals. Understanding the features and capabilities of the ispPAC Power Manager device greatly helps design implementation with the PAC-Designer software.

Implementing Power Supply Management on the ATM Port Card Using PAC-Designer Software

Power supply sequencing and monitoring designs can be implemented on Power1208 devices using Lattice PAC-Designer software. PAC-Designer software is an intuitive, PC-based schematic design entry and simulation tool. The user can easily design complex sequencing and monitoring functionality by using PAC-Designer's newest feature,

LogiBuilder™, which uses a series of easy-to-use pull down menus to define which sequences and conditions to monitor.

To implement the design using the PAC-Designer software:

1. Set **Monitoring** threshold values for each analog input by selecting the appropriate threshold value from a pull down menu.

2. The **Power Supply Ramp Rate Control** is implemented by setting the MOSFET gate drive characteristics for the HVOUT outputs. This is set by a pull down menu as well.

3. Power Supply Sequencing, Tracking and Supervisory Signal Generation Logic can be defined easily using just five point-and-click instructions in the LogiBuilder section.

4. Verification using PAC-Designer's waveform simulator can verify the completed design.

5. ispDOWNLOAD to Power1208 Device. The complete and verified design can be downloaded to the **Power1208** device through its JTAG port.

Tables 2 and 3 summarize the input and output pin configuration and interface specification of the ispPAC-POWR1208.

Datasheet Pin Name	Configured Pin Name	Pin Configuration	Description
VMON1	Good_ASIC_ORT82G5_3V3	Threshold –3.147V	3.3V-5%ASIC and ORT82G5 I/O supply threshold
VMON2	Good_2V5	Threshold – 2.384V	2.5V –5% threshold level for ASIC core voltage monitor
VMON3	Good_1V8_PowerQUICC	Threshold – 1.715V	1.8V-5% threshold level for PowerQUICC processor
VMON4	Good_Input_5V	Threshold – 4.76V	5V-5% threshold for the card power supply input
VMON5	Good_Input_3V3	Threshold – 3.147	3.3V-5% threshold for the card power supply input
VMON6	Good_1V5_ORT82G5	Threshold – 1.429V	1.5V-5% threshold for the ORT82G5 core voltage
VMON7	Good_CPU_3V3	Threshold – 1.429	1.5V-5% for the CPU's I/O supply

Table 2 - ispPAC-POWR1208 Power Management Input Pin Configuration

	OUTPUTS		
HVOUT1	EN_3V3_to_Card_Q1_Q3	10V output with 18 uA Gate Current	Enables MOSFETs Q1 and Q3 to supply 3.3V to all devices
HVOUT2	En_Shorting_FET	10V output with 50uA Gate Current	This is turned on during power down tracking of CPU supply
HVOUT3	En_1V5_to_ORT82G5_Q4	10V output with 18 uA Gate Current	MOSFET drive to supply 1.5V to ORT82G5 core voltage
OUT5	OE_2V5_Brick	Open Drain	Enables 2.5V brick for ASIC
OUT6	OE_1V8_LDO	Open Drain	Enables 1.8V LDO for CPU
OUT7	CPU_Reset	Open Drain	CPU reset during power an and during fault
OUT8	Port_Card_OK	Open Drain	Signals to the main system that the ATM port card has successfully powered on

Table 3 - ispPAC-POWR1208 Power Management Output Pin Configuration

Once the interface to the power supply busses and the MOSFET are specified, the actual power supply sequencing and monitoring steps are designed using the LogiBuilder.

The complete power supply management program is implemented in 14 steps as shown by Figure 4.

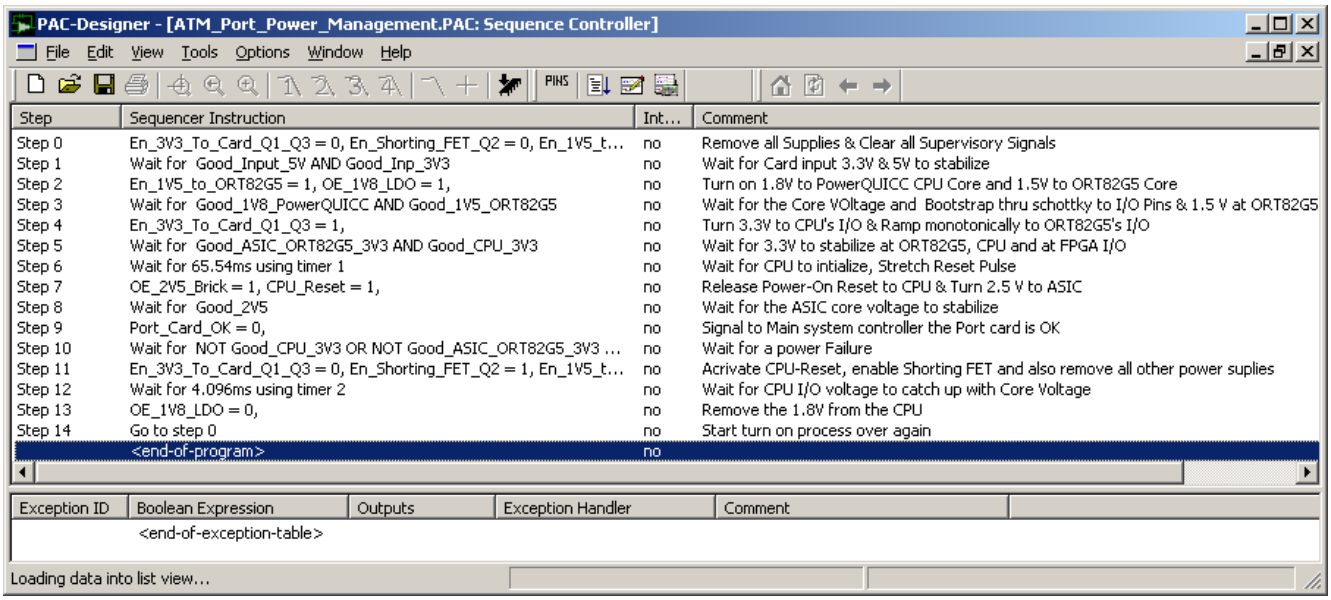

Figure 4 - LogiBuilder Program for ATM Port Card Power Management

The LogiBuilder program steps that correspond with the 5 power supply phases of power management are:

Phase 1 – Step 0 and Step 1 – Waiting for input power supplies to stabilize
Phase 2 – Step 2 to Step 8 – Applying the correct power supply to each device
Phase 3 – Step 6 and Step 7 – Pulse stretching of CPU-Reset
Phase 4 – Step 9 and Step 10 – Card normal operation
Phase 5 – Step 11 to Step 13 – Turning the power supply off

This LogiBuilder program is then compiled and the resulting JEDEC file is downloaded into the ispPAC Power Manager device through its JTAG pins.

The design was implemented and the following oscilloscope screen shot, figure 5, shows the I/O voltage tracking the core voltage during power supply Ramp up.

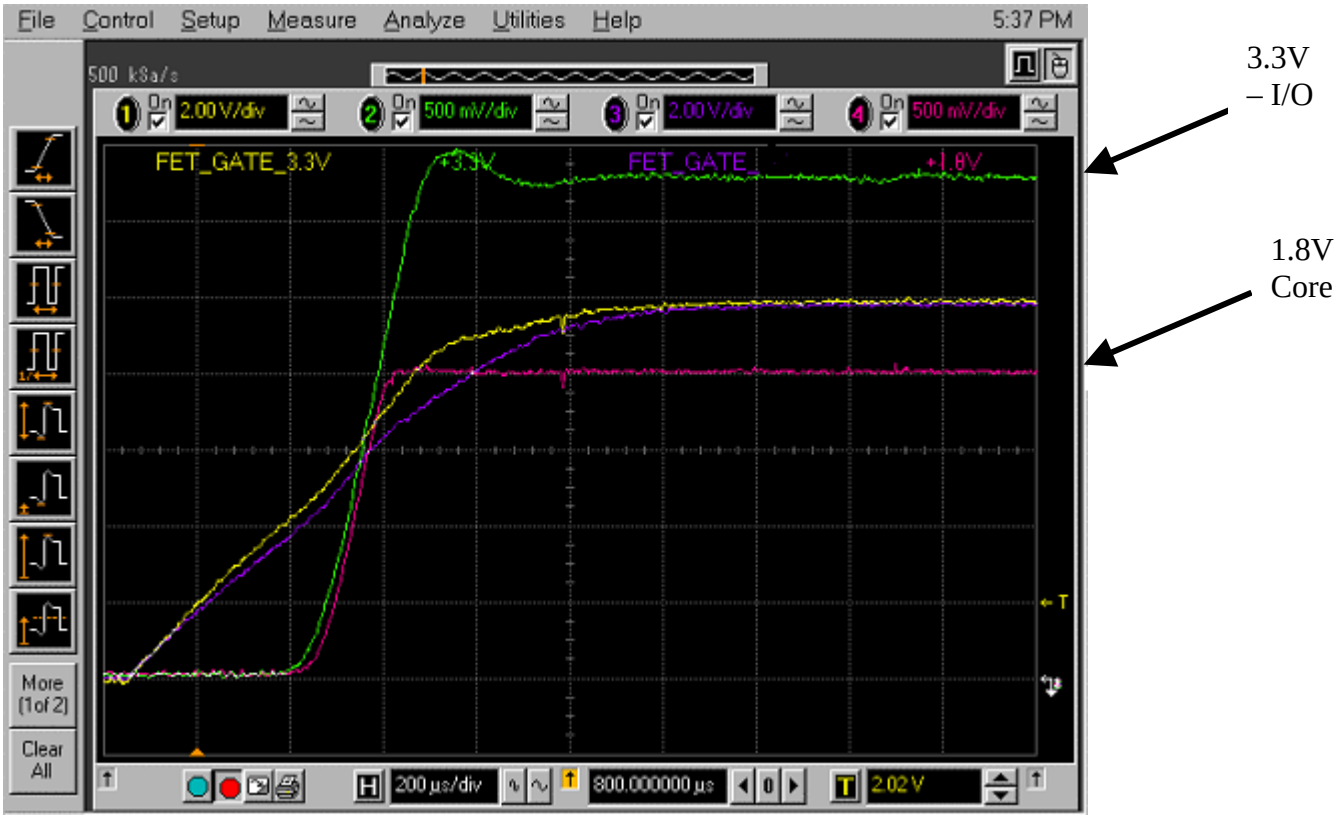

Figure 5- Oscilloscope Waveform Showing 1.8V and 3.3V Tracking at PowerQUICC Processor

Conclusion

Viewed separately, the power supply sequencing and monitoring requirements of each multi-voltage device on a circuit board seem easy to implement. However, the task becomes quite complex when the requirements of all devices on the circuit board are viewed collectively.

Consequently, a circuit board with several multi-voltage devices requires a separate power supply manager. The ispPAC-POWR1208 device satisfies the requirements of individual circuit board designs through programmability.

The PAC-Designer software, with its easy-to-use pull down menus, supports interfacing the ispPAC Power Manager device to various power supply arrangements. Power supply management algorithms can be specified quickly using the LogiBuilder's 5 basic instructions.

The integration and programmability of the ispPAC-POWR1208 device, coupled with the easy-to-use and intuitive PAC-Designer software tool, reduce board space, reduce time to market and increase circuit board reliability.

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