ispPAC® Power Manager

White Paper

May 2003

Lattice – Bringing the Best Together

ispPAC Power Manager

The First Mixed-Signal PLD

Overview

Lattice Semiconductor has been a key industry innovator in providing advanced programmable digital device solutions. During the mid-80's, Lattice introduced the CMOS re-programmable GAL® architecture to replace early fuse-based PLDs and TTL logic. At the end of the 1980's, Lattice's in-system programmable (ISP™) CPLD architecture provided benefits to both design and manufacturing engineers that set an industry standard for all CPLDs to come. Similarly, ispGDX®, a family of programmable interconnect and interface devices introduced in the mid-90's, provided dramatic reductions in circuit board area by replacing the numerous discrete ICs required to implement on-board interfaces. Lattice's recent introduction of the first non-volatile, "instant on", yet infinitely reconfigurable FPGAs, the ispXPGA™ family, further enhances this reputation for programmable logic innovation.

Leading the way to provide the benefits of ISP to the analog designer as well, Lattice has been developing and bringing to market the concept of the in-system programmable analog circuit (ispPAC®). Analog engineers traditionally have used basic building blocks to implement analog functions, similar to digital engineers using TTL to design logic circuits during the 1980's. The only way to design analog circuits was by wiring up a breadboard or prototype circuit board in the lab. With the introduction of Lattice's first ispPAC® devices 3 years ago, all that changed. Analog engineers can now harness the convenience of ISP, like their digital peers, by implementing their analog designs and verifying their functionality employing easy-to-use PC-based software. The final configuration, once debugged through simulation, can be stored in the on-chip EEPROM memory of the ispPAC device much as a standard PLD is programmed today. Lattice has since introduced 5 programmable analog products for a variety of analog tasks including signal conditioning, filtering and general-purpose use.

Now, by combining the ispPAC programmable analog and ispMACH® programmable logic technologies, Lattice has created the world's first mixed signal PLD, **ispPAC Power Manager family**, to provide unprecedented single chip functionality for implementing on-board power supply management solutions. By doing so, Lattice is providing a new power supply control approach for addressing control tasks within the almost $13 Billion power semiconductor market.

The ispPAC Power Manager family consists of the ispPAC-POWR1208 (**Power1208)** and ispPAC-POWR604 (**Power604**) devices. These devices offer flexible, cost effective and convenient implementation of power supply sequencing, monitoring, and supervisory functions for any printed circuit board using multiple voltage supplies.

The Power604 provides cost effective solution for supervisory signal generation function with limited supply sequencing. Whereas the Power1208 device provides for total power supply management including, power supply sequencing, tracking, and the generation of supervisory signals.

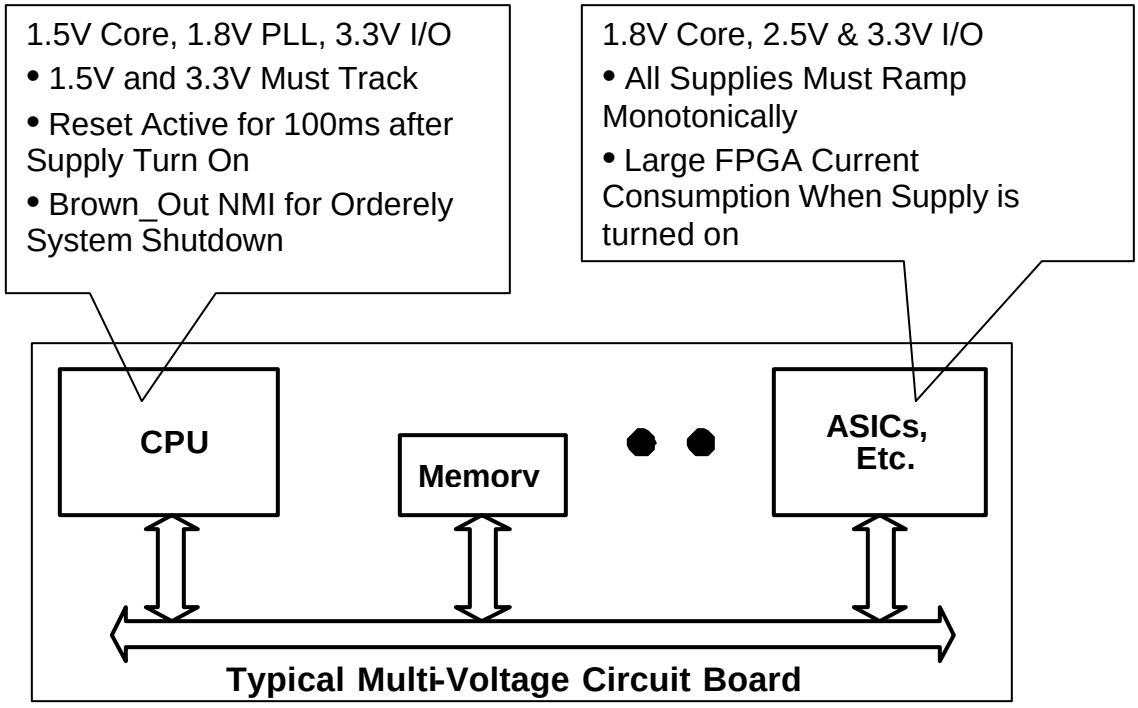

Figure 1 – Power supply issues on a typical circuit board

Multiple Power Supply PCB Challenges

Advanced integrated circuits such as communication processors achieve increased performance, added functionality, and reduced power consumption by being fabricated using the latest sub-micron technologies. This also results in reduced operating core voltages. Inter-device communication standards, however, often dictate the use of certain I/O supply voltages. This results in devices with multiple power supplies. These devices are called multi-voltage devices.

Many multi-voltage devices also require that their power supplies be turned-on or sequenced in a particular order (e.g., the core voltage should be turned on before the I/O supply voltage). Some devices also require that the I/O voltage should be within a given voltage range of the core voltage during turn on (also referred to as 'power supply tracking').

Figure 1 summarizes some of the design challenges an engineer faces when developing a power control system. While the individual functions may be easy to implement in isolation, satisfying the power supply requirement (sequencing, controlling ramp rate, generating supervisory signals, etc.) for all the devices on the circuit board present a significant challenge for today's board designers. **The Power1208 is the world's first device capable of providing all of these power supply management functions in a single chip.**

Power Manager Architecture

The Power1208 and Power604, packaged in 44-pin TQFP packages, provide the following programmable modules to implement sequencing and monitoring functions:

- On-board ispMACH sequence controller CPLD
- Delay timers (for sequence delays and watchdog timers)
- Internal oscillator for precision timing and clocking the CPLD
- Multiple analog inputs with programmable precision analog threshold
- Buffered comparator outputs
- Programmable N-channel MOSFET drivers (Power1208 only)
- General-purpose open-drain digital logic outputs
- General-purpose logic inputs

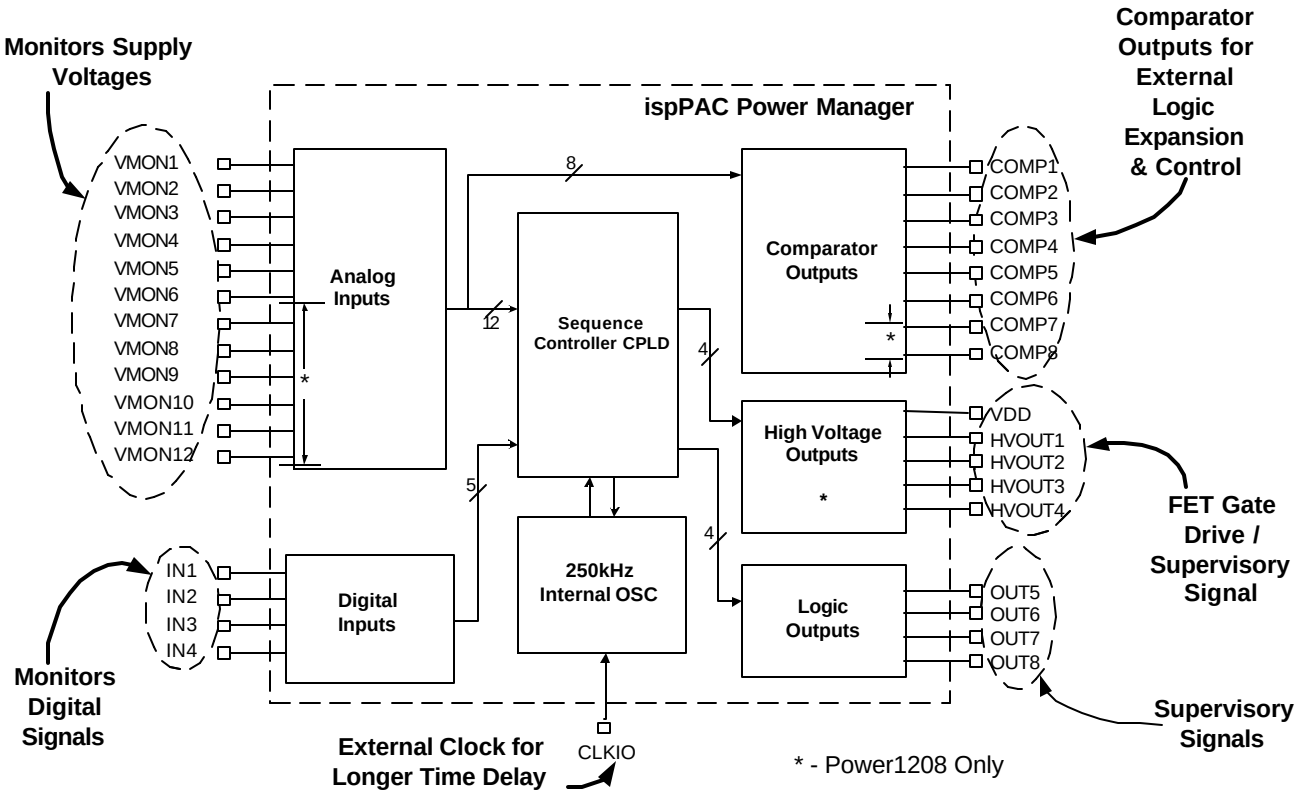

Figure 2. Power Manager – Block Diagram

The Power Manager's embedded CPLD is derived from that of the ispMACH4000 CPLD. The analog inputs (each providing a precision programmable threshold comparator) and 4 general-purpose digital inputs are connected to the input of the CPLD's AND-array. All the outputs are routed to output pins through the output routing pool. The remaining Macrocells can be used for implementing state machines for power sequencing, generating supervisory signals, and controlling the delay timer blocks.

The HVOUT1 through HVOUT4 output pins of the Power1208 can be configured as high voltage FET drivers (for controlling power MOSFETs) or as open-drain outputs for general-purpose logic level interfacing. The 4 outputs (OUT5 to OUT8) provide an open-drain configuration.
Sequencing functions often require multiple long-duration timers. The programmable timers onboard the Power Manager can be individually configured to generate timing delays of up to 500 ms using the internal 250 kHz clock oscillator. Timing delays can be extended to any desired duration through the use of an external clock.

Features	Power1208	Power604
Programmable Sense Inputs	12 (1V-5.7V)	6 (1V-5.7V)
Supervisory Outputs	4	4
FET Drivers/Digital Outputs	4	-
Reprogrammable Timers	4	2
CPLD Macrocells	16	8
Power Supply Voltage	2.25V – 5.5V	2.25V – 5.5V
Packaging	44-pin TQFP	44-pin TQFP

Applications

To understand the role of the Power Manager in a circuit board, examine a typical card power supply cycle. The supply cycle can be divided into 5 phases. Figure 3 outlines the power supply cycle and the functions carried out during each phase.

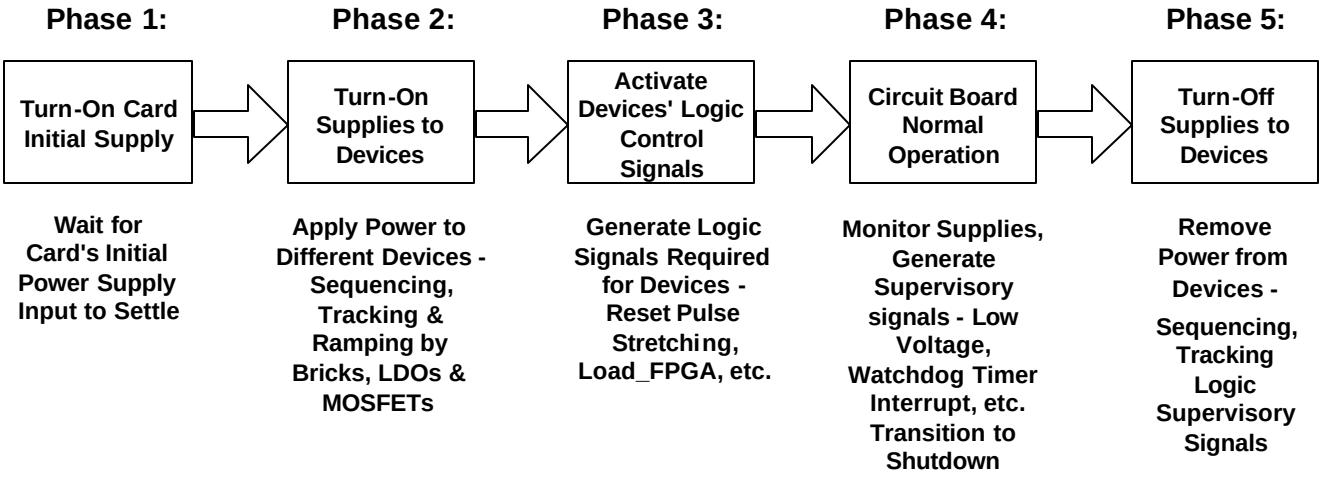

Figure 3: Typical Power Cycle of a Circuit Board

Phase 1: During this phase, the power supplies to the card are enabled. Different power supply voltages on the circuit board are derived from these initial supply voltages. The on-board power supply conversion and distribution mechanisms, however, must wait for the initial supplies to stabilize.

Phase 2: Additional supply voltages, determined by the requirements of multi-voltage devices on the circuit board, are derived from the initial voltages through DC-DC converters ('Bricks'), LDOs, or use MOSFETs to gate the supply voltage to different devices. These power supply conversion and distribution mechanisms must be precisely controlled to meet the sequencing, tracking and ramp

requirements of individual devices. For example, this phase also often requires one or more Power-FET devices to turn on with precisely controlled high-voltage signal characteristics.

Phase 3: Once the board's power system has stabilized and all devices on the board are powered up, the board is ready to operate. Some devices, however, may need some additional logic signals as a part of their initialization procedure. For example, a CPU reset signal may need to be asserted for 50 ms for it to complete its internal reset function.

Phase 4: In this phase the board is performing its normal operating functions and the role of the Power1208 is now shifted to continuously monitoring the health of the power supply voltages. All devices are required to be provided with supply voltages within their data sheet limits. If any one of the supply voltage dips below the device' supply tolerance level, remedial action should be taken – e.g., generate brownout interrupt to CPU.

Phase 5: Removing power from a device in a sequenced manner is as important as applying power. The requirements of the multi-voltage devices determine the exact shut down sequence.

Complete Power-Supply Management in All 5 Phases Using Power1208

The following block diagram is an example of a power supply distribution system in a circuit board with multi-voltage devices. The *Power1208* implements all power sequencing and monitoring functions.

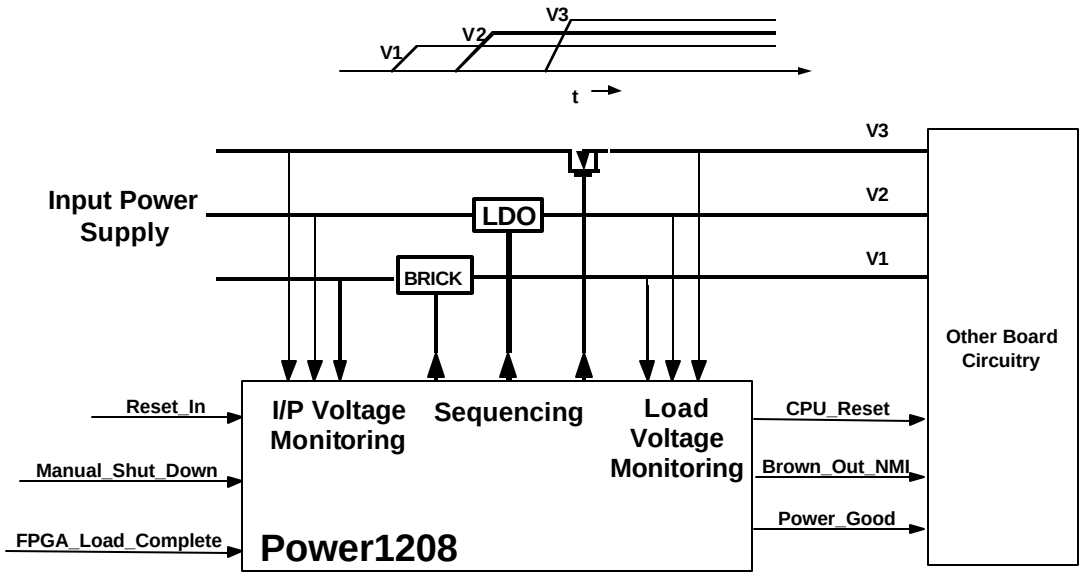

Figure 4 – Circuit Board Power Management with Power1208

Example: Power Supply Monitoring

Each one of the Power1208's analog inputs is connected to a dedicated threshold comparator. These comparators offer precise, independently programmable thresholds that allow them to monitor the supply voltages for over voltage or under voltage conditions.

Phase 1: Input Voltage monitoring ensures that all external power supplies are stable before the on-board power supplies (Brick, LDO, and FET) are turned on.

Phase 2: The voltages on the device side (V1,V2,V3) are monitored to ensure reliable power application to the devices and facilitate jumping to the next phase.

Phase 3. All power supply nodes (input and device side) and digital input signals (Reset_In & FPGA_Load_Complete) are monitored to generate logic control signals (CPU_Reset and Power_Good) for the system to start up.

Phase 4. All power supply nodes (input and device side) are monitored for power supply faults and to facilitate generation of supervisory signals: Brown_Out_NMI, CPU_Reset, and Power_Good. Also, the Manual_Shut_Down signal is monitored to facilitate the control logic to jump to phase 5.

Phase 5. Monitor supplies to ensure controlled shut down.

Example: Power Supply Sequencing and Tracking

Power supplies for the devices can be turned on in a predetermined sequence by controlling the output enable signals of bricks or LDOs or by controlling the gates of MOSFET switches. Here, the Power1208 turns the Brick on first and waits for V1 to settle. The LDO is turned on next. Once V2 is within limits the FET is enabled for V3 to ramp up. During turn-off, the MOSFET is turned off first, followed by the LDO and Brick ensuring the power supply is turned off in the sequence V3, V2 and finally V1.

Example: Generation of Starting Logic Signals Just After Power-up

Often, the circuit board requires some logic signals indicating readiness of the power supply. Once V1, V2 and V3 are stable, the Power_Good signal is activated. The CPU_Reset Signal is deactivated after the FPGA_Load_Complete signal turns active. Once received, the CPU has all the logic on board ready for normal operation.

Example: Supervisory Signal Generation & Additional Glue Logic

In order to increase the reliability of the system as a whole, on-board power supply voltages need to be constantly monitored for faults. If a fault occurs, this is signaled to the CPU by the Brown_Out_NMI signal for saving mission critical information. If the supply fault is serious, the CPU_Reset is activated and automatically proceeds to shut down. The CPU_Reset Signal also mirrors the Reset_In signal. The Manual_Shut_Down signal forces the control logic to shut down.

Integration and Programmability Benefits with ispPAC Power Manager

- Greatly simplifies implementation of complex power-supply sequencing and monitoring systems.
- Reduces design time.
- Programmability reduces prototype-debugging time.
- By programming the threshold voltages, power supply margining tests can be performed on the production line.
- Power Manager provides the ***complete*** collection of functions needed for sequencing and monitoring power supplies in all 5 phases of power supply cycle; it is a ***complete*** single-chip solution.
- The robustness of the Power Manager device ensures reliable start up of the board, even under noisy power supply start up conditions.
- The change in supply sequencing and monitoring requirements due to component substitutions on the circuit board can be easily addressed through re-programmability.

Power1208 and Power604 are Supported by PAC-Designer® Version 2.1 Software

Power supply sequencing and monitoring designs can be implemented on Power Manager devices using Lattice's popular PAC-Designer version 2.1 software. The PAC-Designer software is an intuitive PC-based schematic design entry and simulation tool. The user can design complex sequencing and monitoring functionality easily using PAC-Designer's newest feature, LogiBuilder™, which uses a series of easy-to-use pull-down menus to define sequences and conditions to monitor. Supervisory output signals can be specified using the Supervisory Logic window. Designs can be completely verified using the tool's built-in digital waveform simulator.

Key design tool features include:

Monitoring threshold values for each analog input can be individually set by selecting appropriate the threshold value from a pull down menu.

Power Supply Ramp Rate Control is achieved setting the MOSFET gate drive characteristics for the HVOUT outputs. This is set by a pull down menu as well.

Power Supply Sequencing, Tracking and Supervisory Signal Generation Logic can be defined easily using just five point-and-click instructions in the LogiBuilder section and the Supervisory Logic section.

Verification using PAC-Designer's waveform simulator can verify the completed design.

ispDownload to the Power Manager Device - The complete and verified design can be downloaded to the **Power1208 / Power604** device through the device's JTAG port.

The PAC-Designer 2.1 software is available at no charge and can be downloaded from www.latticesemi.com.

Development Kits

The PACsystemPOWR1208, like Lattice's other ispPAC development kits, comprises an evaluation board, an ispDOWNLOAD cable, and PAC-Designer v2.1 software.