ispXPLD™ 5000MX Family

White Paper

October 2002

Overview

The two largest segments of the high density programmable logic market have traditionally been non-volatile, Complex Programmable Logic Devices (CPLDs) and SRAM-based Field Programmable Gate Arrays (FPGAs). CPLDs have historically provided the benefits of

- Fast, predictable timing
- Single-level wide logic support
- Non-volatile, in-system programmability (ISP™)
- "Instant on" operation

while SRAM-based FPGAs have provided

- Very high logic density
- On-chip Memory Support
- Unlimited in-system reconfigurability
- Low standby power

Lattice Semiconductor has developed a logical successor to earlier Simple PLD and Complex PLD architectures, called the ispXPLD™ (eXpanded Programmable Logic Device), that combines the best attributes of CPLDs and FPGAs in a single architecture. These new devices are based upon a convergence of programming technology and architecture that is truly unique.

The new programming technology, called ispXP™ (for in-system programmable eXpanded Programmability), provides non-volatile in-system programmability combined with reconfigurability via a microprocessor sysCONFIG port. The new architecture, based on a set of homogeneous Multi-Function-Blocks that can implement a variety of functions based on the user's application requirements, supports both logic and memory on-chip with up to 300K system gates in a single device. In addition, extremely wide functions of up to 136 inputs can be implemented in a single level of logic for wide parallel logic processing.

Applications

The mix of system-level functionality, memory and logic allows the ispXPLD devices to address mainstream system functions previously relegated only to FPGAs or ASICs. The ability to integrate multiple independent blocks of buffer memory using a variety of memory architectures (FIFO, dual-port, CAM, etc.) together with fast programmable logic onto a single device offers great application flexibility. The addition of programmable sysIO interface standard support and sysCLOCK high-performance clocking amplifies the value of the devices as efficient control and data conductors within leading-edge systems. Potential application areas include high-performance bus bridges, intelligent backplane interfaces, protocol processors and the like.

The architecture builds upon traditional CPLD strengths and addresses high-density, high-performance (up to 285 MHz) applications for industries requiring fast time to market. These industries include telecommunications, data communications and data processing.

Typical applications in telecommunications include switches, exchange equipment, and cellular base stations; in data communications, high-end routers, bridges, switches, repeaters and intelligent hubs; and, in data processing, disk-array systems, data storage, RAID controllers, high-end graphics, high-end servers, scanners and imaging systems.

The ispXPLD 5000MX Family

These devices extend the capability of Lattice's popular SuperWIDE CPLD architecture by providing flexible memory capability and the ability to trade-off memory and logic resources within the device. The family supports single-port SRAM, true dual-port SRAM, FIFO, and ternary CAM operation. In addition, sysCLOCK PLLs and sysIO interfaces provide support to maximize system-level performance.

The devices provide designers with a convenient one-chip solution that provides logic availability at boot-up, design security, and extreme reconfigurability. The use of advanced process technology provides industry-leading performance with combinatorial propagation delay as low as 4.0ns, 2.8ns clock-to-out delay, 2.5ns set-up time, and operating frequency up to 285MHz. This performance is coupled with low static and dynamic power consumption. The ispXPLD 5000MX architecture provides predictable deterministic timing.

The availability of 3.3, 2.5 and 1.8V versions of these devices (designated the 5000MV, 5000MB and 5000MC series, respectively), along with the flexibility of the sysIO interface, helps users meet the challenge of today's mixed voltage designs. Boundary scan testability further eases integration into today's complex systems. A variety of density and package options increase the likelihood of a good fit for a particular application. Table 1 shows the members of the ispXPLD 5000MX family.

The ispXPLD 5000MX family has been designed to ensure that different density devices in the same package have compatible pin-outs. Furthermore, the architecture ensures a high success rate when performing design migration from lower density parts to higher density parts.

Table 1. ispXPLD Family

	ispXPLD 5256MX	ispXPLD 5512MX	ispXPLD 5768MX	ispXPLD 51024MX
Macrocells	256	512	768	1,024
Multi-Function Blocks	8	16	24	32
Maximum RAM Bits	128K	256K	384K	512K
Maximum CAM Bits	48K	96K	144K	192K
sysCLOCK PLLs	2	2	2	2
t_{PD} (Propagation Delay)	4.0ns	4.5ns	5.0ns	5.0ns
t_S (Register Set-up)	2.5ns	2.9ns	3.6ns	3.6ns
t_{CO} (Register Clock to Out)	2.8ns	3.0ns	3.8ns	3.8ns
f_{MAX} (Maximum Operating Frequency)	285MHz	250MHz	225MHz	225MHz
I/Os	141	149/193/253	193/317	317/381
System Gates	75K	150K	225K	300K
Packages	256 fpBGA	208 PQFP 256 fpBGA 484 fpBGA	256 fpBGA 484 fpBGA	484 fpBGA 672 fpBGA

Architecture

The ispXPLD 5000MX devices consist of Multi-Function Blocks (MFBs) interconnected with a Global Routing Pool. Signals enter and leave the device via one of four sysIO banks. Figure 1 shows the block diagram of the ispXPLD 5000MX. Incoming signals may connect to the global routing pool or the registers in the MFBs. All signals are fed from the device via the MFB. An Output Sharing Array (OSA) increases the number of I/O available to each MFB, allowing a complete function high-performance access to the I/O. There are four clock pins that drive four global clock nets within the device. Two sysCLOCK PLLs are provided to allow the synthesis of new clocks and control over clock skews.

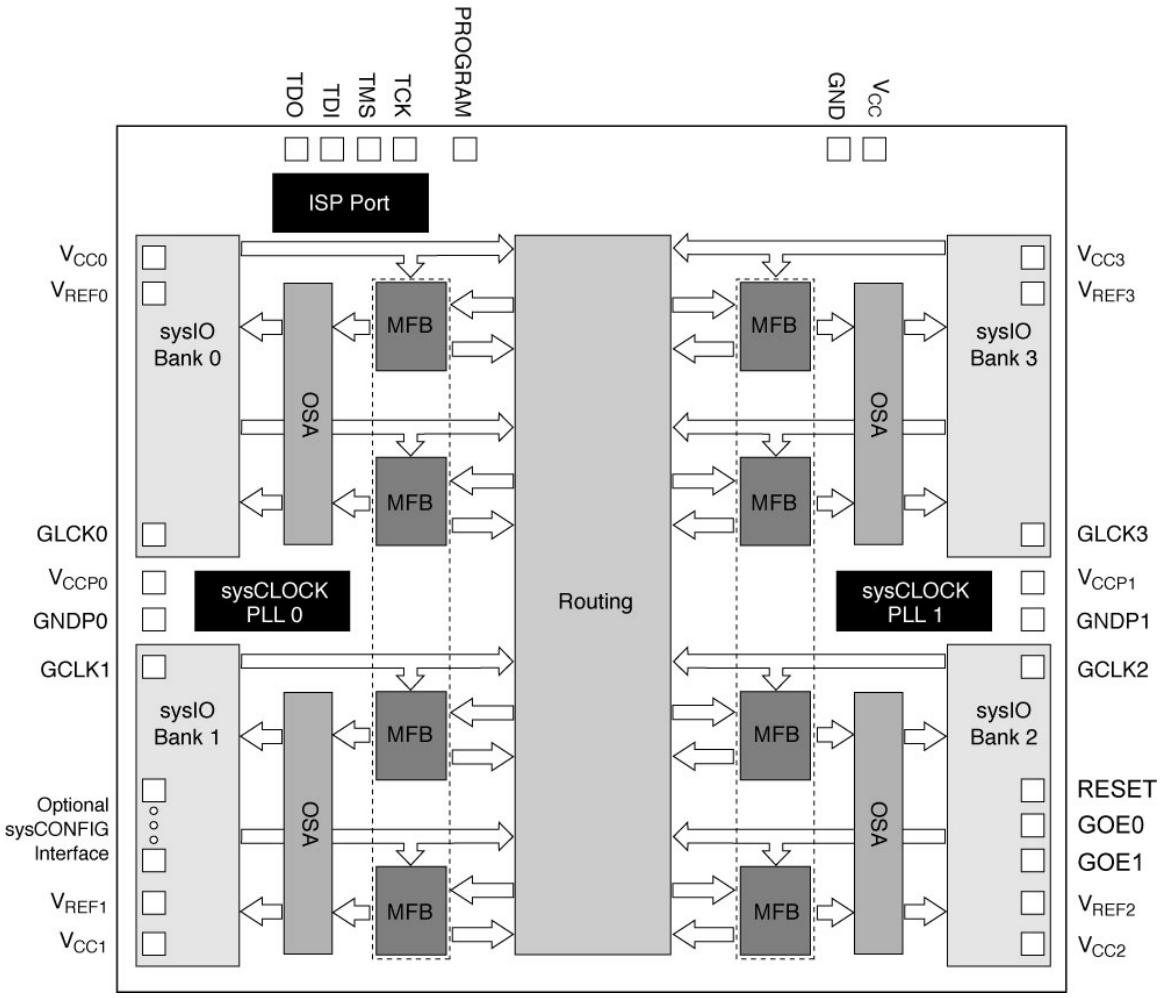
Multi-Function Block (MFB)

Each MFB in the ispXPLD 5000MX architecture can be configured in one of the six following modes. This provides a flexible approach to implementing logic and memory that allows the designer to achieve the

mix of functions that are required for a particular design, maximizing resource utilization. The six modes supported by the MFB are:

- SuperWIDE Logic Mode
- True Dual-port SRAM Mode
- Pseudo Dual-port SRAM Mode
- Single-port SRAM Mode
- FIFO Mode
- Ternary CAM Mode

Figure 1. ispXPLD Block Diagram



The MFB consists of a multi-function array and associated routing. Depending on the chosen functions, a single multifunction array uses up to 68 inputs from the GRP and the four global clock and reset signals. The array outputs data along with certain control functions to the macrocells. Output signals can be routed internally for use elsewhere in the device and to the sysIO banks for output. The various configurations are described in more detail in the following sections.

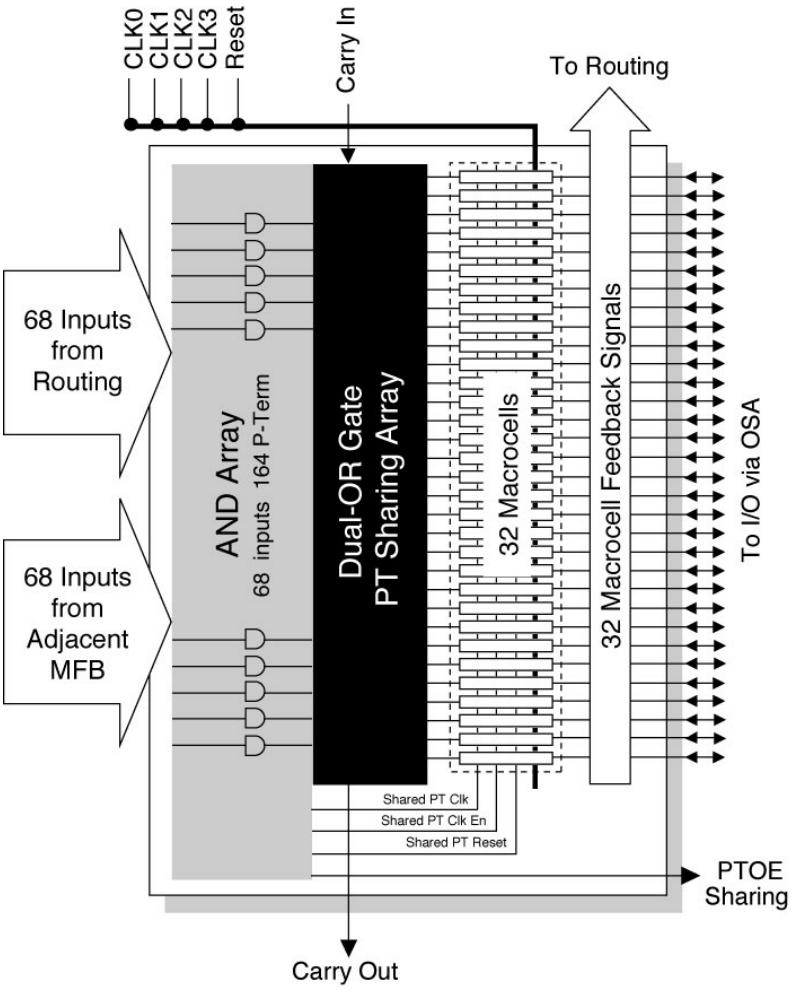
SuperWIDE Logic Mode

In logic mode, each MFB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and four control product terms. The MFB has 68 inputs from the Global Routing Pool. It is also possible to cascade adjacent MFBs to create a block with 136 inputs.

Five product terms form a product term cluster associated with each macrocell. The PTSA (Product Term Sharing Array) allows wider functions to be implemented easily and efficiently by cascading product term clusters across macrocells within the MFB. In this way, functions of up to 160 product terms can be constructed without leaving the MFB.

Four additional dedicated control product terms per MFB are used for shared reset, clock, clock enable, and output enable functions. In addition to the four MFB-level control product terms, designated product terms in each cluster can be used to generate macrocell-specific OE, Clock, Preset and Reset functions. Figure 2 shows the overall structure of the MFB in logic mode.

Figure 2. Multi-Function Block / Logic Mode



The 32 registered macrocells in the MFB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells also contain logic to aid in the efficient implementation of arithmetic functions through dedicated carry chain logic. Macrocell registers can be clocked from one of several global or product term clocks available on the device.

Memory Modes

The ispXPLD 5000MX architecture allows the MFB to be configured as a variety of memory blocks: Single-Port RAM, Pseudo Dual-Port RAM, True Dual-Port RAM, FIFO, and CAM. In each of the memory

modes it is possible to specify the power-on state of each bit in the memory array. This allows the memory to be used as ROM if desired.

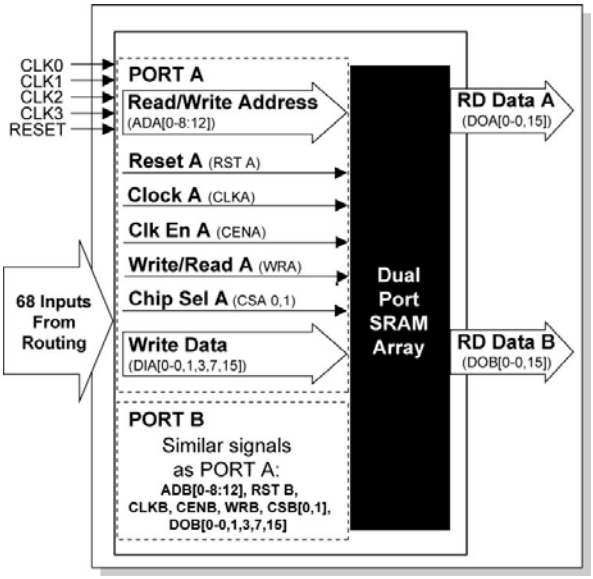
Designs that require a memory depth or width that is greater than that supported by a single MFB can be supported by cascading multiple blocks. For dual port, single port, and pseudo dual port modes additional width is easily provided by sharing address lines. Additional depth is supported by multiplexing the RAM output. For FIFO and CAM modes, additional width is supported through the cascading of MFBs.

The Lattice ispLEVER design tools automatically combine blocks to support the memory size specified in the user's design.

True Dual-Port SRAM Mode
In Dual-Port SRAM Mode the multi-function array is configured as a dual port SRAM. In this mode two independent read/write ports access the same 8,192-bits of memory. Data widths of 1, 2, 4, 8, and 16 are supported by the MFB for all RAM and FIFO configurations. Figure 3 shows the block diagram of the dual port SRAM.

Write data, address, chip select and read/write signals are always synchronous (registered.) The output data signals can be synchronous or asynchronous.

Figure 3. Dual-Port RAM Mode



In Pseudo Dual-Port SRAM Mode, the multi-function array is configured as a RAM with independent read and write ports that access the same 16,384-bits of memory.

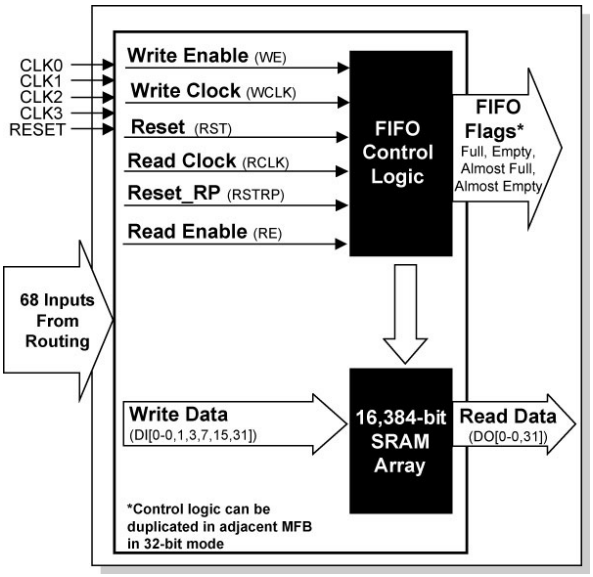
Single-Port SRAM Mode
In Single-Port SRAM Mode the multi-function array is configured as a single-port SRAM. In this mode one ports accesses 16,384-bits of memory.

FIFO Mode
In FIFO Mode the multi-function array is configured as a FIFO (First In First Out) buffer with built in control. The read and write clocks can be different or the same dependent on the application. Four flags show the status of the FIFO; Full, Empty, Almost Full, and Almost empty. The thresholds for Almost full and Almost empty are programmable by the user. It is possible to reset the read pointer, allowing support

of frame retransmit in communications applications. If desired, the block can be used in show ahead mode allowing the early reading of the next read address.

In this mode, one port accesses 16,384-bits of memory. Figure 4 shows the block diagram of the FIFO.

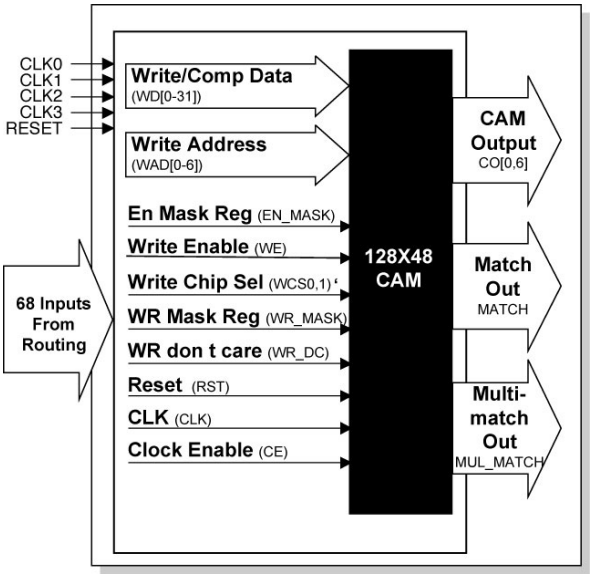
Figure 4. FIFO Mode



CAM Mode

In CAM Mode the multi-function array is configured as a Ternary Content Addressable Memory (CAM.) CAM behaves like a reverse memory where the input is data and the output is an address. It can be used to perform a variety of high-performance look-up functions. As such CAM has two modes of operation. In write or update mode the CAM behaves as a RAM and data is written to the supplied address. In read or compare operations data is supplied to the CAM and if this matches any of the data in the array the Match, Multiple Match (if there is more than one match) flags at set to true and the lowest address with matching data is output. The CAM contains 128 entries of 48 bits.

Figure 5. CAM Mode



To further enhance the flexibility of the CAM a mask register is available. If enabled during updates, bits corresponding with those set to 1 in the mask register are not updated. If enabled during compare operations, bits corresponding to those set to 1 in the mask register are not included in the compare. A write don't care signal allows don't cares to be programmed into the CAM if desired. Like other write operations the mask register controls this.

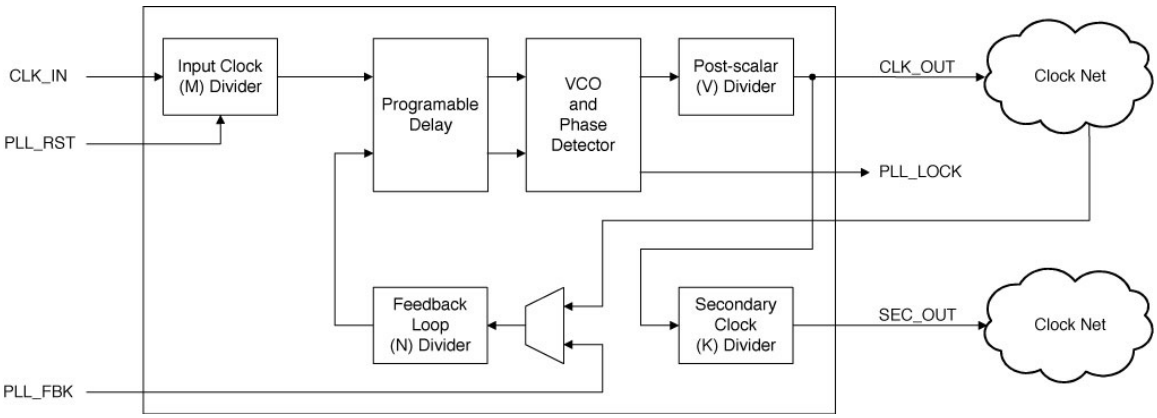
Clock Distribution

The ispXPLD 5000MX family has four dedicated clock input pins: GCLK0-GCLK3. GLCK0 and GCLK3 can be routed through a PLL circuit or routed directly to the internal clock nets. The internal clock nets (CLK0-CLK3) are directly related to the dedicated clock pins (see Secondary Clock Divider exception when using the sysCLOCK circuit). These feed the registers in the MFBs.

sysCLOCK PLL

The sysCLOCK PLL circuitry consists of Phase-Lock Loops (PLLs) and the various dividers, reset and feedback signals associated with the PLLs. This feature gives the user the ability to synthesize clock frequencies and generate multiple clock signals for routing within the device. Furthermore, it can generate clock signals that are de-skewed either at the board level or the device level.

Figure 6. sysCLOCK PLLs



The ispXPLD 5000MX devices provide two PLL circuits. The optional outputs CLK_OUT can be routed to an I/O pin. The optional PLL_LOCK output is routed into the GRP. The optional PLL_FBK into can be routed directly from a pin. Figure 6 shows the ispXPLD 5000MX PLL block diagram.

In order to facilitate the multiply and divide capabilities of the PLL, each PLL has dividers associated with it: M, N and K. The M divider is used to divide the clock signal, while the N divider is used to multiply the clock signal. The K divider is only used when a secondary clock output is needed. This divider divides the primary clock output and feeds to a separate global clock net. The V divider is used to provide lower frequency output clocks, while maintaining a stable, high frequency output from the PLL's VCO circuit. The PLL also has a delay feature that allows the output clock to be advanced or delayed to improve set-up and clock-to-out times for better performance.

sysIO Banks

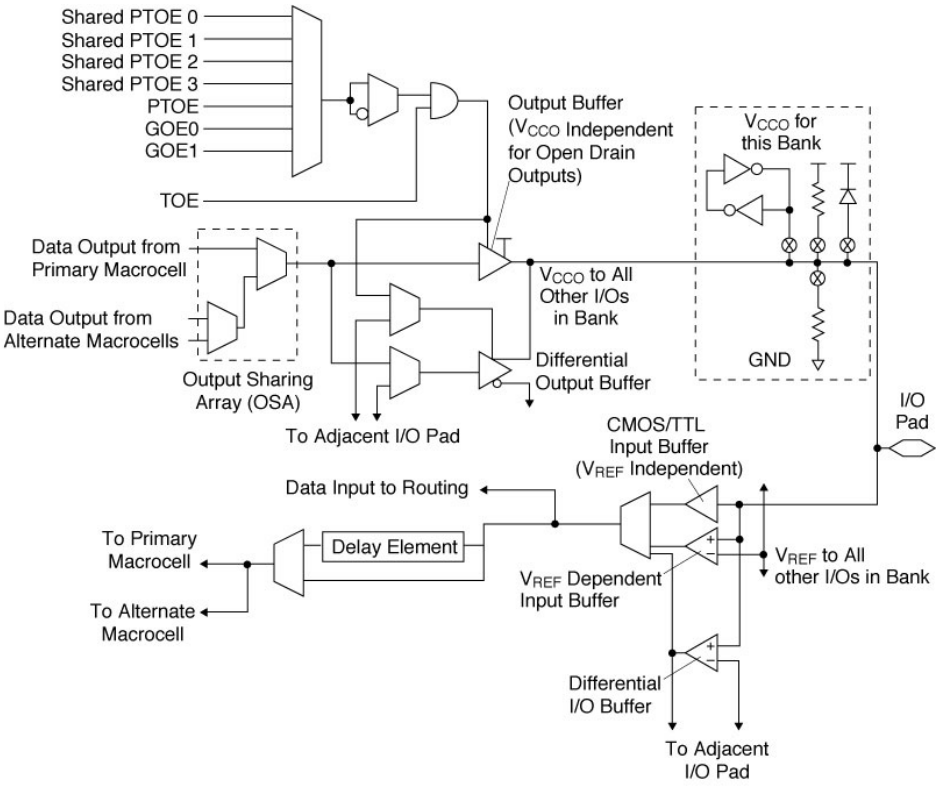
The ispXPLD 5000MX devices are divided into four sysIO banks, consisting of multiple I/O cells, where each bank is capable of supporting 16 different I/O standards. Each sysIO bank has its own I/O voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence from the others.

I/O Cell

The I/O cell of the ispXPLD 5000MX devices contains an output enable (OE) MUX, a programmable tri-state output buffer, a programmable input buffer, programmable bus-maintenance (pull-up, pull-down, bus-keeper, none) circuitry, programmable drive strength to support trace impedance matching and programmable slew rate to minimize ground bounce. The I/O cell receives inputs from its associated macrocells and the device pin. The output enable (OE) MUX selects the OE signal per I/O cell from the global PTOE signals, individual PTOE term or the two Global OE signals.

The I/O pins on the ispXPLD 5000MX devices are also well suited for those applications that require hot socketing capability, when configured as LVCMOS or LVTTL. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged and have minimal effect on active signals.

Figure 7. I/O Cell



sysIO Standards

Each I/O within a bank is individually configurable based on the V_{CCO} and V_{REF} settings. Some standards also require the use of an external termination voltage. Table 2 lists the sysIO standards with the typical values for V_{CCO}, V_{REF} and V_{TT}.

Table 2. sysIO Standards Supported by ispXPLD 5000MX

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3V	3.3V	N/A	N/A
PCI-X 3.3V	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75v
HSTL, Class IV	1.5V	0.9V	0.75v
GTL+	N/A	1.0V	1.5V
LVDS	2.5V, 3.3V	N/A	N/A

Low Power Consumption

The ispXPLD 5000MX devices use zero power non-volatile cells along with full CMOS design to provide low static power consumption. The 1.8V core reduces dynamic power consumption compared with devices with higher core voltages. For example, standby power consumption has been reduced to as low as 36 milliwatts for the ispXPLD 5256MC.

Expanded In-System Programmability (ispXP)

The ispXPLD 5000MX family utilizes a combination of EEPROM non-volatile cells and SRAM technology to deliver a logic solution that provides “instant-on” at power-up, a convenient single chip solution, and the capability for infinite reconfiguration. A non-volatile array distributed within the device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device.

In-system programming of devices provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make in-field modifications. All ispXPLD 5000MX devices provide in-system programmability through their Boundary Scan Test Access Port. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1532 standard. The IEEE1532 programming interface allows programming of either the non-volatile array or re-configuration of the SRAM bits.

In addition to being able to program the device through the IEEE 1532 interface, a microprocessor-compatible interface (sysCONFIG interface) allows reconfiguration of the device.

IEEE 1149.1-Compliant Boundary Scan Testability

All ispXPLD 5000MX devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic notes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for board-level testing. The test access port has its own supply voltage and can operate with LVCMOS3.3, 2.5 and 1.8V standards.

Design Environment – *ispLEVER*™

Lattice's new ispLEVER design tool supports ispXPLD device design. ispLEVER has been designed as Lattice's design platform for the future. Building on the foundations of past design tools, ispLEVER includes fitting and usability enhancements that speed design and improve achievable performance.

The ispLEVER design tools support Timing Driven Design, a new Constraints Manager for easy sysIO and sysCLOCK configuration and pin assignment, enhancements to Lattice's Performance Analyst™, static timing analyzer, as well as other ease-of-use refinements, such as HTML Reporting and Navigation and automatic web-based ispUPDATE™. Every ispLEVER product also includes Lattice's powerful In-System Programming tool, the ispVM™ System.

The new ispLEVER tools also provide a sophisticated IP Manager feature in support of Lattice's LeverCORE™ intellectual property program. As part of its total programmability solution, Lattice is developing and working with Third Parties to deliver high performance IP such as PCI, Utopia, POS-PHY and other functions for its ispXPLD, FPGA and FPSC (Field Programmable System Chip) products.

ispLEVER design tools also integrate leading 3rd party CAE vendor tools for synthesis and RTL and timing simulation from Mentor Graphics® / Exemplar and Synplicity®. Figure 8 shows a typical design flow with the ispLEVER design tool.

Figure 8 – Typical ispLEVER Design Flow