White Paper

Non-Volatility and Infinite Reconfigurability in PLDs

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The ispXPGA™ and ispXPLD™ Families

ispXPGA FPGAs and ispXPLD PLDs cover a range of densities and I/Os with rich functionality. They are SRAM-based families which allows them to be reconfigured an unlimited number of times. What sets these products apart is the inclusion of E^2 memory cells on the same monolithic integrated circuit, which enables non-volatile programming and reprogramming. This attribute is named ispXP™(Expanded Programming).

On-Chip Non-Volatility

Adding non-volatility to an SRAM-based PLD delivers three major benefits:

1) Availability of the PLD logic within microseconds of power-up for Instant-On

2) High security since there is no external bitstream during configuration, and since non-volatile security bits can disable readback of the PLD pattern

3) Simplified system design because there are no noise, reliability, or board space concerns related to configuration from an external Serial PROM (SPROM)

Also, the single-chip solution offers the traditional benefits of in-system programmable non-volatile devices through reduced inventory/handling/manufacturing costs, and easier field system upgrades.

Programming and Configuration Modes

No two applications or manufacturing flows are exactly alike, so multiple ways of programming and configuring programmable logic devices are needed. E^2 devices are typically programmed through an IEEE 1149.1 compliant TAP. SRAM devices are usually configured from a SPROM through a dedicated serial interface or from a microprocessor through a CPU port. Having both E^2 and SRAM memory on the same device allows for additional configuration modes that open up new applications possibilities. Figure 1 shows the modes used for programming and configuring the two memory spaces on ispXPGA and ispXPLD devices.

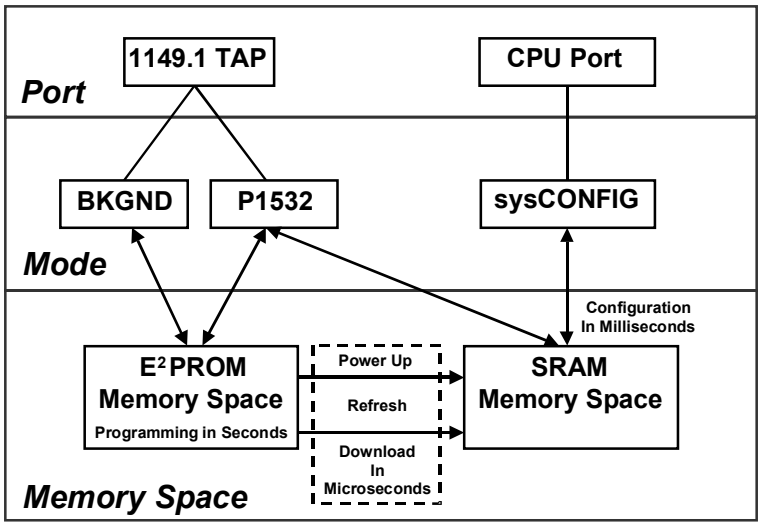


Figure 1 – ispXPGA and ispXPLD Configuration Modes

As is the case with traditional E^2-based programmable logic devices, the non-volatile on-chip E^2 cells are in-system programmable using the IEEE Test Access Port (TAP), although one can also use a device-programmer system. The programming algorithm and circuitry in the ispXPGA and ispXPLD families of devices is fully IEEE1532 compliant, allowing for easier support on third-party ATE and test systems, along with better concurrent programming support for systems with multiple vendors' devices. In addition to the IEEE 1532 compliant programming mode, the E^2 memory can also be reprogrammed in-system in a background mode, where the PLD continues to perform its system logic functions because the logic is directly controlled by the SRAM memory. 1000 E^2 programming cycles are guaranteed as specified on the datasheet.

The SRAM memory on a ispXPGA or ispXPLD device is what actually controls the logic and functionality that is implemented. There are three methods used for configuring the SRAM: downloading from the E^2 memory space, IEEE 1532 compliant configuration, and the *sysCONFIG*™ CPU configuration mode. When downloading from the on-chip E^2 memory, the SRAM is configured in microseconds. This happens automatically at power-up as well as on-command, whenever the user instructs. The device's outputs are tristated during reconfiguration.

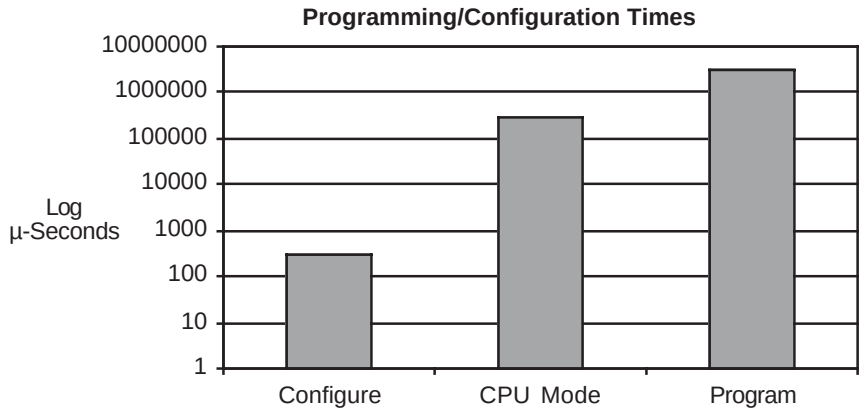
The sysCONFIG CPU-mode allows the SRAM to be configured directly through a 33-MHz 8-bit parallel port. The IEEE 1532 compliant configuration mode downloads configuration data to the SRAM directly through the 1149.1 TAP. In both of these modes the on-chip E^2 memory is bypassed. The sysCONFIG mode is available at power-up and on-command, with I/Os being tri-stated until configuration is completed. When reading back the configuration data using the sysCONFIG mode, the I/Os and logic continue to operate. When configuring the SRAM using the 1532 configuration mode the boundary-scan register controls the I/Os.

This flexible combination of programming/configuration modes lets the system designer achieve multiple desired outcomes:

1) Program in manufacturing, auto-configure at power-up in microseconds
2) Same as 1, but also reconfigure periodically during operation
3) Download a field upgrade and reprogram on-chip E^2 while system is operating, then reconfigure SRAM in microseconds
4) Program default pattern in manufacturing; choose to override with sysCONFIG direct SRAM configuration depending on system conditions
5) Program system power-up and check-out configuration in manufacturing; then reconfigure to system-operation pattern in-system using sysCONFIG mode.

Here is a review of the Modes of Operation:

Operation	At Power-Up In-System	On Command In-System	Off-Line
Auto-configure SRAM from on-chip E^2 cells	Microseconds		
Reconfigure SRAM from on-chip E^2 cells		Microseconds	
Program on-chip E^2 while FPGA is running		Seconds	
Program on-chip E^2			Seconds
Configure SRAM directly in sysCONFIG mode	Milliseconds	Milliseconds	



Reliable Programming/Configuration

After the on-chip E^2 memory is programmed, a standard verify cycle may be performed to ensure that the device has been properly patterned.

Robust 5-transistor-cell SRAM optimized for clean, reliable operation is used. Configuration of the SRAM from the E^2 memory benefits from the reduced noise that single-chip integration affords. This process also has a built-in handshake protocol and a DONE signal that reports successful device configuration. Further, the configuration function uses hysteresis to restart itself if it detects that the power-supply has gone out of spec during configuration. Lastly, the SRAM can be read back transparently while the ispXPGA or ispXPLD is performing its system logic functions, thereby providing an additional pattern check, if desired.

When using the sysCONFIG mode, readback and transparent readback are available for verification of the pattern, complemented by the chip's generation of a CRC code. Here, too, hysteresis guards against power-supply issues.

Security

Until now, configuring an SRAM-based PLD meant risking that one's design would be reverse-engineered by third parties examining the pattern bitstream coming in from off-chip. ispXPGA and ispXPLD devices eliminate this risk, since their SRAM cells can be configured from on-chip E^2 memory that was programmed in one's own safe manufacturing environment. There is no external bitstream available to be pirated during system operation in the field. To complete this theft-resistant solution, there are two security bits which can be set to disable pattern readback from E^2 memory and/or SRAM.

Summary

A non-volatile, infinitely reconfigurable PLD reliably provides designers with desirable but heretofore unavailable benefits, including logic availability within microseconds of power-up or reprogramming, and high security. Significant savings accrue in board space, system design effort, inventory costs, handling costs, and manufacturing costs. Field system upgrades, including those performed during system operation, are simplified.

This new capability is a powerful tool for the system design engineer.

More information is available in the Lattice ispXPGA/ispXPLD Configuration Guide.