ispMACH™ 5000VG CPLD Architecture

White Paper

October 2001

Overview

Lattice Semiconductor's next generation In-system Programmable (ISP™) Complex Programmable Logic Device (CPLD) architecture, the ispMACH 5000VG family, addresses user needs for higher integration, speed performance, and shorter time-to-market. This third generation 5000 family doubles the capacity of Lattice SuperWIDE products taking them to SuperBIG sizes. In addition, sysCLOCK™ and sysIO™ capabilities have been added to maximize system-level performance and integration.

Market Needs

Key needs of logic designers are higher integration, reduced time-to-market and increased speed performance. System integration is driven by today's need to reduce board size for a given level of functionality. This improved integration can be achieved by using devices that provide more logic capacity and integrate peripheral functions. Today's competitive environment means there are tremendous advantages associated with delivering new products to the market more quickly than the competition. In order to facilitate this, designers are looking for logic products that allow them to quickly implement their designs. Logic solutions that allow designers to complete their designs quickly are easy to design with, facilitate rapid implementation of design changes, and can be integrated simply into the rest of the system. Improved speed performance is needed to achieve goals such as increased communication bandwidth and computing power. In order to meet this need logic products have to combine raw silicon speed with architectures that allow designers to efficiently implement their designs.

Architecture Overview

Signals enter the ispMACH 5000VG via I/O banks consisting of sysIO capable I/O cells that support a wide variety of advanced interface standards. Clock signals can be fed through one of two sysCLOCK PLLs that provide enhanced clocking capability within the device. The I/O cells feed SuperWIDE logic blocks, which are interconnected via an innovative two-tiered routing system. Like all recent Lattice CPLDs the ispMACH 5000VG family supports in-system programming and boundary scan testing. Figure 1 shows the overall block diagram of the ispMACH 5000VG.

Figure 1 – ispMACH 5000VG Block Diagram

sysIO Capable Interfacing

Over the past several years, many factors have played heavily into the development of new I/O switching standards. Perhaps the greatest factor has been the need to move signals around a board faster and with less noise. Different system level requirements, such as memory interfaces, backplane drivers and general interconnect, have different needs, hence the proliferation of standards that has occurred. In such an environment a programmable solution can provide unique value by providing in a single standard device the capability to interface between many of the components in a system. To support many of these applications, the ispMACH 5000VG provides a flexible I/O cell that supports multiple standards. Lattice refers to this feature as sysIO capability.

The I/O on the ispMACH 5000VG devices are divided into four sysIO banks, as shown in Figure 2, where each bank is capable of supporting the fourteen different I/O standards listed in Table 1. Clock inputs also provide support for the LVPECL and LVDS standards that are commonly used for system level clock distribution. Each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}) resources allowing complete independence between the banks. Each input and output within a bank can be individually configured to any standard compatible with the V_{CCO} and V_{REF} levels provided to the bank.

LVCMOS I/O also provide bus-maintenance, programmable drive strength, and programmable slew rate options. The bus-maintenance features allow inputs to have weak pull-ups, pull-downs, bus-latches, or none of these features. Outputs have programmable drive strength that can be used to control the impedance of the driver and eliminate the need for external series termination resistors. The slew rate options allow designers to slow down the edge rate of non-timing critical signals, reducing overall noise.

The ispMACH 5000VG also provides flexible output enable (OE) control. Each OE may be controlled from one of two global signals, four segment level signals, or one macrocell level signal. This flexibility, which allows designers to support multiple busses or grouping of signals within the device, has been provided on previous Lattice CPLD devices but becomes increasingly important at these higher logic capacities.

Figure 2 – ispMACH 5000VG sysIO Banking Scheme

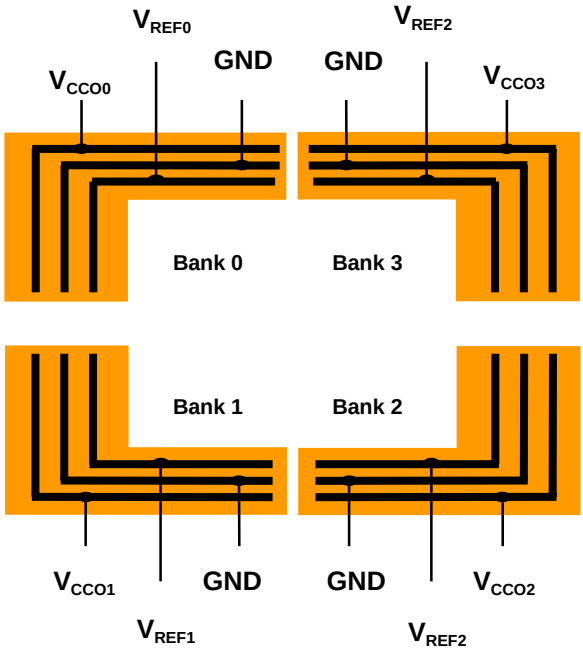


Table 1 – ispMACH 5000VG Supported sysIO Standards

sysIO Standard	V_{CCO} (Nominal)	V_{REF} (Nominal)	V_{TT}
LVTTL	3.3V	N/A	N/A
LVCMOS-3.3	3.3V	N/A	N/A
LVCMOS-2.5	2.5V	N/A	N/A
LVCMOS-1.8	1.8V	N/A	N/A
PCI 3.3	3.3V	N/A	N/A
PCI-X	3.3V	N/A	N/A
AGP-1X	3.3V	N/A	N/A
SSTL3, Class I & II	3.3V	1.5V	1.5V
SSTL2, Class I & II	2.5V	1.25V	1.25V
CTT 3.3	3.3V	1.5V	1.5V
CTT 2.5	2.5V	1.25V	1.25V
HSTL, Class I	1.5V	0.75V	0.75V
HSTL, Class III	1.5V	0.9V	0.75v
GTL+	1.5V to 3.3V	1.0V	1.5V
LVPECL, Differential[1]	N/A	N/A	N/A
LVDS[1]	N/A	N/A	N/A

1. LVDS and LVPECL are only supported on the dedicated clock pins

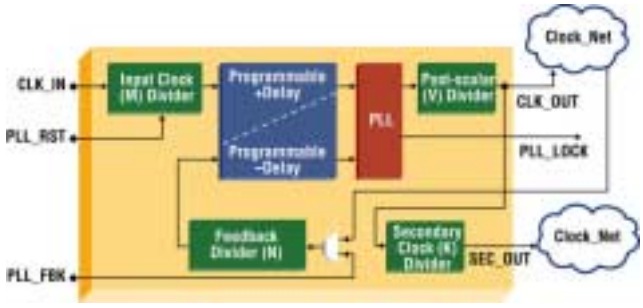
sysCLOCK Phased Locked Loops (PLLs)

As programmable logic devices grow in logic capacity, on-chip clock distribution becomes a major factor in performance. The delay and skew of the clocks can significantly affect the performance of the device. Furthermore, larger designs often require the generation of new clocks for use both internally and elsewhere in the system. The ispMACH 5000VG provides two sysCLOCK PLLs to improve performance and allow the synthesis of new clocks.

Each of the two PLLs within the ispMACH 5000VG operate between 5 and 180MHz. Figure 3 illustrates the PLL. A programmable divider (M) in the input path allows clock division while a divider in the feedback loop (N) allows clock multiplication. Two additional dividers, the post scalar (V) divider and secondary clock (K) divider, allow the internal voltage controlled oscillator to operate in its optimal range and for further division of the clock output, respectively. This multiply and divide capability allows users to synthesize new clocks as required by their designs. The ispMACH 5000VG PLLs also provide delay elements on the input and feedback lines, which can advance or delay the clock to allow for the optimization of set-up and clock-to-out times. This delay can be ±3.5ns in steps of 0.5ns.

The ispMACH 5000VG devices also provide the capability to drive the clock off-chip and the PLL has the option to receive its feedback from an external source. This allows the ispMACH 5000VG to distribute clocks to other devices and compensate for board level skew.

Figure 3 – ispMACH 5000VG sysCLOCK Phased Locked Loop (PLL)

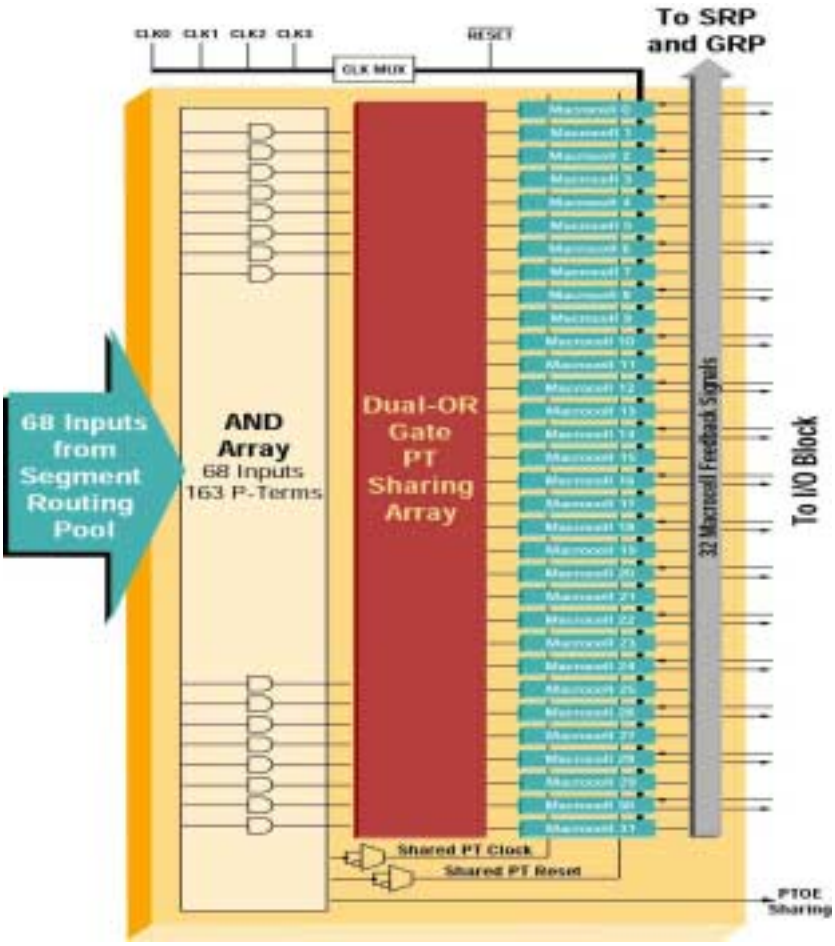


These sysCLOCK PLL features give designers the flexibility of creating a variety of clock signals for use both internal and external to the device. This improves integration, simplifies board design and reduces cost, designers no longer need external circuitry to create these clocks. The ability to remove clock tree delay coupled with the ability to advance or delay clocks allows designers to increase the performance of their designs, again without the disadvantage of additional external components.

SuperWIDE Generic Logic Block (GLB)

The SuperWIDE GLB architecture allows designers to easily implement high-complexity logic functions with high-speed performance while achieving high-utilization of device resources. Many elements of the GLB support this capability including, logic block width, an enhanced dual OR-gate sharing array and flexible macrocells. Figure 4 provides a graphical representation of the GLB.

Figure 4 – SuperWIDE Generic Logic Block (GLB)



68-Input AND Array

Each GLB contains an AND array consisting of 163 product terms fed by a common set of 68-inputs. Traditionally CPLDs have only 36 or less inputs to their AND arrays. Today, many logic designers want to implement functions that require greater than 36 inputs. In a traditional CPLD this requires that two logic blocks be used sequentially and the function incurs the delay associated with these two blocks. The same function can be implemented in one logic block with

one associated delay with a 68-input logic block. For Lattice parts we refer to logic blocks with this capability as SuperWIDE GLBs. For complex functions we have found that the SuperWIDE GLBs can provide up to a 60% performance improvement over more traditional CPLD architectures.

Enhanced Dual-OR Product Term Sharing Array

In any CPLD, product terms have to be allocated and where necessary, combined for use in the macrocells. In the ispMACH 5000VG architecture this function is implemented with the product term sharing array. Two features of this approach increase the utilization that designers can achieve with the device. First, macrocells with I/Os can implement two functions if desired, one registered and one combinatorial. This allows more functions to be placed within a given GLB. Second, common product terms can be shared across multiple macrocells, avoiding the unnecessary duplication of product terms within the logic block.

In analyzing typical user designs, Lattice noted that a significant portion required a large number of product terms to be combined to form a single logic function. In previous Lattice CPLD architectures the maximum number of product terms that could be implemented in a single pass through a logic block was 35. The ispMACH 5000VG removes this restriction allowing up to 160 product terms to be combined in a single function. For certain functions Lattice has found that this enhancement to the product term sharing array can lead to performance improvements of up to 25%.

Flexible Macrocell

The outputs of the product term sharing array are fed to macrocells to be registered if desired by the user. Dependent on the user's design style and the synthesis tool, a variety of register functions may be required. To allow optimum implementation of these functions and flexibility for the place and route design tools it is important to provide sufficient capability and flexibility in the macrocell. The ispMACH 5000VG macrocell provides many clock, clock enable, and initialization options to ensure this flexibility. The end result is an architecture that provides efficient results with a number of design styles and synthesis tools.

SuperBIG Two-Tiered Routing Scheme

As the logic capacity of traditional CPLDs increases, the routing interconnect that connects the macrocells together grows dramatically. This growth in interconnect resources, using a single level of interconnect would, if allowed to continue, result in a very large silicon area with relatively little logic capability. A solution to this problem is to take a hierarchical, multi-tiered, scalable, approach to extending CPLD solutions to higher densities. Lattice Semiconductor has used this technique in its ispMACH 5000VG architecture to double the macrocell count of its SuperWIDE architecture while retaining the performance and predictable timing attributes associated with CPLDs.

A routing pool referred to as the Segment Routing Pool (SRP) interconnects groups of four 32-macrocell GLBs to form a 128-macrocell segment. The pin-to-pin performance within a segment is 5ns. These segments are then further connected together by a Global Routing Pool (GRP) creating a two-tiered routing system. There is a 1.5ns delay associated with using the GRP, thus the worst case pin-to-pin delay across the chip is a predictable 6.5ns.

Initially, Lattice will use the routing scheme described above to create ispMACH 5000VG devices up to 1024 macrocells. However, the scheme is easily expandable to higher densities. The initial devices will provide up to 384 I/O and will be provided in space saving 1mm fine pitch Ball Grid Array (fpBGA) packages.

Monolithic Non-volatile ISP Solution

For many applications, designers want an in-system programmable solution. Such a solution typically allows faster development, lower inventory levels, higher quality, and the ability to make

in-field modifications. In addition, for many designs, it is important for logic to be available at system power-up. This allows the logic to be functioning as various parts of the system are brought out of the reset state.

The ispMACH 5000VG provides a monolithic non-volatile ISP solution that allows logic to be available at power-up. In contrast, PLDs based around SRAM technologies do not allow logic to be available at power-up. This is also a drawback of solutions based on multi-chip modules containing separate non-volatile memory and logic elements. Certain one-time-programmable devices have their logic available at power up but are not able to offer the full benefits of ISP.

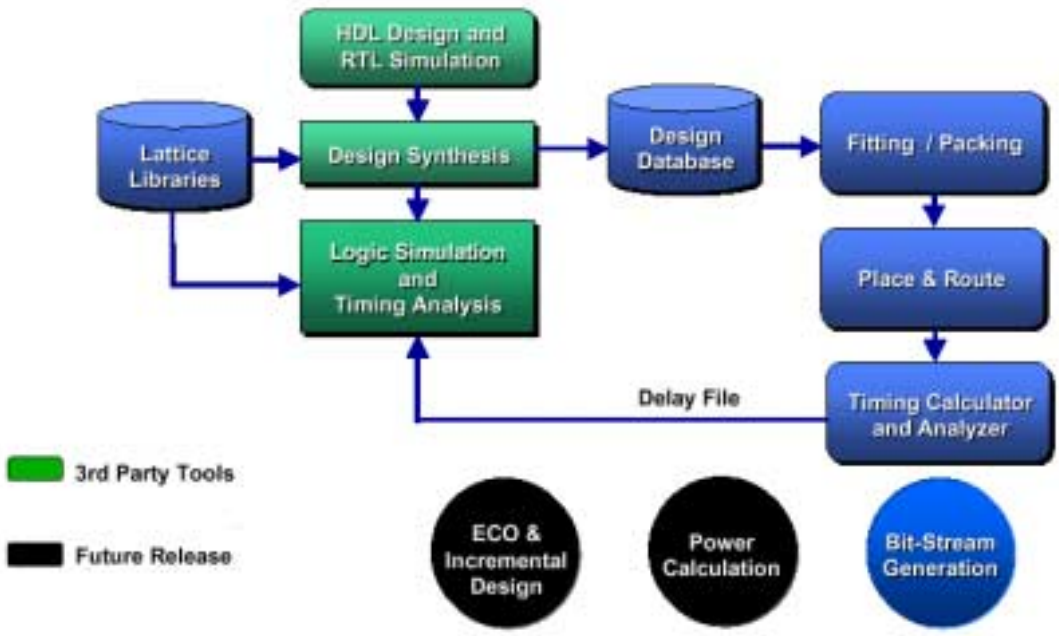
The ispMACH 5000VG implements its ISP through the IEEE 1532 In-system Configuration (ISC) standard. This maximizes interoperability when programming devices from multiple vendors on a single circuit board.

In addition, the ispMACH 5000VG devices have boundary scan test cells and are compliant to the IEEE 1149.1 standard. The test access port has its own supply voltage and can operate with the LVCMOS 3.3-, 2.5- and 1.8-volt standards. To facilitate a more efficient board test, the physical nature of the I/O cells can be configured quickly in a matter of milliseconds, without having to program the entire device. This allows board-level continuity test times to be reduced.

Design Environment – *ispLEVER*™

Lattice's new ispLEVER design tool supports ispMACH 5000VG device design. The ispLEVER tool has been designed as Lattice's design platform for the future. Building on the foundations of past design tools, ispLEVER includes fitting and usability enhancements that speed design and improve achievable performance.

Figure 5 – Typical ispLEVER Design Flow



The ispLEVER design tools include Timing Driven Design, a new Constraints Manager that provides the facility for defining sysIO, sysCLOCK PLL and pin assignments. The ispLEVER tool also provides enhancements to Lattice's Performance Analyst™, static timing analyzer, and other ease-of-use refinements, such as HTML Reporting and Navigation and the automatic

ispUPDATE™ feature. Every ispLEVER product includes Lattice's powerful In-System Programming tool, the ispVM™ System.

The ispLEVER design tools also integrate leading 3rd party CAE vendor tools including synthesis and timing simulation from Mentor Graphics® and Synplicity®. Figure 5 shows a typical design flow with the ispLEVER design tool.