

***LOW-COST FPGA CONFIGURATION VIA
INDUSTRY-STANDARD SPI SERIAL FLASH
&
LatticeECP/EC FGAs***

A Lattice Semiconductor White Paper

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Introduction

There are many criteria that a system designer must evaluate before making a choice of FPGA family and supplier. One of the decision criterion is FPGA “boot-up” configuration methodology. If the system design requires non-volatility, this issue is moot. A non-volatile FPGA, such as the Lattice ispXPGA®, will be selected. The ispXPGA family provides a single chip, self-booting FPGA solution. If, however, the system design needs are best met by a volatile FPGA, then the designer must also plan how that FPGA is going to be configured upon system boot-up.

If the system design has ready access to an on-board microcontroller and available system memory, and the designer is willing to write the code to properly configure the FPGA, then the incremental “configuration” cost of the total FPGA solution is insignificant.

For many system designs, however, a dedicated “Boot” memory is used to configure the FPGA at each system power-up. The unfortunate economic reality of this situation is that the vendor-specific Boot memory traditionally represents up to 30% of the total FPGA “solution” cost (FPGA + Boot memory).

Lattice has addressed this significant cost issue with its new LatticeECP™ (low-cost with high-performance dedicated functions) and LatticeEC™ (optimized for low-cost) families of FPGAs. Both the ECP and EC families can be configured directly from low-cost, industry-standard, third party SPI (Serial Peripheral Interface) Flash memories.

What is the SPI Interface?

The SPI interface is a 4-wire serial interface comprised of the following signals:

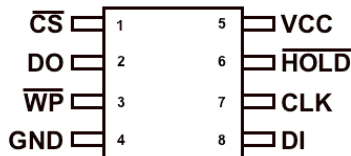
1. **CS – Chip Select:** Enables and disables device operation. When disabled, the device is at standby power levels. When enabled, the device powers up and instructions can be written to and data read from the device.
2. **CLK – Serial Clock:** Provides timing for serial input and output operations.

3. **DI – Serial Data In:** When the device is enabled, allows instructions, addresses and data to be serially written to the device. Data is latched on the rising edge of the Serial Clock.
4. **DO – Serial Data Out:** When the device is enabled, allows data and status to be serially read from the device. Data is shifted out on the falling edge of the Serial Clock.

In addition to the Vcc and Ground (GND) pins, the SPI interface supports the following two functions:

1. **HOLD:** Allows device to be paused while it is actively selected. This function is useful when multiple devices are sharing the same SPI signals.
2. **WP – Write Protection:** Used to prevent inadvertent writing to the Status Register Block Protect bits.

The standard, 8-pin, pin-out for most SPI Flash Memories is shown below:



SPI Flash Vs. Conventional Boot Memory

The ability to configure an FPGA with an SPI Flash Memory provides significant advantages over today's Boot Memory options.

- Broad, Third Party Vendor Base for SPI Flash
 - Competition Drives Lower Pricing and More Immediate Availability
- Lower Component Cost
 - Reduces Configuration Memory Portion of "Total FPGA" Cost
- Smaller Package/PCB Footprint
 - 8-Pin vs. 20-, 44- and 48-Pin Packages
- Broader Density Availability
 - 32M and 64M SPI Flash Densities Available Today

- Superior Density Migration Capability
 - All SPI Flash Densities Available in Same 8-Pin Package

Broad Third Party Vendor Base for SPI Flash

SPI Flash memories are relatively new to the marketplace. Most vendors introduced their SPI Flash product lines during the second half of 2003. However, there is already a significant number of SPI Flash suppliers in the market, with more memory suppliers expected to enter this popular market segment over the coming quarters. In general, 512K through 16M densities are available from multiple sources, with most suppliers having announced plans for 32M and 64M options in the coming quarters. Some of the current SPI Flash memory suppliers, and their products, are listed below:

Vendor	Family	512K	1M	2M	4M	8M	16M	32M	64M
STMicroelectronics	M25Pxx	X	X	X	X	X	X	X	X
Winbond	W25Pxx		X	X	X	X	X	X	
Silicon Storage Technology (SST)	SST25VFxx	X	X	X	X	X	X		
Spansion	S25FLxx				X	X	X	X	
Atmel	AT25Fxx	X	X	X	X	P			
PMC pFLASH	PM25LVxx	X	X	X	X				

X=Available today; P=Planned

Note: Availability based upon vendor web sites as of September 2005

Boot memory suppliers are more limited in number. Xilinx and Altera each offer a variety of Boot memory options targeted for their respective FPGA product families. Atmel offers a family of “FPGA Configuration EE Memory” devices available in two versions, one that is Altera-compatible and one that is Xilinx-compatible. However, Atmel only currently supports densities to 4M. For larger densities, designers must use

either a one- time-programmable solution from Xilinx or an expensive, two-chip, stacked package solution from Altera.

Vendor	Family	Features	512K	1M	2M	4M	8M	16M	32M	64M
Atmel	AT17LVxx	EEProm	X	X	X	X		P		
Xilinx	Legacy XC17Vxx	One-Time Programmable		X	X	X	X	X		
	Legacy XC18Vxx	Flash	X	X	X	X				
	Platform Flash XCFxx	Flash		X	X	X	P	P		
Altera	Config. Devices EPCxx	One-Time Programmable	X	X	X					
	Enhanced Config. Devices EPCxx	2-Chip "Stacked" Package: Flash+Controller				X	X	X		
	Serial Config. Devices EPCSx	Serial Flash		X		X		P		P

X=Available today; P=Planned

Note: Availability based upon vendor web sites as of June, 2004

Lower Component Cost

Given the significantly more competitive SPI Flash memory marketplace, driven by multiple suppliers with commodity, dual-sourced chips, it should come as no surprise that SPI Flash memories are priced more aggressively than the non-standard, proprietary Boot memories from Atmel, Xilinx and Altera.

To quantify this price advantage for SPI Flash, a comparison was made of published pricing (low volume) on distributor web sites for the SPI Flash vendors and for the Boot memory vendors (as of June 1, 2004). At each density level, the lowest price for any SPI Flash vendor was compared to the lowest price for any of the Boot memory vendors. While the absolute value of this pricing is certainly higher than most users would ever pay, the relative price relationships will likely hold true at higher volume pricing. The table below documents the average 71% cost savings available by using industry standard, third party SPI Flash memory versus conventional Boot memory.

Alternatively, one can say that the SPI Flash memory cost is only 29% of an equivalent-size Boot memory.

Density	Lowest Published Price (Any Vendor)		
	SPI FLASH	Boot PROM	SPI Lower By (%)
512K	\$ 1.10	\$ 3.50	69%
1M	\$ 1.25	\$ 3.30	62%
2M	\$ 1.70	\$ 5.70	70%
4M	\$ 2.15	\$ 8.40	74%
8M	\$ 3.00	\$ 15.85	81%
16M	\$ 6.70	\$ 20.95	68%
		Average:	71%

Another way to view the cost advantage of SPI Flash is to understand that conventional Boot memory can represent anywhere from 5% to 30% of the “total FPGA solution cost,” depending upon the FPGA/Boot memory densities. At the smaller densities, the Boot memory represents a more significant percentage of the total FPGA solution. With SPI Flash, this percentage range drops to <1% to <10%. The following table shows 100+ piece Unit Prices for Xilinx’s Spartan III and associated Xilinx “Platform Flash” Boot PROM.

FPGA + Boot Memory		100+ Unit Price		TOTAL COST	PROM % of Total
Spartan-3	Platform Flash	Spartan-3	Platform Flash		
XC3S50	XCF01S	\$8.15	\$3.30	\$11.45	29%
XC3S200	XCF01S	\$14.35	\$3.30	\$17.65	19%
XC3S400	XCF02S	\$25.15	\$5.70	\$30.85	18%
XC3S1000	XCF04S	\$55.60	\$8.40	\$64.00	13%
XC3S1500	XCF08S	\$98.25	\$15.85	\$114.10	14%
XC3S2000	XCF08S	\$176.50	\$15.85	\$192.35	8%
XC3S4000	XCF16S	\$324.35	\$20.95	\$345.30	6%
XC3S5000	XCF16S	\$409.55	\$20.95	\$430.50	5%

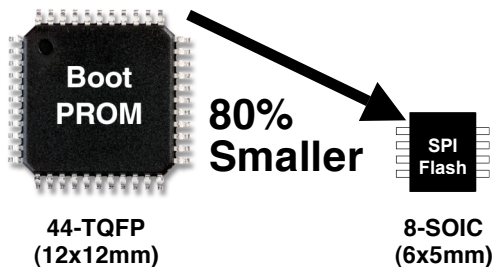
Smaller Package/PCB Footprint

One of the key advantages of using SPI Flash memory is that all density options are available in the 8-Contact MLP (Micro Leadframe Package). This tiny package features a 6 x 5mm body size/PCB footprint. For 16M densities and smaller, the SPI Flash memories are also available in a lower cost, conventional 8-pin SOIC package. This package has the same PCB board footprint (6 x 5mm) inclusive of leads.

Boot memories, on the other hand, come in a variety of package styles that vary from vendor to vendor for a given memory density. Common packages vary by density and include:

- 8-Pin DIP
- 20-Pin PLCC, SOIC, and TSSOP
- 32-Pin TQFP
- 44-Pin TQFP and PLCC
- 48-Pin TSOP
- 48-Ball csBGA
- 88-Ball □BGA
- 100-Pin PQFP

As an example of the significant board area savings associated with the use of SPI Flash memory, consider the case of configuring an FPGA that requires 4M, 8M or 16M of memory. The SPI Flash package requires 30mm² (6 x 5mm) of PCB area, compared to the 44-Pin TQFP package, which requires 144mm² (12 x 12mm) of PCB area. The SPI Flash is ~80% SMALLER than the equivalent Boot memory.



Note: All dimensions include package leads. Size is not actual, but is proportional.

Broader Densities Available

From the earlier tables above showing Vendor/Density product offerings, one can see that SPI Flash memory is broadly available from multiple vendors at the 512K through 64M density levels.

For “conventional” Boot memory, Atmel, the only “independent” supplier, supports up to 4M (with a 16M device planned). Xilinx supports up to 16M with an older, one-time-programmable offering and Altera supports up to 16M with an expensive, dual-stacked-chip solution. None of these vendors has plans to support 32M, and only Xilinx has announced plans for a 64M device that supports only two of its FPGA product families.

Designers looking for a full portfolio of configuration memory densities will certainly prefer the SPI Flash memory approach.

Superior Density Migration Capability

Another key advantage of the SPI Flash memory approach is “density migration.” With SPI Flash, any density point from 512K through 64M is available in the same, 8-Contact MLP package. Designers can lay out their prototype boards for this single package footprint without concern over having to re-spin the board for a different memory size.

This feature is particularly useful with the LatticeECP and EC FPGA families, because they both support data compression of the configuration datastream. Designers can complete the debug of their systems using a large SPI Flash memory. After the design has been finalized and the final compressed datastream file size is known, the designer can downsize the configuration memory to accommodate the compressed file for the production builds. The PCB does not need to be touched.

LatticeECP/EC Product & Configuration Overview

LatticeECP/EC Overview

The LatticeECP-DSP family provides advanced DSP blocks coupled with an efficient FPGA fabric, resulting in higher DSP performance and improved logic utilization. For

even lower cost solutions, the LatticeEC family supports all the features of the LatticeECP-DSP family without dedicated DSP resources.

The LatticeECP and EC families both utilize a silicon-efficient FPGA fabric in which I/O capability, distributed memory, embedded memory, logic and routing have been optimized for high-volume markets.

The LatticeECP-DSP is ideal for use in applications in which cost-effective DSP functionality is needed. Such applications include software-defined radio, wireless communications, military applications and video processing equipment. LatticeEC devices are ideal for general non-DSP applications such as low-cost networking, blade servers, network access equipment, consumer electronics, industrial, medical and automotive applications.

Key Features and Benefits

- **Low-Cost FPGAs**
 - Features optimized for mainstream applications
 - Balanced logic / memory / I/O resources
- **High Performance sysDSP™ Blocks (LatticeECP-DSP)**
 - Multiply, accumulate, addition and subtraction
 - Input, intermediate and output pipeline registers
 - 4 to 8 sysDSP blocks per device
 - Each block supports multiple 9x9, 18x18 & 36x36 multipliers
- **Extensive Density and Package Options**
 - 1.5K to 32.8K LUT4s; 67 to 496 I/Os
 - Density migration supported
 - TQFP, PQFP and fpBGA packaging options
- **Embedded and Distributed Memory**
 - 18 Kbits to 498 Kbits sysMEM™ Embedded
 - Block RAM (EBR)
 - Up to 131 Kbits distributed RAM
- **Flexible I/O Buffer**
 - Hot Socketing
 - Programmable sysIO™ buffer supports wide range of interfaces:
 - LVCMOS 3.3/2.5/1.8/1.5/1.2
 - LVTTTL

- SSTL 3/2 Class I, II, SSTL18 Class I
- HSTL 18 Class I, II, III, HSTL15 Class I, III
- PCI
- LVDS, Bus-LVDS, LVPECL, RSDS
- **Dedicated DDR Memory Support**
 - Implements interface up to DDR400 (200MHz)
- **sysCLOCK™ PLLs**
 - Up to 4 analog PLLs per device
 - Clock multiply, divide and phase shifting
- **System Level Support**
 - Standard IEEE 1149.1 Boundary Scan, plus ispTRACY™ internal logic analyzer capability
 - Industry standard, third-party SPI boot flash interface
 - 1.2V power supply

The LatticeECP-DSP and LatticeEC FPGA Families

Parameter	EC1	EC3	ECP6 / EC6	ECP10 / EC10	ECP15 / EC15	ECP20 / EC20	ECP33 / EC33
PFU/PFF Rows	12	16	24	32	40	44	64
PFU/PFF Columns	16	24	32	40	48	56	64
Number of PFUs/PFFs	192	384	768	1280	1920	2464	4096
sysDSP Blocks*	—	—	4	5	6	7	8
18x18 Embedded Multipliers*	—	—	16	20	24	28	32
LUTs (K)	1.5	3.1	6.1	10.2	15.4	19.7	32.8
Distributed RAM (K bits)	6	12	25	41	61	79	131
EBR Block SRAM (K bits)	18	55	92	277	350	424	535
Number of EBR SRAM Blocks	2	6	10	30	38	46	58
V _{CC} Voltage (V)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Number of PLLs	2	2	2	4	4	4	4
Packages & I/O Combinations							
100-pin TQFP (14 x 14 mm)	67	67					
144-pin TQFP (20 x 20 mm)	97	97	97				
208-pin PQFP (28 x 28 mm)	112	145	147	147			
256-ball fpBGA (17 x 17 mm)		160	195	195	195		
484-ball fpBGA (23 x 23 mm)			224	288	352	360	360
672-ball fpBGA (27 x 27 mm)						400	496

Configuration Memory Requirements

The ECP/EC FPGA families both support compression of the configuration datastream. For most datastreams, one can expect a file size reduction of up to 25%. The original device configuration datastream is compressed by the Lattice ispLEVER® development tool. The ECP/EC devices each contain an on-board decompression “engine” which

decompresses the incoming configuration datastream from the SPI Flash. This compression capability, in many cases, allows a smaller capacity SPI memory device to be used. For example, the EC20 device, containing 5.3M configuration bits, would normally require an 8M SPI memory. With a datastream compression of 25%, the EC20 device can now be configured from a 4M SPI memory, further reducing overall system costs.

The following table summarizes the SPI memory size requirements for the ECP/EC FPGA families:

Family	Member	LUTs (K)	Max Config Bits (M)	Required SPI Memory (M)	
				w/o Comp	w/Comp
EC	1	1.5	0.6	1	512K
	3	3.1	1.1	2	1
EC/ ECP	6	6.1	1.8	2	2
	10	10.2	3.1	4	4
	15	15.4	4.3	8	4
	20	19.7	5.3	8	4
	33	32.8	7.9	8	4

The shaded cells highlight those cases in which the datastream compression capabilities of the ECP/EC families enabled the use of a smaller SPI memory device. In all but two cases, the required Boot memory was cut in half.

SPI Flash Interface to Lattice ECP/EC

How are the LatticeECP/EC devices able to interface with all third party SPI Serial Flash memories? Lattice takes advantage of the fact that the vast majority of SPI Serial Flash vendors utilize the same set of Operation Codes (OP Codes). In particular, the common Op Code for the “Read Data” command is “03H”. The ECP/EC devices have hardwired

the 03H Op Code into device silicon. When the ECP/EC device is powered up, it automatically enables the SPI Flash memory via the Chip Select (CS) pin and follows that with the “03H” Read Op Code combined with Memory Address “0”. The SPI memory device then outputs the configuration datastream to the ECP/EC device. This simple, 4-wire (1 Data, 3 Control) configuration mode is referred to as “SPI3,” referencing the 03H Read Op Code.

In addition, the “SPIx” mode allows the ECP/EC devices to easily interface with SPI Flash memories with a Read Op Code other than “03H”. This mode is also useful for supporting other Op Codes available on these or the “SPI3” class of SPI memories, such as the “0BH” Fast Read Op Code, which effectively doubles the data output rate from ~20MHz to ~40MHz. This 11-wire (8-Data, 3-Control) interface determines the desired Op Code on the 8 Data I/Os of the sysCONFIG Programming Port (D7:0) of the ECP/EC devices. To use this mode, the 8-bit Op Code is “hardwired” on the PCB with weak (4.7KΩ) resistors on the D7:0 pins. At power-up, the ECP/EC devices extract the Op Code from the D7:0 Data I/Os and pass it onto the SPI Flash memory.

SPI Flash Programming Support

The Lattice ispVM[®] System, combined with a Lattice ispDOWNLOAD[®] Cable (fly-wire), supports programming of SPI Serial Flash memory in either of two modes:

1. Directly via a dedicated SPI interface/header connected to the SPI Flash (today).
2. Directly via the JTAG interface/header connected to the ECP/EC device and the SPI Flash.

Summary

By supporting configuration via industry-standard, third party SPI Serial Flash memory, Lattice’s ECP/EC FPGA families provide system designers with a significantly more cost-effective configuration option than is available with other competitive FPGA solutions.

In addition to being priced significantly lower than conventional Boot memory solutions, SPI Flash is available in a wide range of memory densities, all in the same, space-conscious 8-pin package. The pain-free density migration capability of SPI Flash can be used to leverage the data compression capabilities of the ECP/EC products. Finally, Lattice development tools provide a comprehensive portfolio of SPI Flash configuration solutions to speed the development effort.

By supporting the use of low-cost, industry-standard, third party SPI Serial Flash, Lattice delivers a truly cost-effective FPGA solution. Compared to alternative FPGAs currently available, the LatticeECP/EC “total FPGA solution” delivers users a 30%-50% cost savings.ⁱ

ⁱ Based upon published competitive pricing as of June 1, 2004

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