Flexible Power-Up Sequencing for LCDs Using A Programmable Power Manager IC

A Lattice Semiconductor White Paper

April 2005

Lattice Semiconductor
5555 Northeast Moore Ct.
Hillsboro, Oregon 97124 USA
Telephone: (503) 268-8000
www.latticesemi.com

Introduction

For many systems, LCDs are a large part of the BOM. In some cases, such as HDTVs, more than 80% of the entire system cost is that of the LCD panel. From a perceived quality perspective, if the LCD begins to fail the end customer will associate the system and its manufacturer with poor quality. Clearly, safeguarding the LCD component is a critical aspect of these system designs.

LCDs are typically comprised of a liquid crystal fluid sandwiched between two polarizing layers of glass or plastic, separated into cells (pixels). For color LCDs, each pixel is divided into three sub-cells—red, blue and green. When a voltage is applied across these LCD sub-cells, a certain amount of light passes through the LCD cell from the backlight or reflective surface, depending upon the voltage applied and polarization of the liquid crystal fluid.

LCDs use thin film transistors (TFT) or electrodes in a matrix of rows and columns on the glass substrate to apply voltage across a particular sub-cell, and to control the amount of voltage applied to the crystal fluid. The crystal in the sub-cell twists, based on the amount of voltage applied to the electrodes, allowing light to pass from the backlight through to the polarized glass. Typically, 256 levels of brightness (8-bits) voltage can be applied to the sub-cell, twisting the crystal in up to 256 positions, from open to closed and from bright to dark. Note that 24-bit color is three strings of 8-bit brightness for the red, blue and green sub-cells.

In order for the LCD to operate reliably, the liquid crystal fluid must be protected from the DC voltages (typically negative) that cause breakdown. If too much DC current inadvertently flows through the LCD fluid, the fluid will become damaged, electrochemically decomposing and breaking down over time as the fluid changes state. This change in state becomes noticeable as the color of the liquid crystal pixel changes. Given further damage, gas bubbles will form inside the liquid crystal cell, resulting in permanent damage and a noticeable degradation of display quality. Pixel damage cannot be repaired.

Preventing LCD Break Down: Power-up Sequencing

In order to prevent any DC current from damaging the liquid crystal fluid, some LCDs have an “M” clock which, when activated at power-up, produces an AC current wave on the electrodes and into the fluid cells before the display “comes to life,” protecting the cells from breakdown. Many LCDs have built in controllers that require DC logic signals upon power-up. Care must be taken in the order and timing of how power is applied to the LCD. The Vcc supply voltage is usually turned on first; then, within 10-20ms, all logic and data signals are applied. If the data signals come in either before or too long after Vcc power-up, latch-up or damage to the LCD cells can occur. Similarly, at power-down, removal of Vcc is usually delayed until the logic and data signals have been turned off. All LCDs have power-up sequencing requirements of some type. The key to power-up sequencing requirements is to make sure that the LCD fluid is protected from DC voltages without the AC wave being setup, within the requirements provided by the LCD vendor.

This white paper examines a solution that not only provides proper power supply sequencing to an LCD panel but also prevents the LCD panel from getting damaged due to faulty power supply and faulty controller. Additionally, this solution can be easily customized across multiple types of LCD displays.

LCD System Design Example

A basic power-up sequence for a popular 18-inch TFT LCD is shown in Figure 1 below. For this particular LCD, Vcc needs to be powered up before data comes in, no longer than 10ms, and the ramp rate of Vcc must not be longer than 60ms. Vcc cannot go below 11.4V for more than 20ms, and if Vcc goes below 9.6V, a proper power-down sequence should occur. If the design is to support LCDs from multiple vendors, then multiple power-up circuits will most likely be required.

Support for multiple LCD vendors' timing requirements can be complex, since the values shown in Figure 1 for t3, t2, and Vcc can vary.

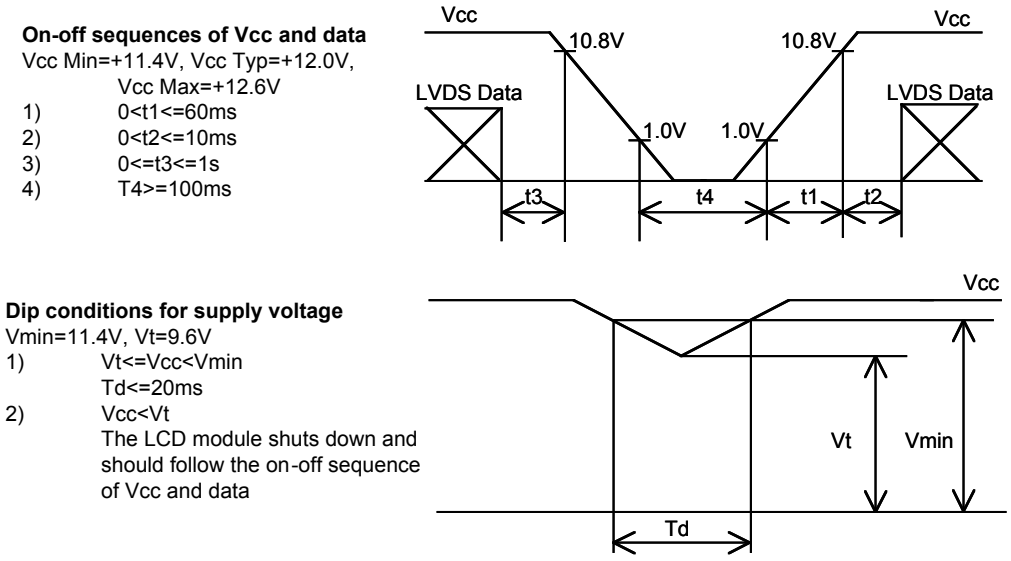

Figure 1- Example of power-up sequencing waveform for TFT LCD

Single system support for multiple LCD vendors can be extremely beneficial, since multi-vendor competition often leads to price reductions of 10% or more. In addition, if an LCD vendor decides to obsolete a particular LCD, and the design supports multiple vendors, the design will easily accommodate the switch to another vendor.

Protection From Faulty Power Supplies

The focus so far has been on power-up sequencing requirements for the LCD, with the assumption that the power supply is operating correctly. Now consider a case in which the power supply itself becomes faulty. In this case, the LCD needs protection from the damage that could be caused by the faulty power supply; this is accomplished by ensuring that the unwanted DC current is not pumped into the LCD fluid. The end customer will find a minor repair for a faulty power supply more tolerable – and less damaging to the manufacturer's reputation – than a complete LCD replacement.

In order to protect the LCD from a faulty power supply, a circuit is required that senses the correct operation of the power supply and only then supplies DC to the LCD controller in the proper sequence for a particular LCD.

Integrating Additional Power-Up Circuitry

Power-up circuitry to protect the LCD from unwanted DC at power-up and faulty power supplies can be complex, requiring several analog and digital components. Since the system design will require power-up and faulty power supply protection of some type, it would be preferable to be able to re-use some or all of this circuitry for additional portions of the system. Many chips common in systems also have power-up sequencing and timing requirements: e.g., ASICs, DSPs, ASSPs, FPGAs and microprocessors, to name a few, many of which comprise much of the overall system cost. Coordinating the power-up of the I/O and core supply voltages and protecting these chips, in conjunction with the LCD, would be yet another important aspect of the system design. To further complicate matters, some of these chips might require their highest voltage to be turned on prior to their lowest voltage, or vice versa, and also require the reverse for power-down.

In most cases, however, protecting two different chips or two different LCDs would require a completely different power-up circuit, a different design and more components.

LCD System Solution Using A Programmable Power Manager IC

Traditionally, designers have addressed the power supply sequencing, monitoring for faulty power supplies, as well as the power supply management of the controller board, individually, by using standard off-the-shelf power management ICs like supervisors, reset generators, sequencers, charge pumps,

etc. Not only does this approach often result in a solution that requires multiple ICs (in some cases from different vendors), it also is a solution that is inflexible, because the complete system level management function has to be realized by hardwiring individual power management ICs together. This renders the changing of the LCD panel (to address obsolescence or cost reduction) not only a time consuming exercise, but also one that will often require a total redesign of power management.

The use of programmable power management ICs for this function, on the other hand, not only requires fewer ICs to implement the complete function, but also eases modification of the power management function to accommodate different power supply sequencing and monitoring, and timing functions.

Detailed Circuit Description

Figure 2 shows the power supply arrangement for the LCD panel as well as its control circuitry. The LCD Panel is powered by the +12V Supply through a MOSFET for controlling its turn-on/off ramp rate. The supply voltage is monitored for four different voltage threshold levels to meet its sequencing and monitoring specifications. As described earlier, the power supply-sequencing algorithm also factors in the presence of clock/data at the input of the display and this part of the specification is met by monitoring the data presence through a low-pass filter and controlled by a LVDS buffer. There are three power supplies, 3.3V, 2.5V and 1.5V, generated locally in the system that are also controlled and monitored to meet the power management requirements of other logic control circuitry.

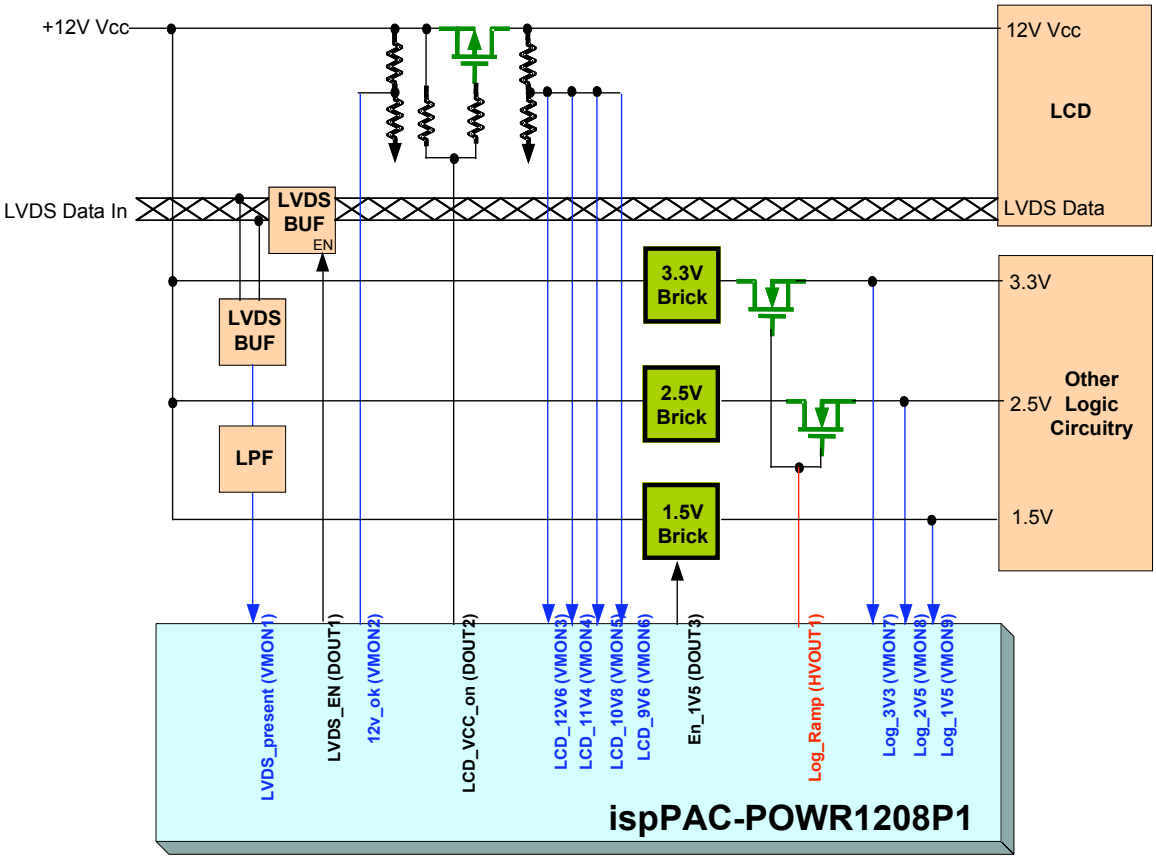

Figure 2 - LCD Power-Up System Block Diagram

The design is straightforward for the LCD power-up/power-down sequencing and monitoring. The signals used for the device employ the following convention: signal name (device pin). The low pass filter averages the LVDS data and generates the LVDS present signal. The threshold is set at 80mV to detect the presence of data with very few excursions to logical 1. The 80mV precision feature of the power manager IC allows the LVDS present signal to be detected. LVDS_EN enables LVDS data into the LCD through an LVDS buffer. 12V_OK checks for faulty power supply (above 10.8V). LCD_Vcc_on connects Vcc to the LCD through a p-channel MOSFET. LCD_12V6 monitors Vcc>12.6V, which would result in a shutdown sequence. LCD_11V4 monitors Vcc>11.4V, which is the low point of proper Vcc operation. If the power supply falls below this level, a 20ms timer is started. A shutdown procedure is initiated if either the timer expires or the voltage drops below 9.6V. LCD_10V8 monitors Vcc>10.8V, which is the threshold to begin the timer between Vcc and LVDS Data. LCD_9V6

monitors Vcc>Vt, requiring a proper shutdown if Vcc dips below Vt. The remaining signals are used for 3.3, 2.5 and 1.5V bricks to power additional logic circuitry. These power supplies are turned on starting with 1.5V first and followed by 2.5V and 3.3V tracking each other. In case of a faulty (12V_OK) signal, these supplies are turned off with 2.5V and 3.3V first, followed by 1.5V.

Power Management Algorithm Through Software

Power management designs using the programmable power manager IC are implemented using the software tool, PAC-Designer. The monitoring voltage threshold, current to control the ramp rate through the MOSFET, logic algorithm that controls the sequence of events including the power supply sequencing of the controller board, LCD panel, monitoring of power supply voltages, as well as corrective action under power supply faults are all implemented using software.

Because the power management algorithm is entirely implemented in software, changing the design to accommodate the power supply management requirements for a different LCD panel can be achieved simply by changing the software code implemented on the programmable power manager IC device.

Summary

Power management solutions for LCD panels from multiple vendors can vary greatly. Designing a standardized power management solution to accommodate LCD panels from multiple vendors usually results in a solution that is both expensive and requires many off the shelf power management devices.

Programmable power management devices, such as the Lattice Power1208P1, offer not only a convenient solution for power management and sequencing for LCDs from multiple vendors, but also can be used to offload additional power-up tasks such as logic circuitry. Since power-up management can be integrated into one programmable design platform, the benefit to the designer is clear: the

device can be re-programmed during manufacturing to support multiple display vendors.

###