# HDL Synthesis Design with Synplify: ORCA Flow

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# HDL Synthesis Design with Synplify: ORCA Flow

This tutorial shows you how to use Synplify from within ispLEVER® to synthesize a Verilog design and generate an EDIF netlist file. You will implement the design in a Lattice ORCA FPGA device and prepare the design for ModelSim timing simulation.

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***Note**: If you want to learn how to use Synplify in standalone mode, or understand more about its advanced features, please download or view the ORCA Synplicity Interface Manual online in PDF format by selecting **Help > ispLEVER Documentation Library** in the ispLEVER Project Navigator.*

## Learning Objectives

When you have completed this tutorial, you should be able to:

- Use ispLEVER to create a new EDIF project and target a device.
- Launch Synplify from within ispLEVER, synthesize your Verilog design, and generate an EDIF netlist file.
- Import the EDIF file into the ispLEVER.
- Implement the design using the Map, Place, and Route processes and view the reports.
- Prepare the design for timing simulation using ModelSim.

## Time to Complete This Tutorial

The time to complete this tutorial is about 20 minutes.

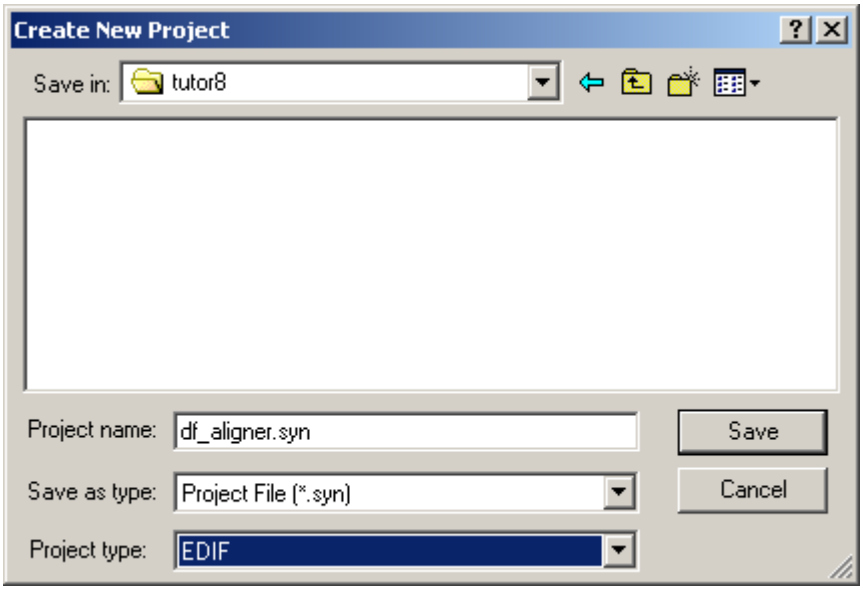
## Task 1: Create a New Project

To begin a new project, you must create a project directory. Then you must give the project file (`.syn`) a name and declare the project type (EDIF).

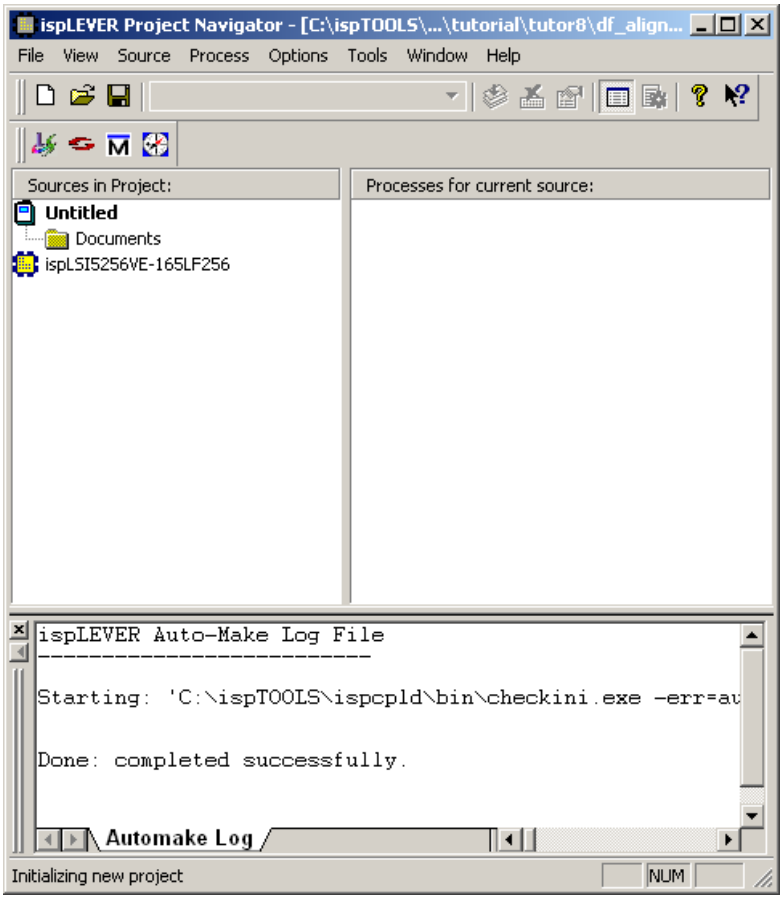
The ispLEVER software saves an initial design file with the `.syn` file extension in the directory you specify. All project files are copied to or created in this directory. The project type specifies that all design sources will be of this type.

*To create a new project:*

1. Start the ispLEVER system, if it is not already running.
2. In the Project Navigator, choose **File > New Project** to open the Create New Project dialog box.
3. In the dialog box,
   - Change to the directory: `<install_path>\ispcpld\examples\tutorial\`**`tutor8.`**
   - In the Project name box, type **`df_aligner`**.
   - In the Project type box, select **EDIF**.
   - Click **Save**.



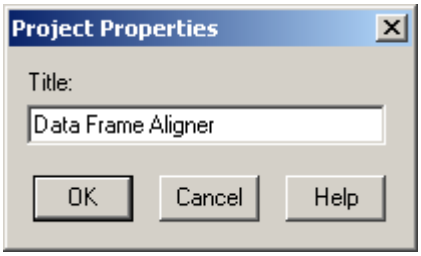
In the Sources window, the project title defaults to `Untitled`. You will change the project title in the next step.




4. In the Sources window, double-click the project title (**`Untitled`**) to open the Project Properties dialog box.

   The default title for a new project is "Untitled." You can create a title for the project with as many characters as you want. The title can contain spaces and any other keyboard character except tabs and returns.

5. In the Title text box, type **`Data Frame Aligner`** and click **OK**.



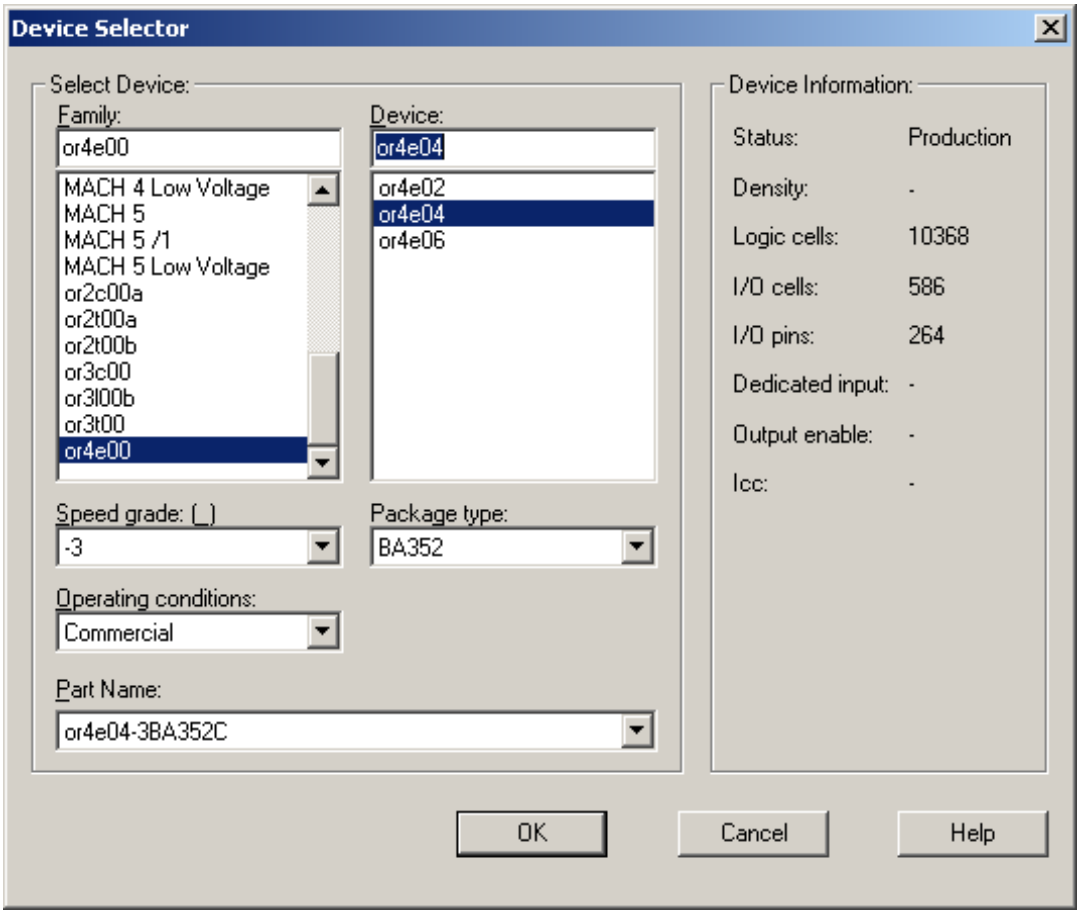

 

## Task 2: Target a Device

In the Project Navigator Sources window, there is a device icon next to the target device for the project. The Project Navigator lets you target a design to a specific Lattice device at any time during the design process. A default device for the project is already selected, but you will target an ORCA FPGA device for this tutorial.

*To view the list of available devices and to change the target device:*

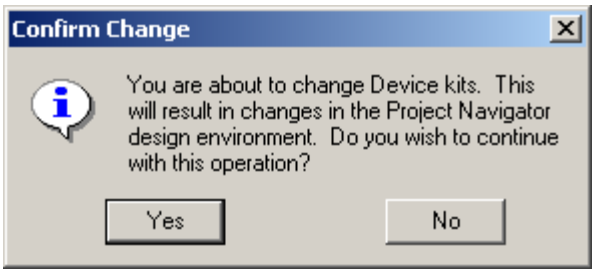
1. In the Sources window, double-click the **target device name** to open the Device Selector dialog box. The Device Selector dialog box shows the default device as well as all available devices and their options.



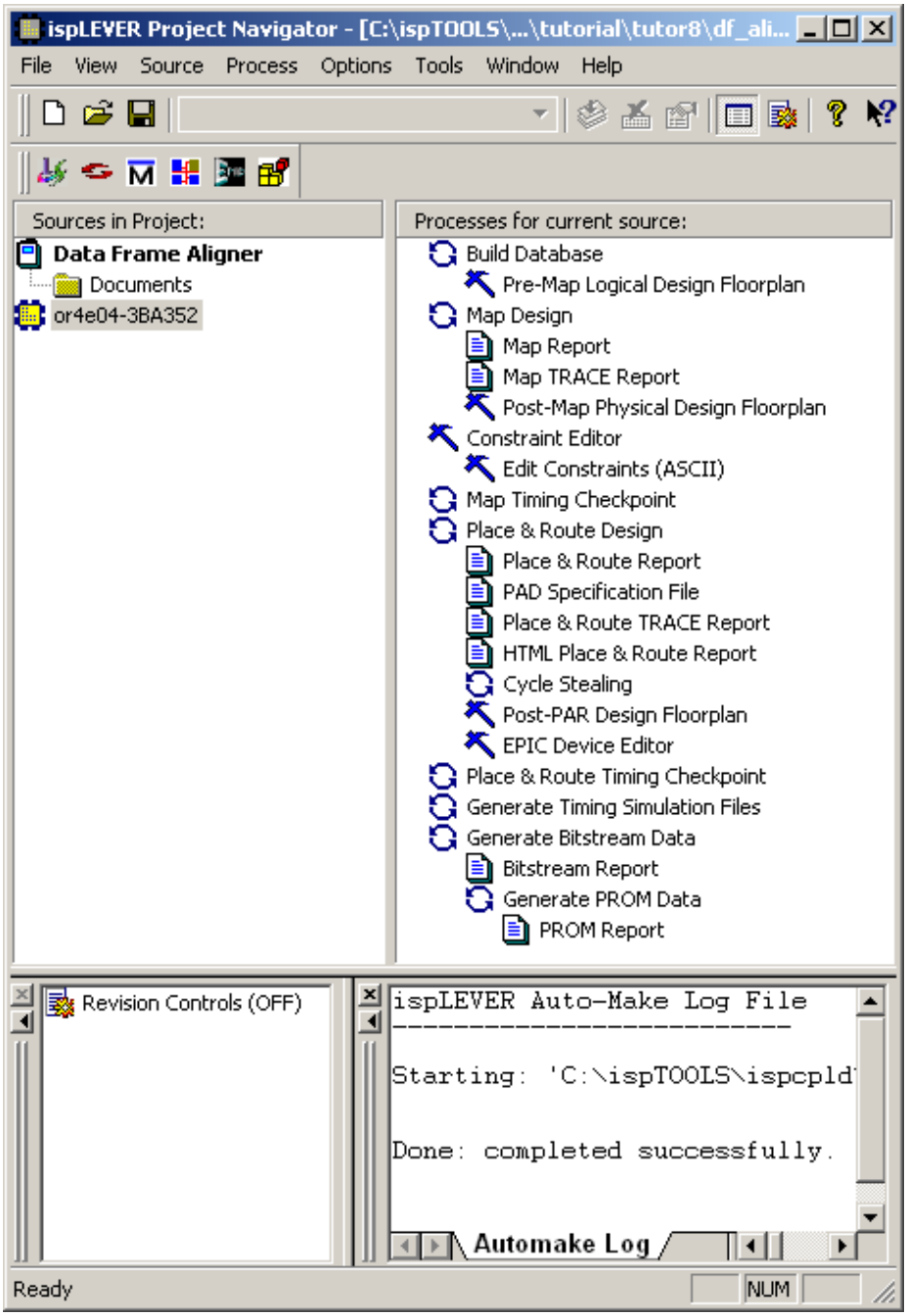

In the dialog box:

- Under Family, select **or4e00** from the drop-down list.
- Under Device, select **or4e04**.
- Click **OK**.

2. In the message box, click **Yes** to change device kits.




3. Your Project Navigator should look like this:



## Task 3: Create a Synplify Project

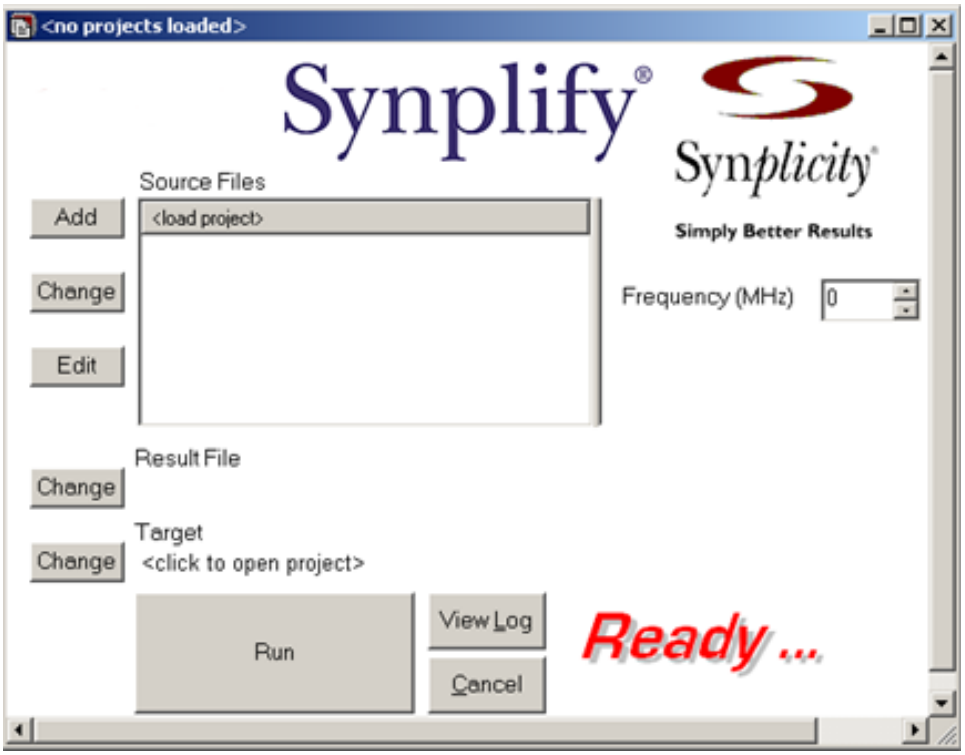
For HDL designs, the ispLEVER software provides two synthesis tools that are integrated into the Project Navigator environment: *Synplify for Lattice (*Synplify*)* and *LeonardoSpectrum*. You can synthesize your Verilog or VHDL design as a standalone process by choosing the synthesis tool from the Lattice Semiconductor program group in your Start menu, or you can synthesize automatically and seamlessly within the Project Navigator.

### About Synplify

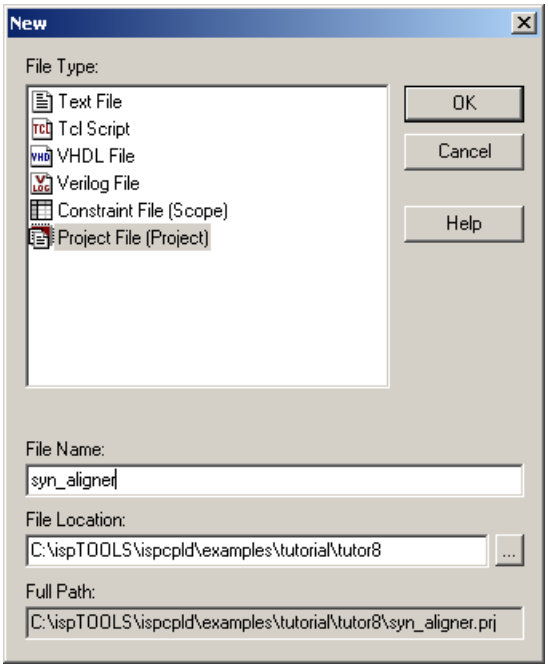
Synplify is a logic synthesis tool that starts with a high-level design written in Verilog or VHDL hardware description languages (HDLs). Then Synplify converts the HDL description into small, high-performance, design netlists that are optimized for Lattice devices.

*To start Synplify:*

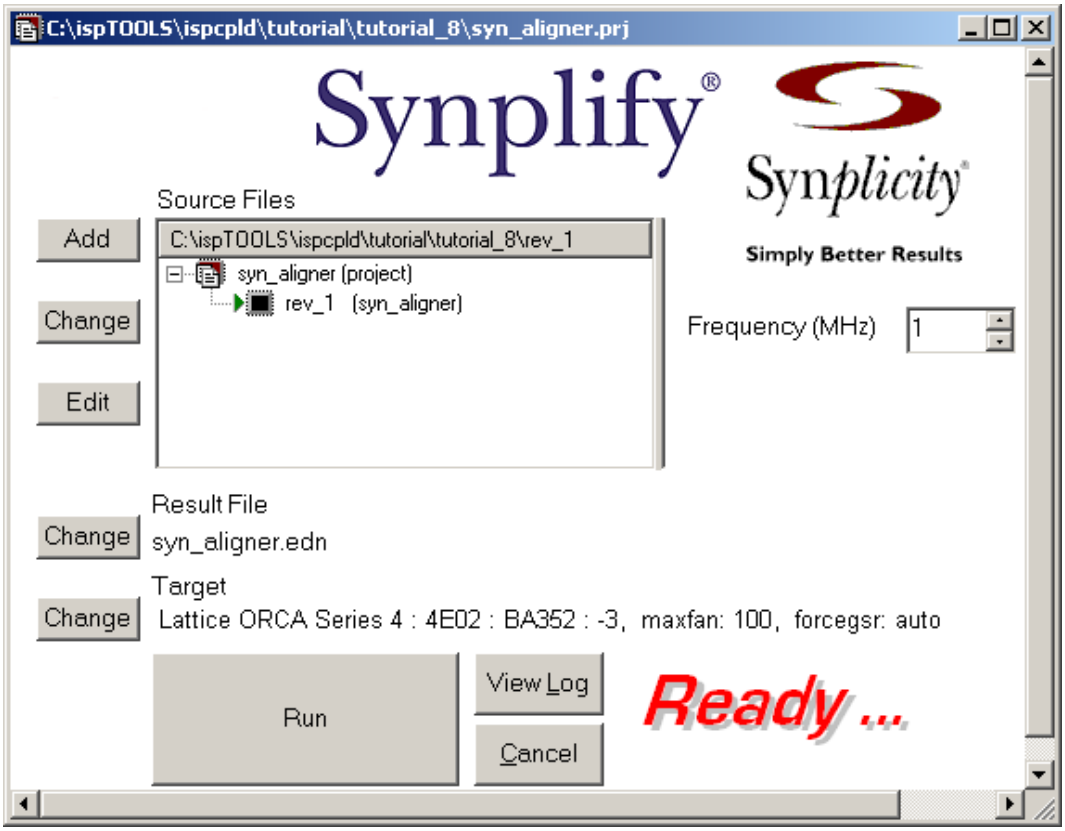
1. In the Project Navigator, choose **Tools > Synplify Synthesis** to open the Synplify synthesis tool in the Project view.




2. Choose **File > New** to open the dialog box. In the dialog box, do the following:
   - Under File Type, select **Project File**
   - Under File Name, type **`syn_aligner`**
   - Under File Location, make sure you are in the **tutor8** folder
   - Click **OK**




3. The Synplify screen should look like this:



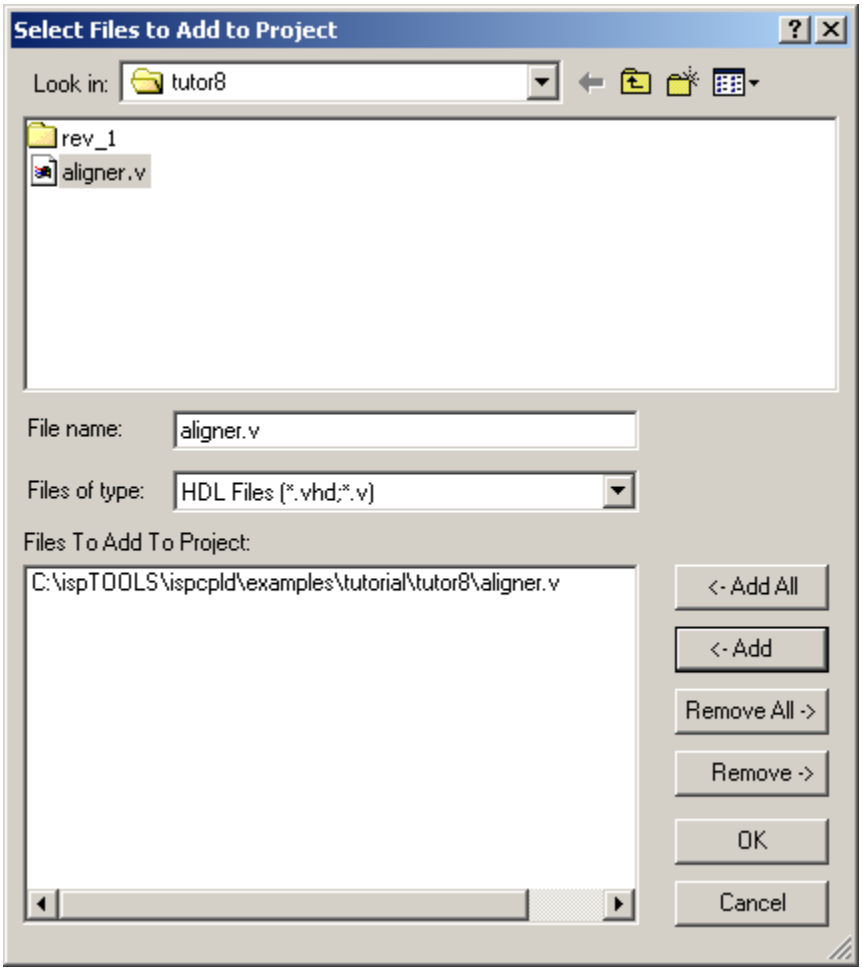

 

## Task 4: Add the Verilog Source Files

In this task you will add Verilog source files to the project.

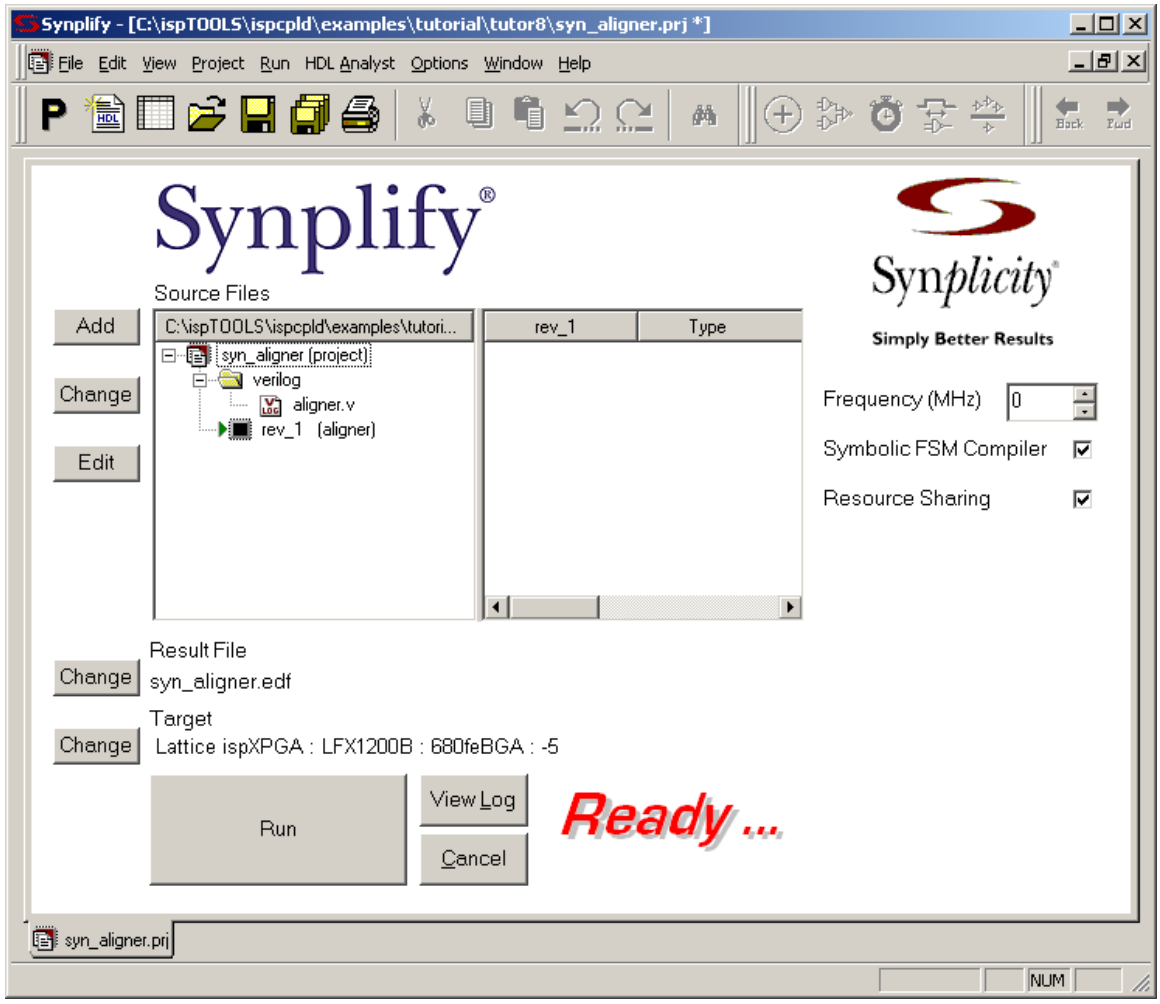
*To add source files to the project:*

1. On the Synplify main window, click **Add** to open the dialog box. You should see one Verilog file named `aligner.v`.
2. Select the file and click **Add** to add the Verilog file to the project (shown in the Files To Add To Project field).




3. Click **OK** to close the dialog box.

4. In Synplify, expand the **verilog** folder. The Synplify screen should look like this:



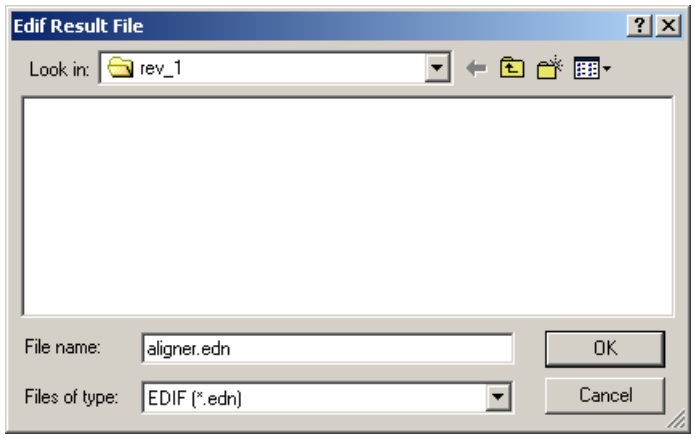

 

## Task 5: Set Implementation Options

Synplify has probably set your implementation options correctly. However, it is good practice to check them.

*To set the implementation options:*

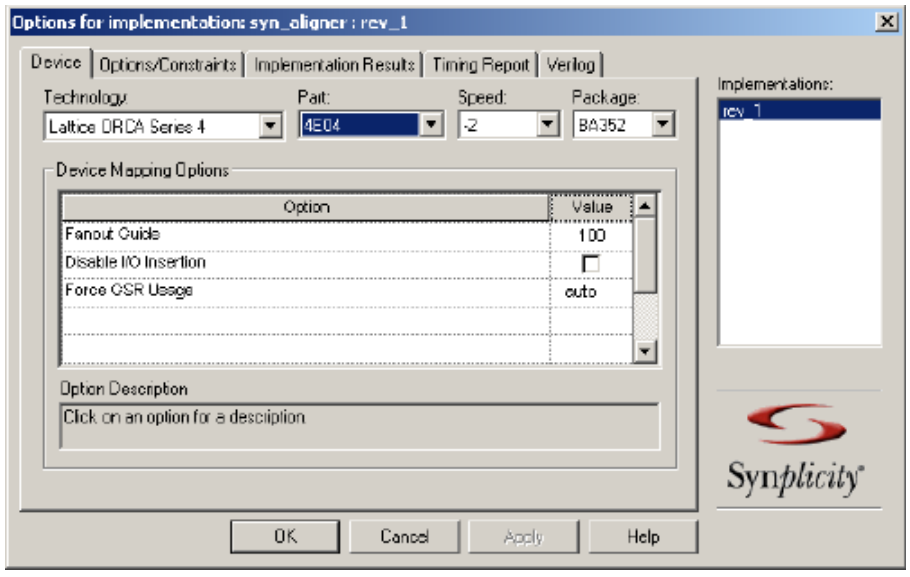
1. Below the Source Files project window, click the **Change** (**Results File)** button to open the dialog box.



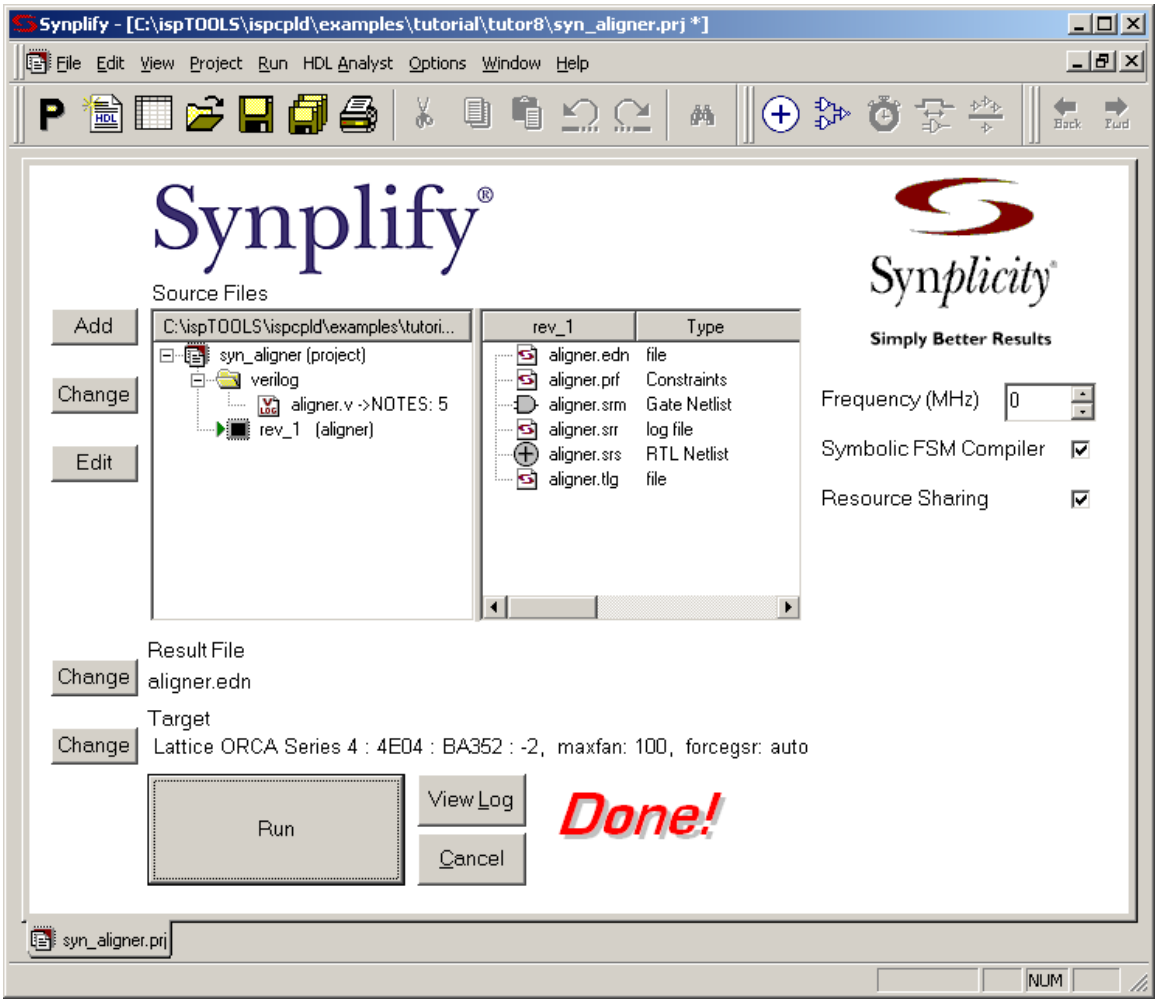

   This dialog box allows you to change the file name or destination of the output EDIF file. In this tutorial, we will not change anything so all our project files remain in our current project directory. Notice that Synplify automatically creates revision folders inside your project folder. You should be in the `rev_1` folder, inside your project folder.

2. Click **Cancel** to close the dialog box.

3. Below the Change (Results File) button, click the **Change** (**Target)** button to open the dialog box.



4. Under Technology, select **Lattice ORCA Series 4**. Under Part, select **4EO4**. Click **OK** to close the dialog box.
5. Click the large **Run** button to start the synthesis process. Synplify synthesizes the Verilog design and creates an EDIF file, as well as several other files, and displays them in the window. If you like, you can double-click the different file names and view them. When you are finished, close the files.




6. Choose **File > Save** to save the Synplify project.
7. Choose **File > Exit** to exit Synplify. The Project Navigator Main window will be activated again for the next task.

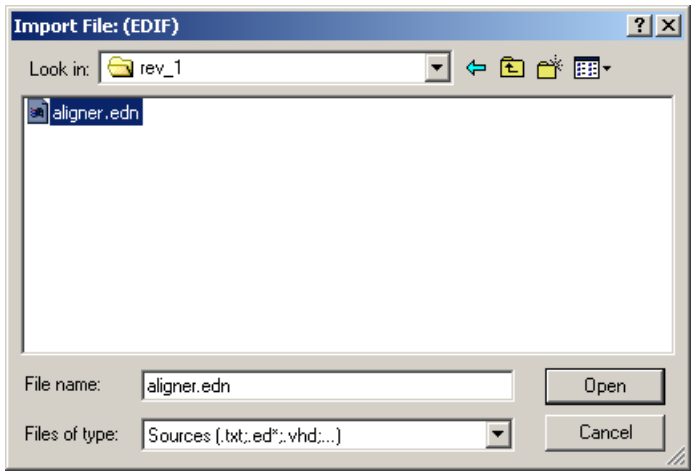
 

## Task 6: Import the EDIF File into Your Project

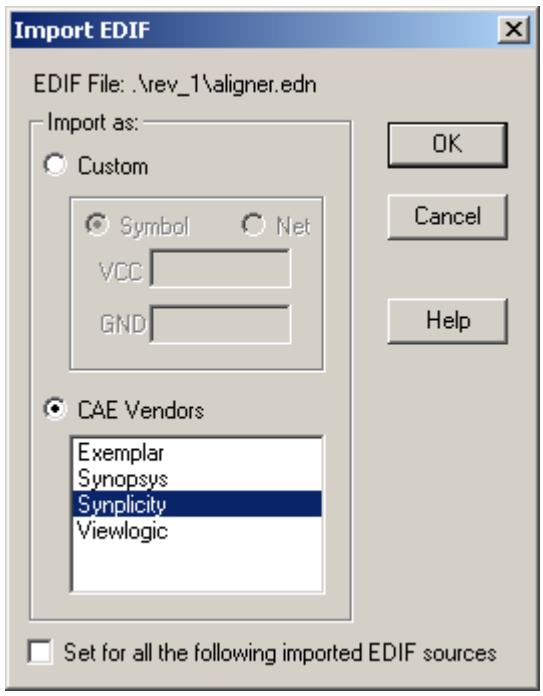
Using the Project Navigator, you can import EDIF 2.0.0 netlists from third-party synthesis tools, such as Synplicity Synplify, into ispLEVER. In this task, you will import the EDIF netlist you synthesized in the previous task into your project.

*To import the EDIF netlist you synthesized into your project:*

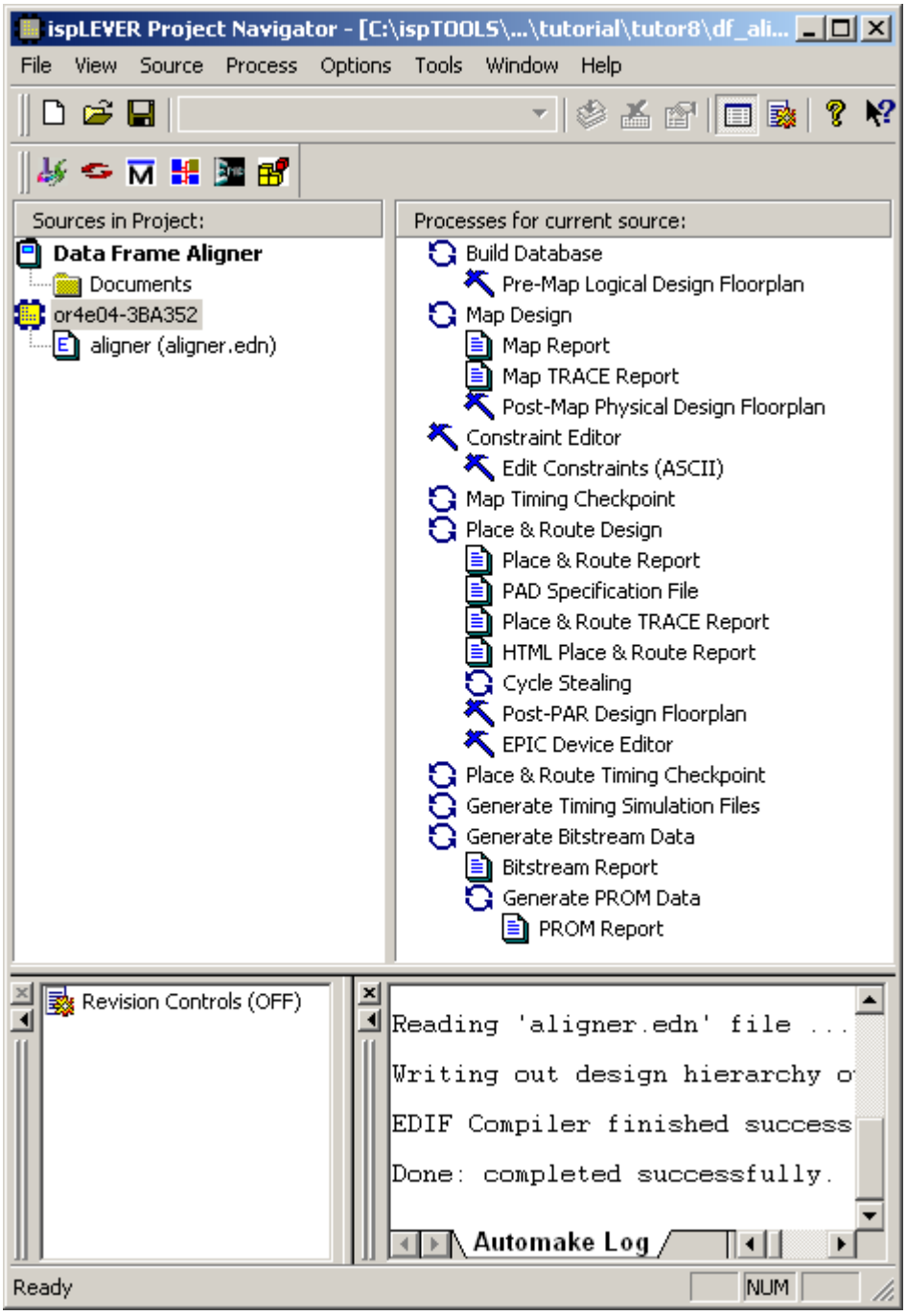
1. In the ispLEVER Project Navigator, choose **Source > Import** to open the dialog box.
2. Go to the **rev_1** folder, select **`aligner.edn`**, and then click **Open**.




3. In the Import EDIF dialog box under CAE Vendors, select **Synplicity** and click **OK**.



The software adds the selected EDIF file (`aligner.edn`) to the project sources.




***Note**: After you import an EDIF file into the ispLEVER project, it is always linked to the Project Navigator. Therefore, if you make changes and recompile your HDL file to create a new EDIF file, your project is automatically updated as well.*

## Task 7: Map the Design

In this task you will review Map options, run the Map program, and view the Map report. Using the EDIF netlist file you synthesized and imported into Project Navigator as input, you will actually run two processes, Build and Map. Before mapping can occur, the Build process automatically translates and builds your netlist into an ORCA-based database file. The ispLEVER software automatically does this netlist conversion when you start the Map process.

### About the Map Process

Mapping is the process of converting a design represented as a logical network of device-independent components (e.g., gates and flip-flops) in the input logical design file into a network of device-specific components, e.g., programmable functional units (PFU) to be placed on the physical device represented in the post-map physical design (`.ncd`) file. Before mapping occurs, the EDIF netlist input is automatically converted into a logical generic database file (`.ngd`) in terms of ORCA FPGA primitives during the Build operation. After mapping, the resulting physical description is output to a Physical Design file (`.ncd`), in terms of the components in the target architecture. This physical design can then be placed and routed.

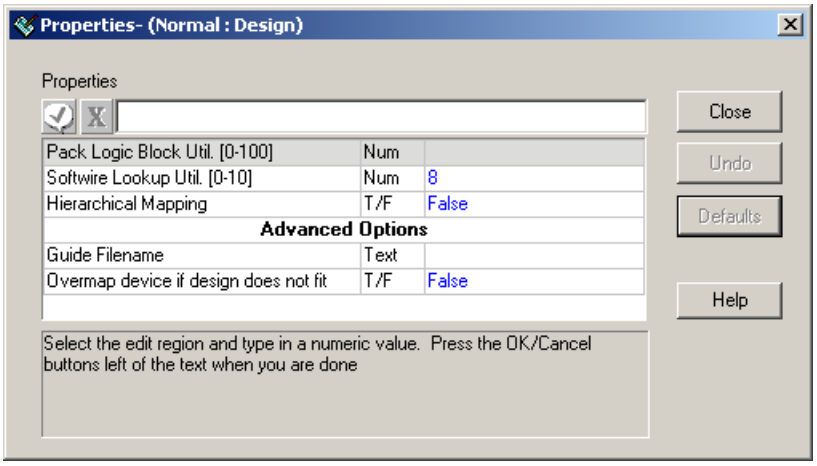
Also note that the resulting mapped `.ncd` files may include information based on user-defined attributes (ORCA properties) specified in the input netlist. For example, a property may specify where a component in the logical design must be placed in the physical device, or what nets should be given the highest priority when the design is routed. You can also use the ORCA Floorplanner to define component and regional grouping in the pre-map `.ngd` file in the logical domain and/or in the post-map `.ncd` in the physical domain.

To learn more about the Map process, refer to the "Mapping A Design" topic in the ispLEVER Help system. To learn more about using attributes (properties) in your netlist, download or view the *ORCA Properties for Design Entry Desk Reference* guide in PDF format using the Project Navigator: **Help > ispLEVER User Documents** command. See appropriate topics on floorplanning in ispLEVER for more on that subject.

*To review Map properties, run the Map process, and view the Map report:*

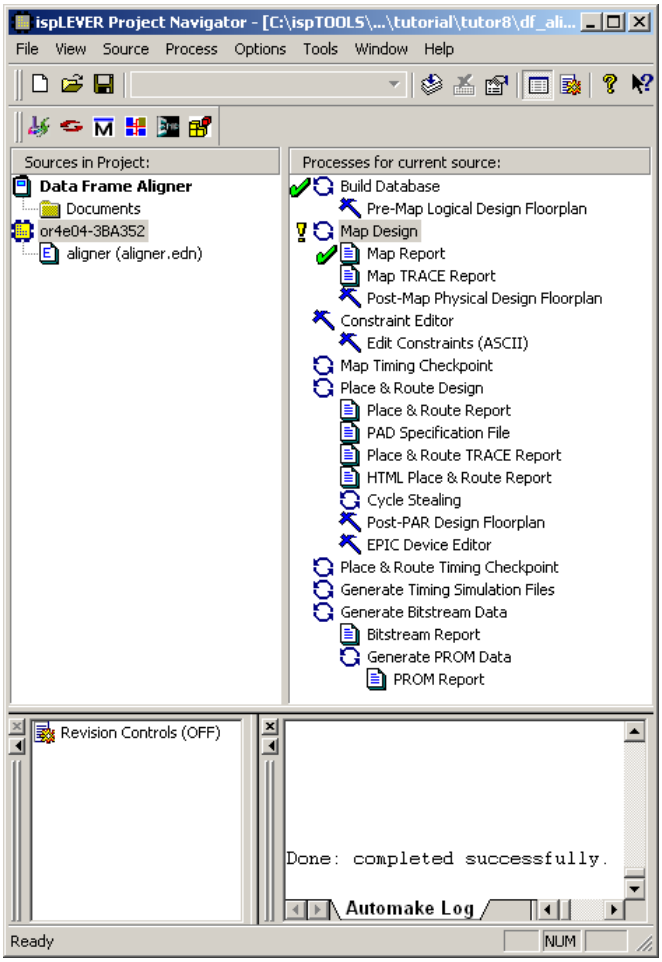
1. Before you run the Map program, you can set Map properties. Many ispLEVER processes have associated properties, which are displayed in the Properties dialog box.

   With the target device selected in the Sources window, right-click **Map Design** in the Processes window and choose **Properties** from the popup menu to open the dialog box.



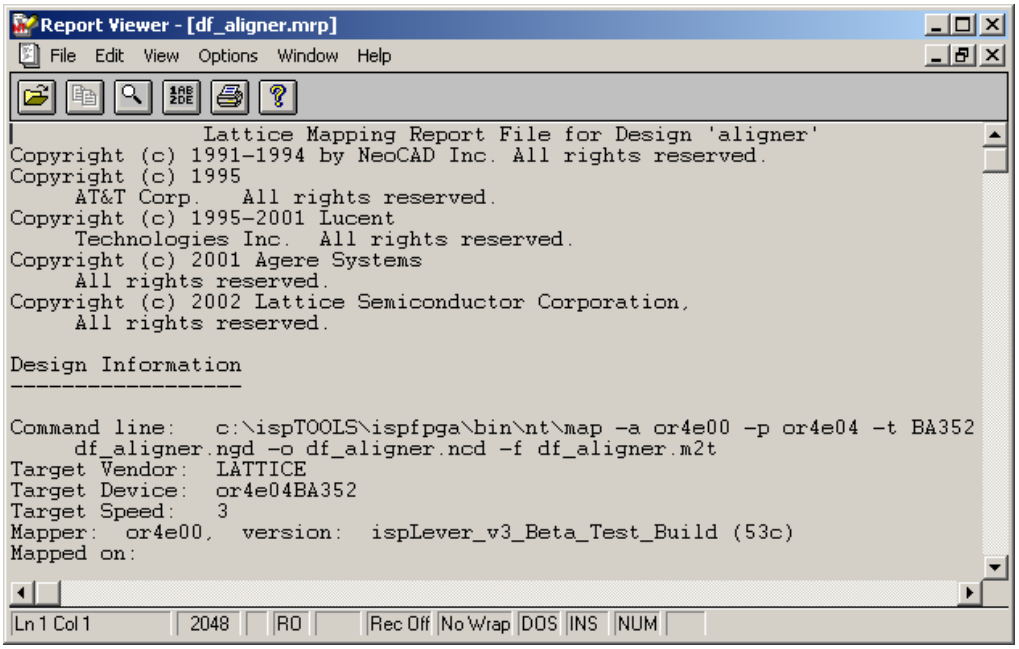

Properties can be True/False, List, or Text/Number. Accept the default properties and click **Close** to close the dialog box. Now you are ready to map the design.

2. In the Processes window, double-click the **Map Design** process. When the process is completed, a green check mark appears next to the Build Database processes. (Don't worry about the warning for Map Design.)



3. Double-click the **Map Report** process to open in the map report in the Report Viewer.




The Map Report (`.mrp`) file is an ASCII file containing information about the MAP command run. The `.mrp` file lists any DRC errors found in the design, details how the design was mapped (e.g., the schematic constraints specified, the logic that was removed or added, and how signals and symbols in the logical design were mapped into signals and components in the physical design). It also supplies statistics about component usage in the mapped design and contains information about the Map Design process run.

4. View the report and then choose **File > Exit** to exit the Report Viewer.

## Task 8: Place & Route the Design

After a design has undergone the necessary translation to bring it into the physical design format, you can run the Place & Route Design process (PAR). This process takes a mapped physical design file (`.ncd`), places and routes the design, and outputs another `.ncd` file.

### About the Place & Route Process

PAR works in timing-driven mode. The timing-driven approach uses the constraint file and various cost tables that assign weighted values to relevant factors such as constraints, length of connection, and available routing resources.

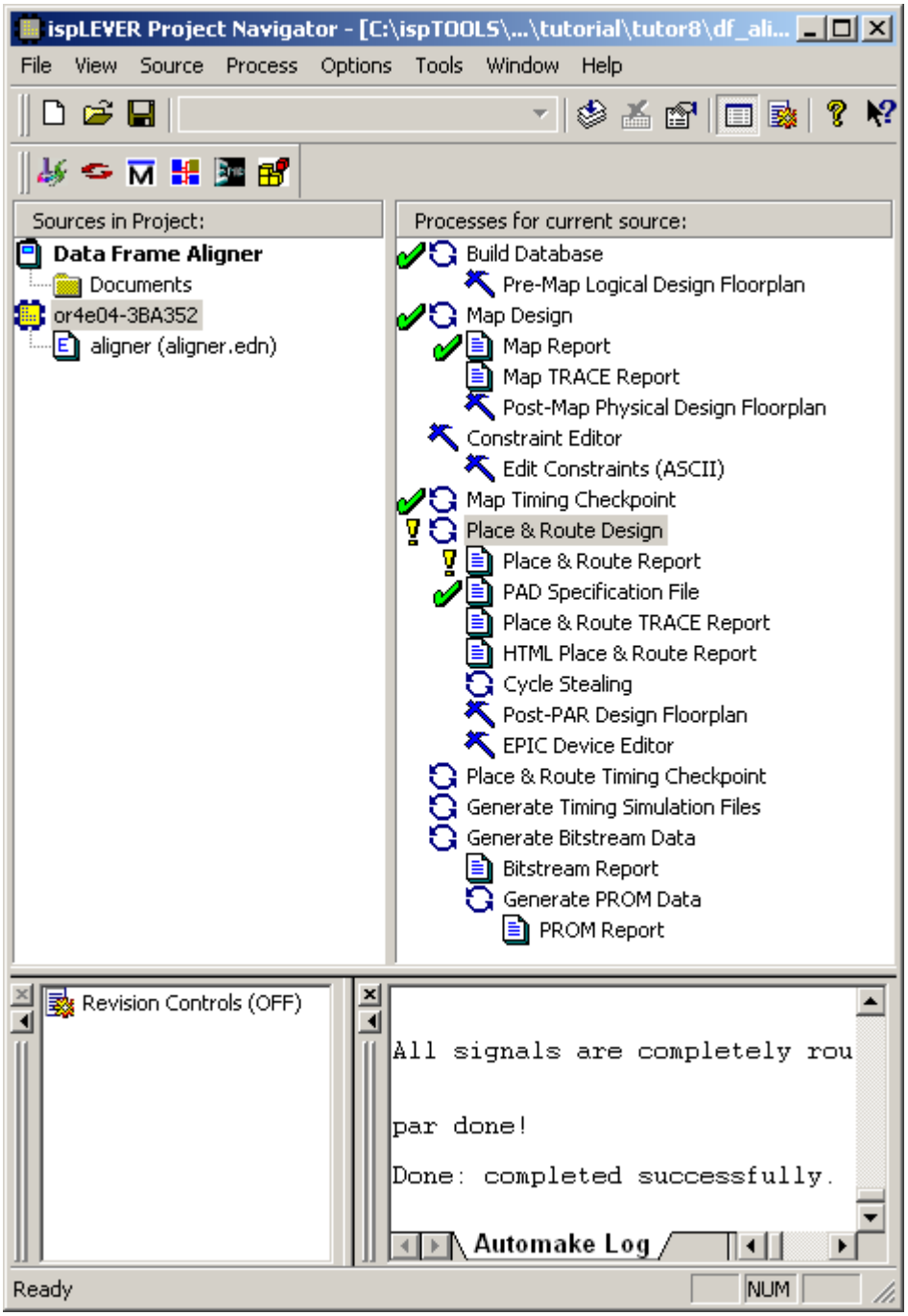
The PAR process places the mapped physical design file (`.ncd`) in two stages: a constructive placement and an optimizing placement. PAR writes the physical design after each of these two stages completes.

Routing is done in two stages: iterative routing and delay reduction routing (also called cleanup). PAR writes the physical design file (`.ncd`) only after iterations where the routing score has improved. During iterative routing, the router performs an iterative procedure to converge on a solution that routes the design to completion or minimizes the number of unrouted nets. During reduction routing, the router takes the result of iterative routing and re-routes some connections to minimize the signal delays within the device.

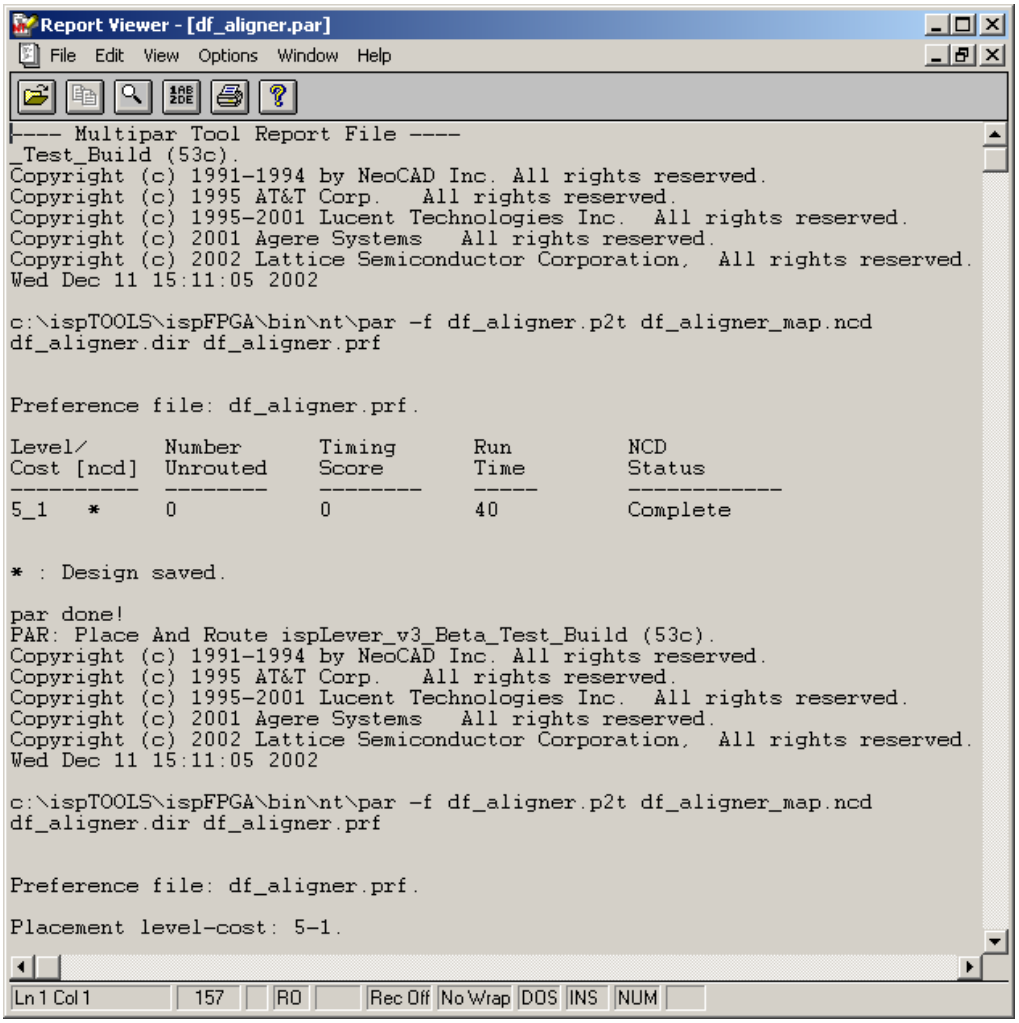
*To run Place & Route and view the reports:*

1. In the Processes window, double-click the **Place & Route Design** process. The ispLEVER software places and routes the design in the specified device and generates the Place & Route Report. When the process is completed, a green check mark appears next to the Place & Route process. (Don’t worry about the warnings.)




2. Double-click the **Place & Route Report** process to open the PAR report file (`.par`) in the Report Viewer. The `.par` file contains execution information about the Place & Route command run. The report also shows the steps taken as the program converges on a placement and routing solution.




3. View the report and then choose **File > Exit** to exit the Report Viewer.

## Task 9: Prepare for Simulation

The ispLEVER software supports third-party timing simulation with ModelSim™ from Mentor Graphics®. Using this integrated package, you can simulate a single Verilog design within one environment.

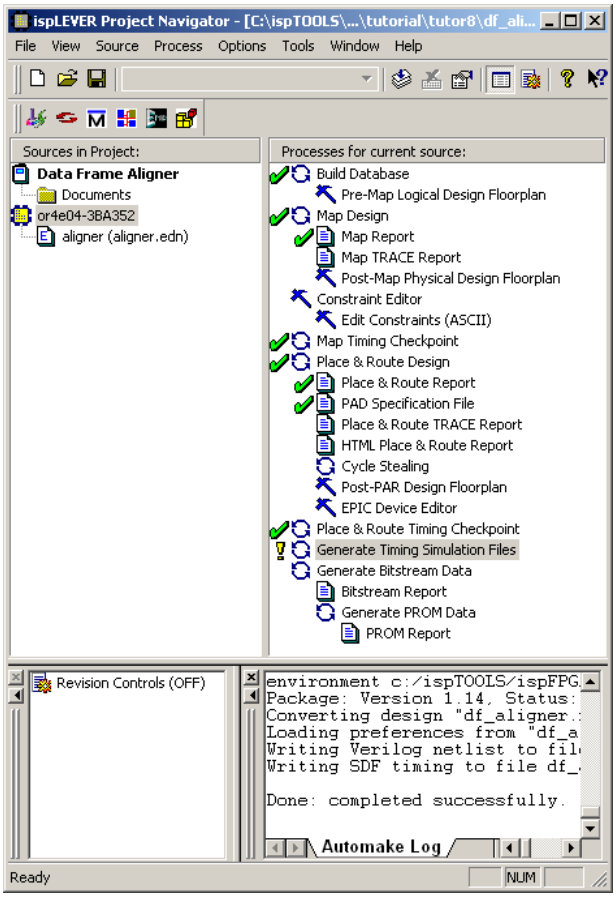
### About Timing Simulation

Where as timing *analysis* returns partial timing information, dynamic timing *simulation* will give you detailed information about gate delays and minimum and worst-case circuit conditions. Because total delay of a complete circuit will depend on the number of gates the signal sees and on the way the gates have been placed in the device, timing simulation can only be run after the design has been implemented.

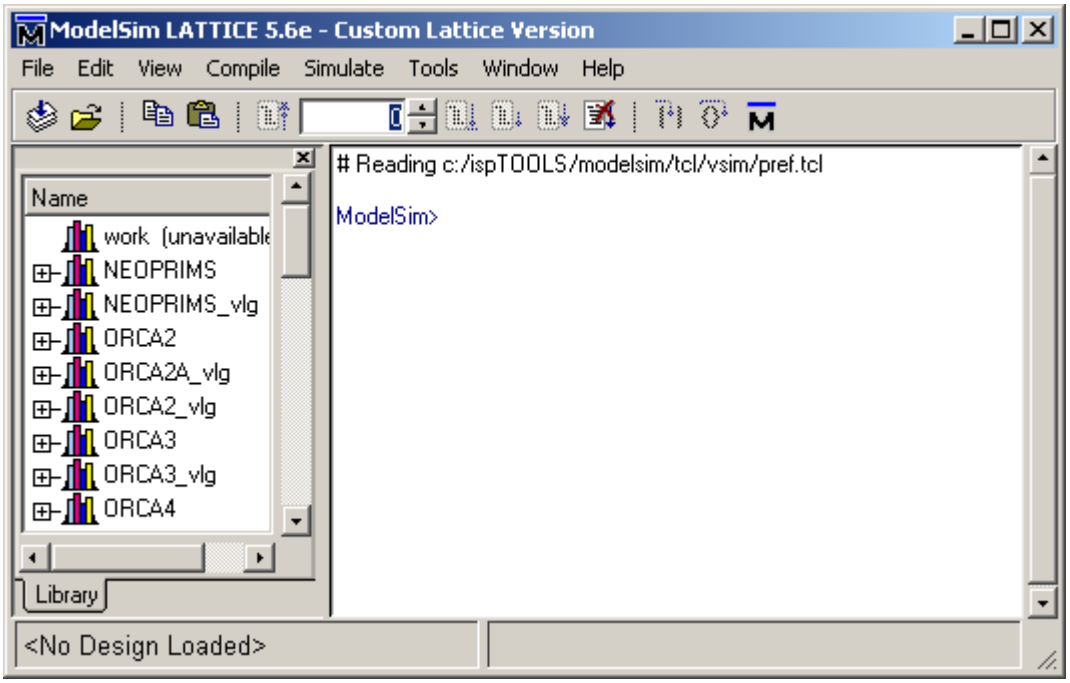
Timing simulation also requires several input files to run a Verilog netlist, a delay file, and a test fixture. The netlist and delay files are automatically generated from within ispLEVER. The test fixture must be written before hand.

*To create the timing simulation files and start ModelSim:*

1. In the Processes window, double-click the **Generate Timing Simulation Files** process. The software writes two files to the project directory: `df_aligner.v` (the Verilog netlist) and `df_aligner.sdf` (the standard delay file). (Ignore the warnings.)



2. To run ModelSim for timing simulation, in the Project Navigator choose **Tools > ModelSim Simulator**.




**Note**: To complete this task, you would need a Verilog test fixture file, which is not included as part of this tutorial.

3. Close ModelSim.

## Congratulations

You have completed the HDL Synthesis Design with Synplify tutorial. In this tutorial you have learned how to:

- Use ispLEVER to create a new EDIF project and target a device.
- Launch Synplify from within ispLEVER, synthesize your Verilog design, and generate an EDIF netlist file.
- Import the EDIF file into the ispLEVER.
- Implement the design using the Map, Place, and Route processes and view the reports.
- Prepare the design for timing simulation using ModelSim.