RGMII to GMII Bridge

Reference Design

FPGA-RD-02136-2.4

January 2020

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1. Introduction

GMII (Gigabit Media Independent Interface) is an Ethernet interface standard, and RGMII (Reduced Gigabit Media Independent Interface) is intended to be an alternative to GMII. The principle objective of RGMII is to reduce the number of pins from 22 to 12 in a cost-effective and technology-independent manner. This reference design provides a bi-directional bridge function for transferring data between RGMII and GMII.

2. Features

- Data bridging from GMII to RGMII
- Data bridging from RGMII to GMII
- Works at >125 MHz
- Uses the HSTL I/Os with no additional HSTL buffers required

3. Functional Description

This reference design provides bridging from GMII to RGMII and from RGMII to GMII. The pins of this design are divided into two sides, the GMII side and the RGMII side. This design assumes both the GMII device and RGMII device are external devices, even though both can be implemented inside the programmable logic. Figure 3.1 shows an example of how the interface is used when the design is targeted to a Lattice FPGA.

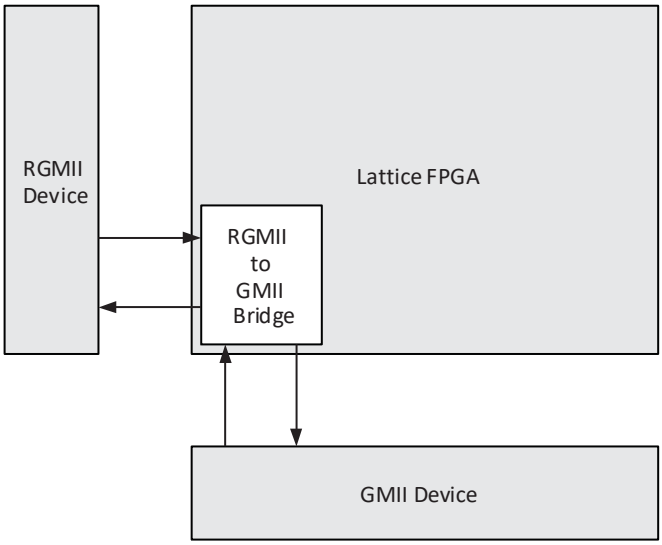

Figure 3.1. System-Level Diagram

The RGMII to GMII Bridge reference design transfers data at double data rate (DDR). Double data rate allows data to be transferred on both rising and falling edges of the clock and therefore doubles the data throughput. The FPGA has I/O shift registers (IOSR) available for each group of PIOs that are programmed to work together and transfer data on both clock edges. The DDR elements in the Lattice Diamond® software library are used on the RGMII side. The input/output signal diagram is shown in Figure 3.2.

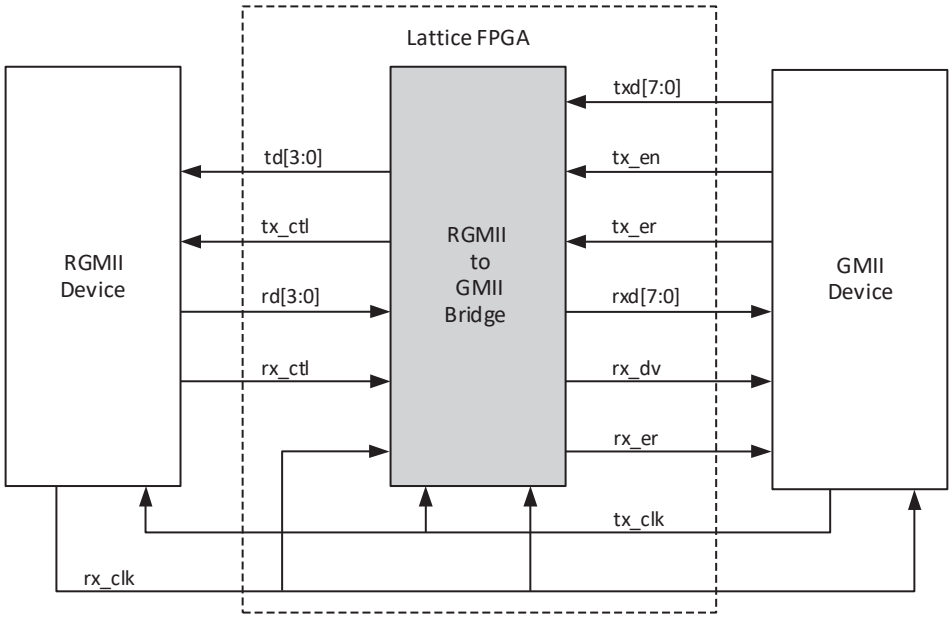

Figure 3.2. Input/Output Signal Diagram

The signal descriptions are provided in Table 3.1.

Table 3.1. Signal Descriptions

Signal Name	I/O Type	I/O Standard	Function/Connection Description
tx_clk	I	HSTL*	Transmit clock
rx_clk	I	HSTL*	Receive clock
td[3:0]	O	HSTL*	Transmit data out to the RGMII device, bits 3:0 on the rising edge of tx_clk, and bits 7:4 on the falling edge of tx_clk.
tx_ctl	O	HSTL*	Control signal for transferring other Tx signals to the RGMII. The signal tx_enis transferred to RGMII on the rising edge of tx_clk, and tx_eris transferred on the falling edge of tx_clk.
rd[3:0]	I	HSTL*	Receive data in, from the RGMII device, bits 3:0 on the rising edge of rx_clk, and bits 7:4 on the falling edge of rx_clk.
rx_ctl	I	HSTL*	Control signal for transferring other Rx signals from the RGMII. The signal rx_enis transferred on the rising edge of rx_clk, and rx_dvon the falling edge of rx_clk.
txd[7:0]	I	HSTL*	Transmit data in from the GMII device.
tx_en	I	HSTL*	Transmit enable, from the GMII device, active high.
tx_er	I	HSTL*	Transmit data error, from the GMII device, active high.
rxd[7:0]	O	HSTL*	Receive data output to the GMII device.
rx_dv	O	HSTL*	Receive data enable, to the GMII device, active high.
rx_er	O	HSTL*	Receive data error, to the GMII device, active high.

***Note:** ECP5™ devices cannot support HSTL15 I/O standard. LVCMOS25 is the I/O standard used for ECP5™ devices.

4. Waveforms

The design has been verified through RTL function simulation and timing simulation. The following figures are the timing waveforms of the design. For detailed timing waveforms, please download the design and run the RTL function simulation.

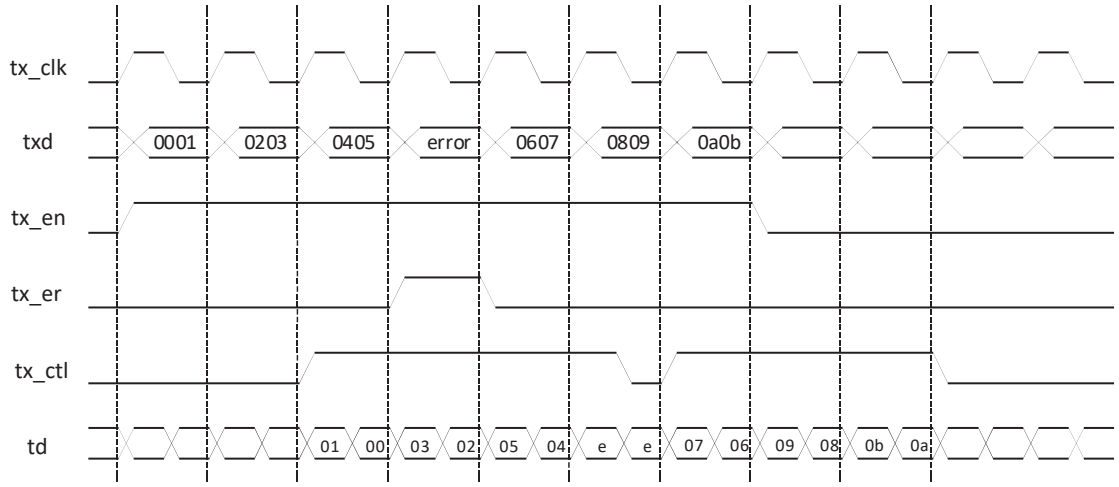

Figure 4.1. Timing Waveforms for Transmit Data

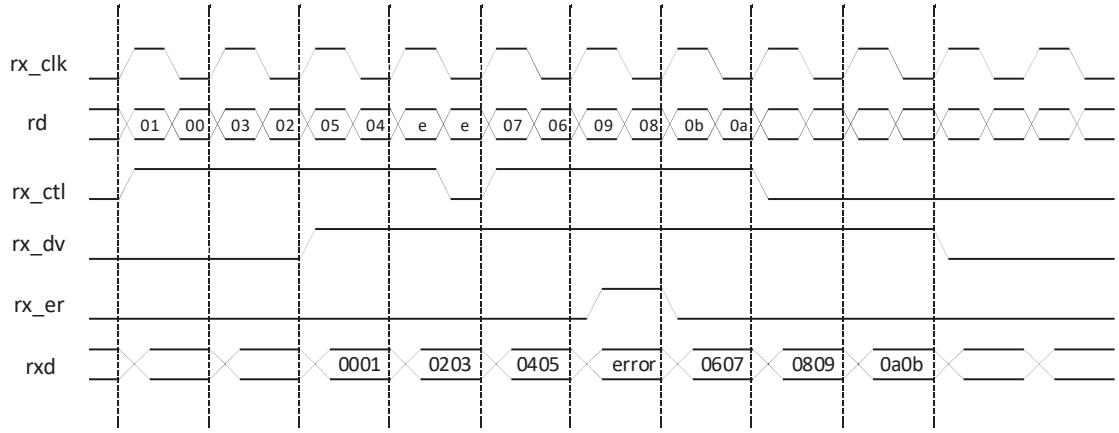

Figure 4.2. Timing Waveforms for Receive Data

5. Implementation

This design is implemented in Verilog. When using this design in a different device, density, speed, or grade, performance and utilization may vary. Default settings are used during the fitting of the design.

Table 5.1. Performance and Resource Utilization

Device Family	Language	Speed Grade	Utilization (LUTs)	f_{MAX} (MHz)	I/Os	Architecture Resources
ECP5™ [4]	Verilog	-8	4	>125	33	2 PLLs, 5 ODDR
LatticeECP3™ [1]	Verilog	-7	4	>125	33	2 PLLs, 5 ODDR
LatticeECP™/ LatticeEC™ [2]	Verilog	-4	3	>125	33	2 PLLs, 5 ODDR
LatticeXP™ [3]	Verilog	-4	3	>125	33	2 PLLs, 5 ODDR

Notes:

1. Performance and utilization characteristics are generated using LFE3-95EA-7FN1156C, with Lattice Diamond 3.8 design software.
2. Performance and utilization characteristics are generated using LFEC20E-4F672C, with Lattice Diamond 3.8 design software.
3. Performance and utilization characteristics are generated using LFXP10E-4F256C, with Lattice Diamond 3.8 design software.
4. Performance and utilization characteristics are generated using LFE5UM-85F-8BG756C, with Lattice Diamond 3.8 design software with LSE (Lattice Synthesis Engine).

Note: The Maximum Clock Frequency is obtained by running the timing analysis with the Lattice design software. Timing simulation should be run after any changes are made and the reference design is merged with the overall design.

Reference Design Package

The files provided in the reference design package are listed in the rd1022_ReadMe.txt file under the “docs” directory.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 2.4, January 2020

Section	Change Summary
All	• Changed document number from RD1022to FPGA-RD-02136. • Updated document template.
Disclaimers	Added this section.

Revision 2.3, November 2016

Section	Change Summary
Functional Description	Added note to Table 3.1 on ECP5 I/O standard limitation.
All	Added support for Lattice Diamond 3.8 design software.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 2.2, March 2014

Section	Change Summary
Implementation	Updated Table 5.1, Performance and Resource Utilization. • Added support for ECP5 device family. • Added support for Lattice Diamond 3.1 design software.
All	Updated corporate logo.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 2.1, April 2011

Section	Change Summary
Implementation	Added support for LatticeECP3 device family.
All	Added support for Lattice Diamond 1.2 design software.

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