Reliability and Quality Assurance

April 2003

Introduction

Lattice Semiconductor Corporation (LSC) designs, develops and markets high performance programmable logic devices (PLDs) and related development system software. Lattice Semiconductor is the inventor and world's leading supplier of in-system programmable (ISP™) CPLDs and FPGAs. PLDs are standard semiconductor components that can be configured by the end customer as specific logic functions, enabling shorter design cycle times and reduced development costs. Lattice Semiconductor products are sold worldwide through an extensive network of independent sales representatives and distributors, primarily to original equipment manufacturers (OEMs) of communications, computing, industrial controls and military systems. Lattice Semiconductor was founded in 1983 and is based in Hillsboro, Oregon.

Our mission statement is Lattice Semiconductor will consistently conceive, develop, and deliver field programmable solutions which create extraordinary value for our customers, provide outstanding returns for our shareholders and, in turn, bring reward and pride to all our employees for a job well done.

The keys to Lattice success are as follows:

- Consistently provide innovative solutions to the market ahead of the competition.
- Continuously set new industry standards in total customer satisfaction.
- Build an organization comprised of individuals who take ownership, drive for results, and demonstration the passion to win.

Individuals working in teams, making and meeting commitments to achieve mutual objectives serve as the foundation for our success.

Lattice Quality Systems

At Lattice Semiconductor, quality is a corporate responsibility and an integral part of all operational activities. Lattice Semiconductor became the first major PLD manufacturer to complete ISO 9000 registration. Lattice Semiconductor's Quality Systems have been certified and the company has been continually fully registered to the ISO9001 standard since September 1993.

Certification to the ISO 9000 standard provides a recognized and standardized basis for the continued development of the quality and reliability of LSC products. This certification assures Lattice Semiconductor's customers that its Quality Systems are well organized and embody a "Quality First" philosophy. It also reaffirms Lattice Semiconductor's promise to provide its customers with the highest quality and most reliable products in the industry.

Lattice Semiconductor's quality system is described in the Lattice Quality Manual available at http://www.latticesemi.com. Lattice Semiconductor's Quality Assurance organization is independent from Manufacturing and is a core function management responsibility, assuring sufficient authority is afforded to quality issues.

Lattice Semiconductor maintains complete on-line documentation and computer aided manufacturing systems to control manufacturing. Internal specifications are in compliance with applicable JEDEC and Military standards. Lattice Semiconductor's computer aided manufacturing enables complete Fabrication and Assembly lot traceability. Lattice Semiconductor maintains a network of Application and Quality engineering personnel to support customers in the design, manufacturing, and distributions of its products.

Lattice Semiconductor's quality program is in full compliance to the quality assurance requirements of MIL-I-38535B Appendix C and all inspection systems requirements of MIL-I-45208.

Manufacturing Partners

All Lattice Semiconductor Wafer Foundry and Assembly/Test manufacturing partners are high volume top tier industry recognized sources. Lattice Semiconductor requires these key suppliers to maintain Quality System ISO9000 and Environmental System ISO14000 registrations. Key suppliers are audited periodically to monitor their compliance to Lattice Semiconductor quality initiatives and goals. Lattice Semiconductor samples incoming materials to provide feedback and continuous improvement of subcontractor performance with the main objective being to control quality at the source. Communications and in-line data are continuously exchanged to allow real-time monitoring of subcontractor manufacturing operations.

All test facilities, including all subcontractors, use Lattice Semiconductor specified test equipment and hardware. All test software is generated by Lattice Semiconductor with revision controlled by central test host based at Lattice headquarters and downloaded each day to all test facilities. Test data is transferred daily to Lattice Semiconductor.

Lattice Semiconductor purchases all direct materials and services affecting quality or reliability of end product from qualified sources. Selection of these critical suppliers is based upon quality system audits, product qualification testing, correlation studies, incoming inspection and demonstrated capability. A qualified supplier list is maintained.

Self Audit

Internal self audits of the entire quality and delivery system are regularly performed per written procedures. The functional audits evaluate actual method to written procedure. The results of these audits are documented and any discrepancies are brought to the attention of personnel responsible for the audited area. Deficiencies require corrective actions and these corrective actions are subsequently verified as to deployment and effectiveness. A periodic review of these functional audit results and corrective actions is performed by Quality Assurance.

Corrective/Preventive Action

All operational functions utilize a documented corrective action system coordinated, recorded and monitored by Quality Assurance. The system is designed to provide for proactive problem identification and resolution in a timely manner. Inputs include vendor, internal and customer related problems. Emphasis is placed on effective elimination of the root cause to prevent recurrence of the problem.

Lattice Semiconductor Management is responsible for ensuring that employees have sufficiently well defined responsibilities, authority and organizational freedom to identify potential quality related problems as well as initiate and implement solutions.

Continuous Improvement

Lattice Semiconductor works at providing innovative solutions for our customers. The primary tool is our continuous design enhancements to our products by adding features and making each generation of products more robust with respect to the product use environment. With our manufacturing partners, we work at continuous process enhancements and improvements to build better product performance and cost effective solutions.

Lattice Semiconductor offers the best available device packages to our customers allowing for space efficient and energy managed solutions.

Lattice Semiconductor reviews all product failures discovered during qualification testing, inspections, customer returns or in-process screening to determine the cause or relevancy of the failure. This information is used to initiate improvement actions to eliminate the root cause and generate the appropriate solutions.

Calibration

All equipment involved in determining product conformance to specifications through inspection, measurement, or testing meet the required accuracy. Equipment is calibrated and maintained on defined intervals against a nationally recognized standard. In addition, equipment exhibits a calibration status to safeguard against unauthorized adjustments.

Training

Key manufacturing personnel complete a formal training program and obtain certification for each operation before they are allowed to perform activities affecting quality. Methods and records identifying the type and extent of training are maintained and recertification required on an annual basis.

Lattice Semiconductor performs comprehensive testing and manufacturing controls on all its products. Figure 1 shows a typical product manufacturing flow.

Lattice Quality

Lattice Semiconductor Corp. has a comprehensive program for Quality Sampling to ensure outgoing product meets all datasheet requirements and customer expectations. The sampling plan includes Electrical and Visual/Mechanical inspections of product. Sample sizes are determined by the production lot size and device technology family.

Outgoing Quality Sampling is performed in conformance to written Lattice Semiconductor procedures. The QA Visual Mechanical Inspection Process (Doc #70-103064) defines the requirements for package and lead inspection. The Electrical In-line QA and CQA Sampling Instruction (Doc #70-102963) defines the requirements for device electrical testing. All product inspected using these procedures must meet all datasheet parameters prior to shipment.

This quality conformance testing program ensures Lattice products meet datasheet expectations. This program also provides valuable feedback to our manufacturing systems to identify continuous improvement opportunities. Defective product is analyzed to determine the root cause of failure, and corrective actions are implemented to eliminate future issues. Lattice has used this program to drive outgoing product quality to industry leading levels.

Lattice Product Reliability

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, data is continuously accumulated through ongoing monitor programs.

All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Policy (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are contained in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from the Lattice Semiconductor sales office.

Failure rates in this reliability report are expressed in FITS. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Each new product is fully characterized for device performance and reliability. Product families are qualified based upon the requirements outlined in Table 1. Reliability monitors are based on the schedule outlines in Table 2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

Customer Issue Resolution Process
Product Analysis Request System

Lattice Semiconductor Corporation maintains a Worldwide Product Analysis Request (PAR) system to provide prompt responses to customer inquiries on integrated circuits, packaging and shipment materials, and anything of an administrative nature. The focus of the system is on identification of root cause, and the corrective actions necessary to resolve or eliminate the problem. Permanent solutions and improved systems are used to prevent recurrence. In addition, this system provides Lattice information used to improve the product design, manufacturing, and service areas. The goal is to improve our systems and services to prevent future issues.

Using the PAR system is straightforward. The customer only needs to contact their local Lattice sales office, Field Applications Engineer, or sales representative. A request form with failure information is then completed and sent to the Lattice factory to start the process. A PAR tracking number will be assigned, and routing information will be provided if parts need to be returned. During the analysis process, communication is maintained with the requestor to ensure complete analysis and correlation of root cause to customer reported symptoms.

Turnaround times are set to satisfy the customer's need for resolution, and Lattice's need for rapid information to resolve quality, reliability, or corrective issues. Lattice targets the cycle times in Electronics Industry Association specification EIA-671 for Initial and Final Responses.

The objective of the PAR system is to provide timely analysis to customer requests, and provide valuable feedback to our systems and development processes. This ensures Lattice will provide the highest quality and reliability Programmable Logic Product available.

Conclusion

Lattice Semiconductor is committed to industry leadership in the supply of high performance logic components and design tools. We strive for customer satisfaction through on-time delivery of innovative products with the highest level of quality and reliability.

The combination Lattice Semiconductor's ISO 9000 Quality Systems, World-class Wafer Foundry and Assembly/Test manufacturers partners, innovative programmable logic products, proven reliability, and Top rated customer service makes Lattice Semiconductor the supply source of programmable logic devices.

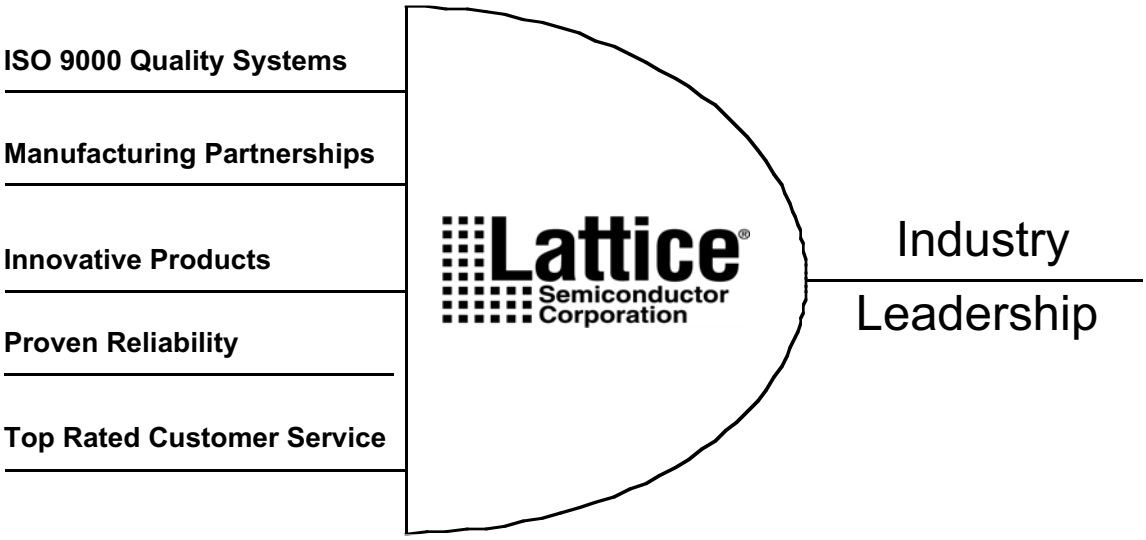
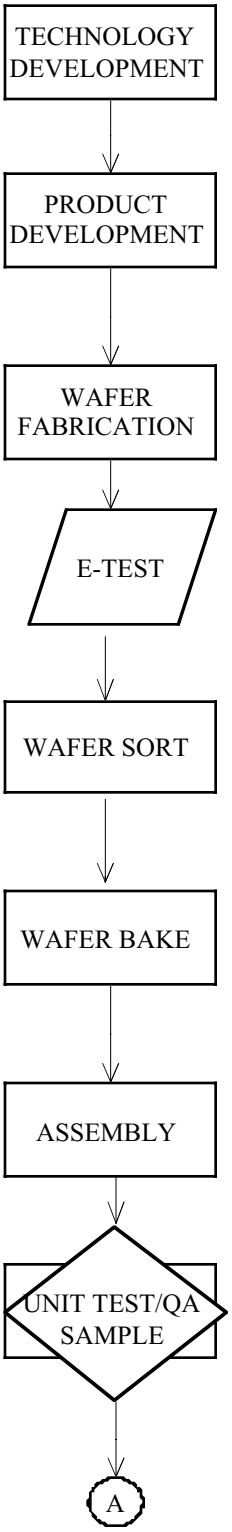
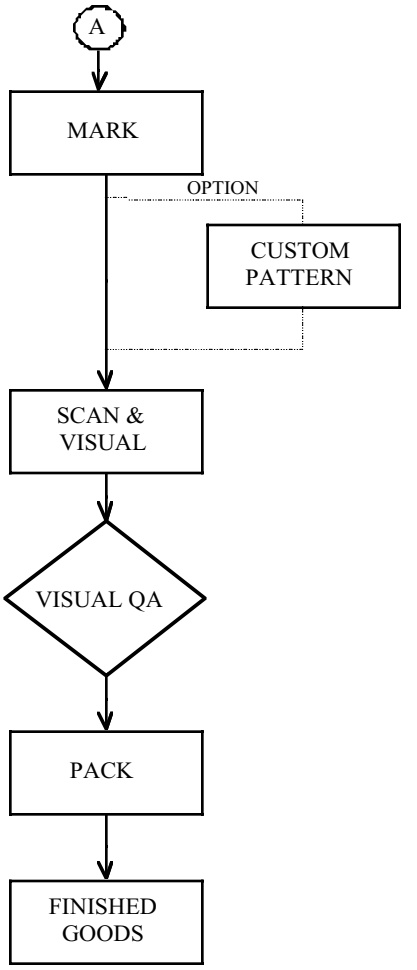


Figure 1. MANUFACTURING FLOW



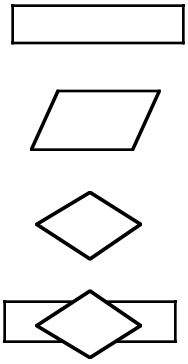
DESCRIPTION	DOC #
Define, simulate, characterize and qualify wafer fabrication process.	57-102785
Define, design, simulate, layout, characterize and qualify new design.	58-102965
Foundry operation utilizing SPC on in-line data.	60-102964
5 wafer/lot sample; measure and trend process parameters.	80-102590
DC, functional and reliability testing at the wafer level.	80-102592
Temperature stressing of E2 cells for enhanced reliability.	81-102592
Subcontracted operation utilizing SPC on in-line data.	81-100145
100% AC/DC and functional testing utilizing multiple patterms at maximum operating temperature with in-line QA sampling (LTPD=2)	88-102790

COMMERCIAL PRODUCTS



DESCRIPTION	DOC #
Topside ID retaining full traceability to wafer lot.	92-103054
Optional customization with customer specified pattern.	80-102690
100% lead scan and visual inspection for defects.	92-103054
QA sample (LTPD=2).	70-103064
Final count and packaging into final ship containers.	92-103054
Packed and finished stock ready for shipments.	94-102933

LEGEND - FLOW DIAGRAM SYMBOLS



PRODUCTION STEP

PRODUCTION GATE

QA GATE

PRODUCTION STEP + IN-LINE QA GATE

Table 1. RELIABILITY TESTING

1. QUALIFICATION TESTING				
TEST	**STANDARD**	**TEST CONDITIONS**	**SAMPLE SIZE**	**PERFORMED ON**
High Temperature Operating Life HTOL	Lattice Procedure # 70-101566, MIL-STD-883, Method 1005, JESD22-A108-A GAL Products ispLSI Products	125° C, 5.5/3.6V Vcc, 168, 500, 1000, 2000 hours. Preconditioned with 100 read/write cycles Preconditioned with 1000 read/write cycles	77/lot 2 lots typical	Design, Fab Process Package Qualification
High Temp Retention	Lattice Procedure # 70-101567, JESD22-A103-A	Vcc=5.25/3.6V, 150° C, 2K hours, Devices are preconditioned with 100 read/write cycles	77/lot 2 lots typical	Design, Fab Process, Package Qualification
Temperature Cycling	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Cond. B JESD22A104-A	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45/lot 2 lots typical	Design, Fab Process, Package Qualification
Endurance - Program/Erase Cycling	Lattice Procedure, # 70-101569	Program/Erase ispLSI devices to 10x specified datasheet cycles	10/lot 2 lots typical	Design, Fab Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JEDS22-A114-A	Supply voltage applied during measurement=5V HBM minimum 2000V[1, 2, 3]	3/lot 2 lots typical	Design, Fab Process, Package Qualification
ESD CDM	Lattice Procedure # 70-100844, JEDS22-C101-A	Charged Device model (CDM) sweep to 1500 volts[1, 2, 3]	3/lot 2 lots typical	Design, Fab Process, Package Qualification
Latch Up Resistance	Lattice Procedure # 70-101570, JESD 17	±200ma on I/O's, Vcc +50% on Power Supplies	2/lot 2 lots typical	Design, Fab Process, Package Qual
Moisture Resistance 85/85 Biased HAST	Lattice Procedure # 70-101571, JESD22-A101-B JESD22-A110-B	Vcc = 5.0/3.3V biased 85° C, 85% Relative Humidity, 1000 hours Vcc = 5.0/3.3V biased 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45/package family 2 lots typical	Design, Fab Process Package Qualification Plastic Pkg. only
Solderability	Lattice Procedure # 70-100212, MIL-STD-883E, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245° C + 5° C	3 devices 22 leads/device	Package Qualification

1. ESD results do not include temperature sensing diode pins (PTEMP pins for all ORCA Series 4 FPGA and FPSC devices).

	Device	**ESD HBM (Minimum)**	**ESD CDM (Minimum)**
2.	ORT82G5	±1500V to ±2000V	±500V to ±1000V
3.	ORSO82G5	±1500V to ±2000V	±500V to ±1000V

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE	PERFORMED ON
Lead Integrity	Lattice Procedure # 70-100192, MIL-STD-883E, Method 2004	PDIP, CDIP packages	3 devices	PDIP, CDIP package Qualification
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or appl. LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification
Unbiased HAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45/package family	Fab Process, Package Qualification Plastic Pkg. only
Surface Mount Pre-conditioning	Lattice Procedure # 70-103467, Jedec J-STD-020A CPLD - MSL 3 SPLD - MSL 1	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 168hr. 85/85 Soak 3 SMT simulation cycles.	100 devices/ Package Family	Plastic Packages only

Other Qualification Tests **(For Hermetic/Military Products Only) Testing is done 1 time/year/pkg. type**				
TEST	**STD**	**TEST CONDITIONS**	**SAMPLE SIZE**	**PERFORMED ON**
Wire Bond Strength Bond Strength Group B	Lattice Procedure # 70-100220 MIL-STD- 883, Method 2011, Condition D	6 gr. min. for 1.25 mil gold wire 3 grs min. for 1.25 mil AL wire	15 pieces per pkg. per year 15 leads	Design, Fab Process, Package Qualification PDIP. only
Thermal Shock	Lattice Procedure # 70-100612, MIL-STD- 883, Method 1011	Measure all dimensions listed on the case outline and compare with case outline limits. Note any failed dimensions on the lot traveler. 4/30/97	15 pieces per pkg. per year	Hermetic packages only
Vibration	Lattice Procedure # 70-100613, MIL-STD- 883 Method 2007.2	Leakage, visual, functional 20-2000 Hz for 10 min. 20q's for 4 min. in 3 planes, limit of .06" (24 mm) of movement	15 leads 15 pieces per pkg. per year	Hermetic packages only
Salt Water Spray Salt Atmosphere	Lattice Procedure # 70-100614, MIL-STD- 883 Method 1009.8	Less than 5% of metal surfaces covered with corrosion	15 pieces per pkg. per year	Hermetic packages only
Constant Acceleration Centrifuge	Lattice Procedure # 70-100611, MIL-STD- 883 Method 2001.2	Acceleration:= 30KG m/sec. Leakage, visual, functional	15 pieces per pkg. per year	Hermetic packages only Design, Fab Process, Package Qualification
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or appl. LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	All package types
Resistance to Solvents Mark Permanency	Lattice Procedure # 70-101102, MIL-STD-883, Method 2015	Mark legible in one of 4 solutions. Monitor if mark is degrading.	4 units 3 lots of each pkg.	All package types
Mechanical Shock	Lattice Procedure # 70-100613, MIL-STD- 883, Method 2002 Cond. B	Leakage, visual, functional 1500gms for 5ms.	15 pieces per pkg. per year	Hermetic packages only

Table 2. RELIABILITY MONITOR TESTING

2. Reliability Monitor				
TEST	**STD**	**TEST CONDITIONS**	**SAMPLE SIZE**	**PERFORMED ON**
High Temperature Operating Life HTOL Early Life Inherent Life	Lattice Procedure # 70-101566, MIL-STD-883, Method 1005, JESD22-A108-A	Preconditioned datasheet read/write cycles 125° C, 5.25/3.6V Vcc, 168 hours. 125° C, 5.25/3.6V Vcc, 1000 hours.	200 devices/ Process Technology/ Month 100 devices/ Process Technology/ Month	Released Process Technologies

3. QA Package Monitor				
TEST	**STD**	**TEST CONDITIONS**	**SAMPLE SIZE**	**PERFORMED ON**
Resistance to Solvents	Lattice Procedure # 70-101102, MIL-STD-883, Method 2015	Mark legible in one of 4 solutions. Monitor if mark is degrading.	10 units/ Package family/ Subcontractor /month	All package
Lead Integrity	Lattice Procedure # 70-100192, MIL-STD-883E, Method 2004	PDIP, CDIP packages	5 devices / Package family/ Subcontractor /month	PDIP packages only
Solderability	Lattice Procedure # 70-100212, MIL-STD-883E, Method 2003	Steam Pre-conditioning 4-8 hours. Solder dip at 245°C+5°C	22 leads 3 devices/ Package family/ Subcontractor /month	All packages
Scanning Acoustic Tomography	Lattice Procedure # 70-103772 J-STD-035		10 units/ Package family/ Subcontractor /month	All plastic packages